A Prototype Front-End Readout Chip for Silicon Microstrip Detectors Using an Advanced SiGe Technology

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Abstract

The upgrade of the ATLAS detector for the high luminosity upgrade of the LHC will require a rebuild of the Inner Detector as well as replacement of the readout electronics of the Liquid Argon Calorimeter and other detector components. We proposed some time ago to study silicon germanium (SiGe) BiCMOS technologies as a possible choice for the required silicon microstrip and calorimeter front-end chips given that they showed promise to provide necessary low noise at low power. Evaluation of the radiation hardness of these technologies has been under study. To validate the expected performance of these technologies, we designed and fabricated an 8-channel front-end readout chip for a silicon microstrip detector using the IBM 8WL technology, a likely choice for the ATLAS upgrade. Preliminary electrical characteristics of this chip will be presented.

I. Introduction

The planned upgrade of the ATLAS Inner Detector will consist of an all silicon tracker consisting of several layers of pixel detectors and several layers of microstrip detectors. The inner strip layers will likely consist of short strips (~2.5 cm long) and the outer layers long strips (~10 cm long). The capacitive load of the sensors presented to the front-end amplifier circuit will be approximately 5 pF for the short strips and 15 pF for the long. These relatively large loads have in the past presented difficulty for CMOS front-end circuits if the required shaping time is tens of nanoseconds. That is, the bias current of the front-end FET will have to be large in order to achieve high enough trans-conductance to achieve low noise with fast shaping time. Under these conditions, bipolar transistors can often out perform CMOS with lower power for the same noise level. Silicon germanium technologies (SiGe) represent a modern bipolar version. They are designed to have very high f_Ts (e.g. 200 GHz) and achieve this by maintaining very low base resistance (tens of Ohms). The benefit for sensor readout circuits is that this low base resistance affords low noise at low bias current but fast shaping time.

We have been studying the radiation hardness of several SiGe technologies for several years and those results have been presented elsewhere [1], [2], [3], [4], [5], [6], [7]. In order to demonstrate the electrical performance of at least one technology, we have designed and fabricated an 8-channel prototype chip on the IBM 8WL technology. This was chosen primarily because the CMOS component of this BiCMOS technology is compatible with the IBM 8RF all CMOS technology that is being used by other ATLAS collaborators. This would allow a future full readout chip with a bipolar front-end and a CMOS back-end to make use of digital CMOS circuits already being developed on the 8RF process. There is another similar SiGe BiCMOS process, the 8HP, which also includes a 130 nm CMOS technology. The SiGe component of that technology is even higher performance than the 8WL but is it is also more costly. We chose the 8WL over the 8HP for this prototype primarily for cost considerations.

II. The Prototype Circuit

The 8-channel prototype chip is based upon the binary readout architecture used in the present ATLAS strip detector and planned for the upgraded detector, which yields only a simple hit or no-hit signal. Each of the 8 channels consists of a first stage preamp, a DC coupled second stage differential amplifier, followed by an AC coupled shaper stage, which differentially drives a comparator. There is global bias adjustment for the DC coupled differential amplifier, and control of the final shaping time using varactors. These adjustments would be controlled by on-chip programmable DACs in the final readout chip and allow optimization of performance for variations in input characteristics and radiation damage. Individual channel-by-channel adjustment of comparator threshold allows for compensation of DC matching offsets in the shaper and comparator. A block diagram of the circuit is shown in Figure 1.

Both analogue and digital supplies power the comparator. The digital signal is passed between the two sections by a differential current. The comparator CMOS output is converted to LVDS in the output stage of the actual prototype. The CMOS signal would become the input to the digital processing section (e.g. a pipeline, etc.) in a future full readout chip. This differential connection between analogue and digital sections insures negligible coupling between analogue and digital sections, thus reducing EMI noise. In this prototype front-end only chip, the digital section includes only an LVDS driver to send the signal off chip. For testing, these LVDS signals were fed to an FPGA for processing.

The separation of analogue and digital sections, even given the minimal digital components of this chip, allows

separate analysis of the analogue power consumption, one of the primary objectives of this study.

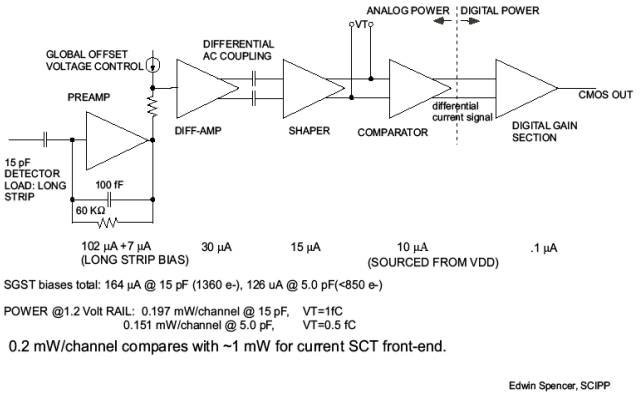

Figure 1: Block diagram of single channel with nominal bias and power settings indicated for each stage.

While the test results below show that the chip can operate successfully with the expected capacitive loads of the short and long strip silicon sensors, certain optimizations were made in the circuit design for the long strip option. Further optimization for the short strips, primarily a reduction in the front transistor size and a larger feedback resistor, would improve the noise vs. power performance for short strips.

III. TESTING

A. *The test board*

A test board was designed and fabricated to allow one chip to be completely tested. The board provided all the necessary power rails, the adjustable bias currents and voltages, current pulses to simulate sensor signals to each channel and connection of the LVDS output signals to an external FPGA. The response to different input loads could be tested by changing capacitors mounted on the board. A picture of the board is shown in Figure 2.

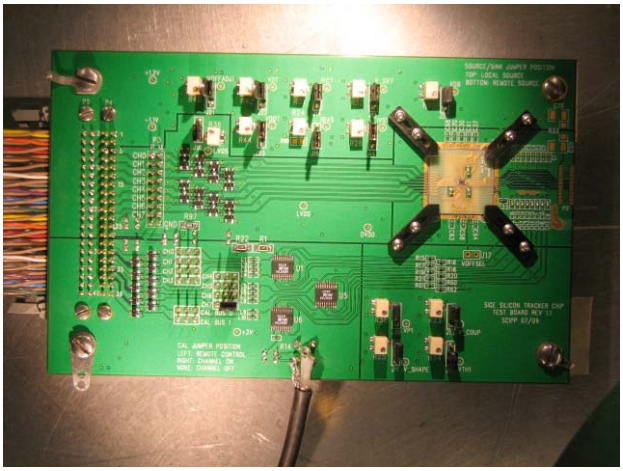

Figure 2: Test board with chip at right

The chip to be tested was not mounted directly on the test board but instead was glued and wire-bonded to a mini-board, which was then mounted in a shallow cavity in the test board. Wire bonds electrically connected the traces on the mini-board to the corresponding nodes on the test board. The mini-board was secured mechanically with Delrin clamps and covered with a plastic cap to protect the wire bonds. A close-up of this part of the test board is shown in Figure 3.

By breaking the wire bonds between mini-board and test board, the mini-board with chip can be removed and irradiated without exposing all the support components on the test board to radiation damage since most of them are not rad-hard. This strategy also minimizes the activation of the chip and mini-board during irradiation. After irradiation, the mini-board can be re-mounted and the wire bonds restored for post-radiation testing. Care was taken to keep traces on the mini-board to a minimum in order to minimize stray inductances, which might confuse the expected low noise, high performance of the chip.

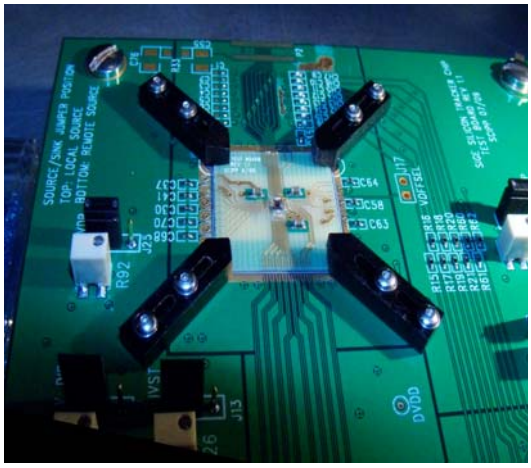

Figure 3: Close-up of mini-board with Delrin clamps

While the chip is fully capable of reading out a real silicon sensor, a new test board would have to be designed which mounted the chip in a position where it could easily be attached to a sensor. As of now, we have only tested the chip on this test board with simple chip capacitor loads and externally supplied input signals. Radiation testing is also planned for the future.

B. *Measurements*

Figure 4 shows scope traces to illustrate shaper signal timewalk. Shaper signals are buffered by source followers for Picoprobe measurements. Traces are 1 fC, 1.25 fC, and 10 fC. Vertical cursors intersect the 1.25 fC and 10 fC signals at 1 fC threshold. The measured timewalk is 13.6 ns. Two amplifiers have varactor capacitors with the controlling VSHAPE = 1.000 V in this case, so that shape can be tuned for a specific timewalk.

Figure 5 and Figure 6 show how the shaper signal is affected by VSHAPE and input load capacitance. The figures show one side of the differential shaper signal with a 1 fC input and Ibias at 120 µA and two different input loads. The three signals shown correspond to VSHAPE = 1.5 V, 0.75 V, 0. V (highest amplitude to lowest). The signal peak shifts

10.8 ns over the VSHAPE range for a 3.31 pF load, and only slightly less, 8.4 ns, for 19 pF load.

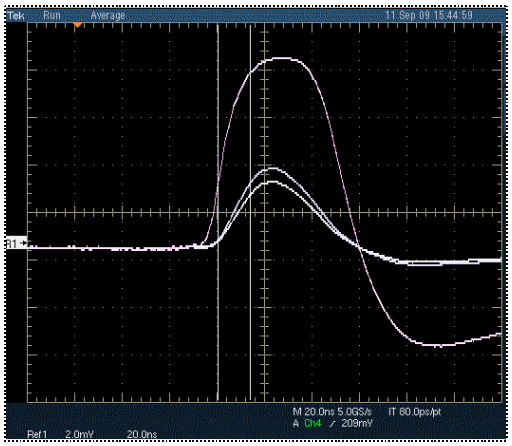

Figure 4: Shaper outputs for 1 fC, 1.25 fC and 10 fC input signals

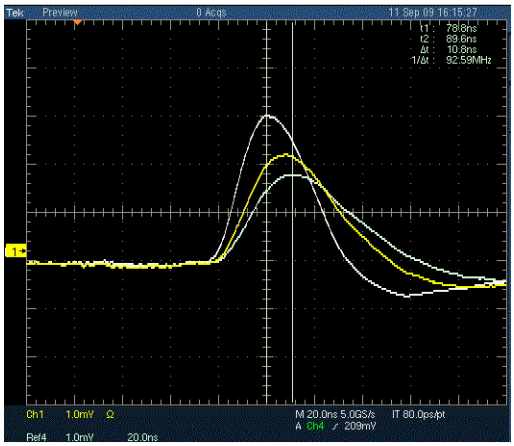

Figure 5: Shaping range of 10.8 ns using the varactor control is illustrated. One side of differential shaper signal shown with 1 fC input, 3.31 pF load.

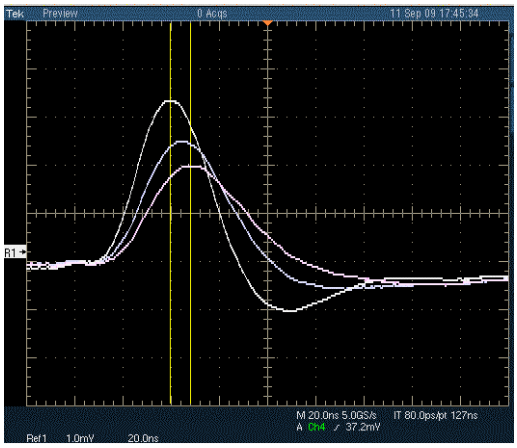

Figure 6: Shaping range of 8.4 ns using the varactor control is illustrated with much larger load than in Figure 5. Input signal is 1 fC, and load, 19 pF.

The timewalk measurement technique using a digital scope is illustrated in Figure 7. The scope trigger is the LVDS comparator signal at the lower right. This signal varies in width with noise in the shaper analogue signal. The calibration trigger signal on the upper traces is averaged ~200 times. Since it has constant width and amplitude, the average shows as a signal with lower rise time for the 1.25 fC trigger on the left. The apparently faster 10 fC trigger shown on the right indicates much less jitter in the comparator LVDS signal width and timing. The cursor indicates a timewalk of 16 ns for this amplifier setting. Note that the earlier 10 fC signal appears to the right of the later 1.25 fC signal, since we are post-triggering.

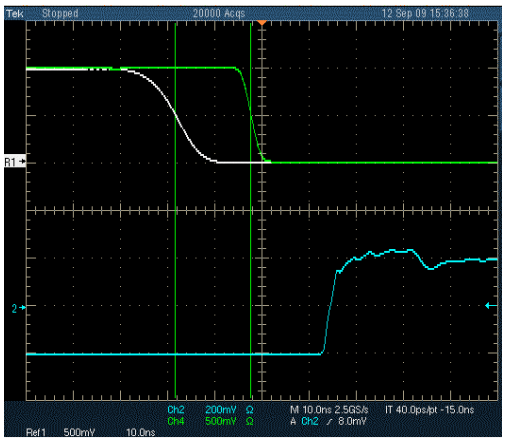

Figure 7: Timewalk of 16 ns for input signals of 1.25 fC and 10 fC

For the simple binary readout architecture the preamp and shaper circuit is characterized by varying the comparator threshold and counting the percentage of comparator firings vs. the threshold. The count rate ranges from 100% at low threshold to 0% at the highest threshold. The plot of count rate versus threshold is actually the standard Error Function where the 50% point corresponds to the mean signal amplitude and the width of the slope the Gaussian noise. This was measured for several input charges and several settings of the front transistor bias current and input capacitance. Figure 8 shows the results for a 13 pF input load at six different front transistor currents. Using the varactor, the timewalk was adjusted to 16 ns for all points. The 50% responses shown are non-linear by design in order to minimize power since a linear response is not required in this readout architecture. It is linear in the region of the planned operating threshold, 0.5 fC to 1.0 fC. The small signal gain is then the derivative of the response curve. The small signal gain is used in calculating the noise referred to preamp input and is shown in Figure 9.

The noise as referred to preamp input was measured for input loads from 3.3 pF to 17.4 pF, and front transistor bias currents from 60 μA to 180 μA. Figures 10 and 11 show the results of these tests. Load capacitance includes all strays, including the mini-board, the bond pads, and an estimate of the chip circuit and protection diodes. The noise equivalent of 640 nA sensor leakage current has been added in quadrature to the measured noise to include the effect of radiation damaged sensors. Note that the 17.4 pF curve in figure 10 has no data points below 120 μA since the VSHAPE control is out of range for lower front currents.

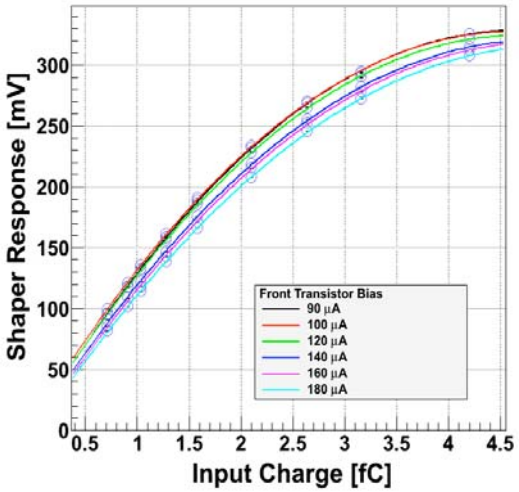

Figure 8: Response curve for 13 pF load and 16 ns timewalk

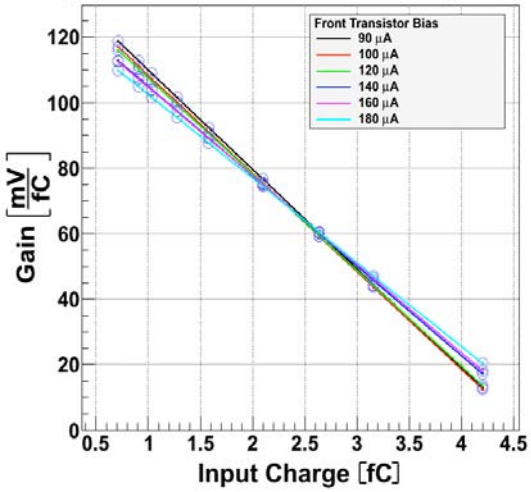

Figure 9: Small signal gain, the derivative of the response curve, such as in Figure 8, for 13 pF load and 16 ns timewalk

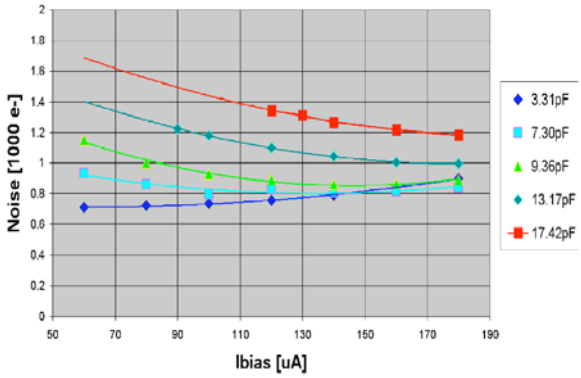

Figure 10: Noise referred to input vs. front bias current

Using results shown in Figure 11, we measure 1360 e^- at a front bias current of 102 µA for a 15 pF load. When we include the additional noise due to the expected post radiation DC gain reduction as well as the irradiated sensor leakage current, a post radiation noise level of 1500 e^- can still be achieved. Adding in the bias currents of the remainder of the analogue circuit at nominal rail voltage of 1.2 V, the total analogue power consumption is 197 µW per channel. This would be the expected power consumption for the long strip ATLAS upgraded detector. For the short strip option (5 pF load), the front bias current can be reduced to about 60 µA for minimal noise and 146 µW total power per channel. The noise, however, would not be optimal once the post radiation front transistor DC gain reduction is taken into account. This could be remedied by further optimization, namely a reduction in the size of the front transistor and an increase in the feedback resistance. The results of such a further optimization will be quantified in the near future.

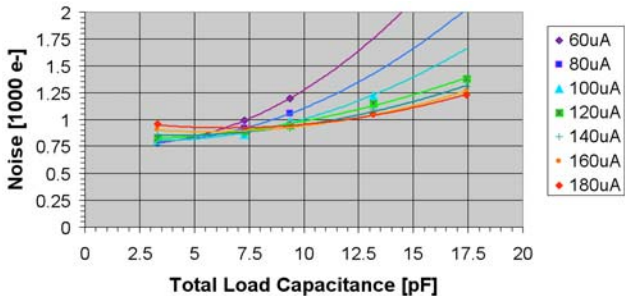

Figure 11: Noise referred to input vs. load capacitance

IV. Conclusions

This 8-channel chip demonstrates that acceptable noise values can be achieved for the silicon microstrip detectors currently envisaged for the ATLAS Upgrade Detector, especially the long strip (~10 cm) sensor version, at exceptionally low power. Additional optimization of the front transistor and feedback could further reduce noise and power for the short strip sensor version. The design and technology easily meet the required 16 ns time-walk requirement and faster performance could be easily achieved. The design allows for variable control of the front transistor bias current and the shaping time, thus allowing noise vs. power optimization for a range of sensor characteristics, in particular to accommodate changes in sensor characteristics due to ongoing radiation damage.

V. References

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