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VIDEO-TAPE NUCLEAR PHYSICS DIGITAL DATA RECORDING

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Summary:

A mass memory system for digital data, comprising a video tape recorder interfaced to a small controlling computer, is being developed by CERN for use in on-line data acquisition in elementary particle physics experiments. The storage capacity of each video-tape cartridge is about 7.10^{10} data bits, equivalent to several hundred conventional 9 track 800 bpi computer magnetic tape reels, and the system accepts a continuous data input rate of over 360,000 16-bit words/sec.

1. Introduction

In particle physics experiments at CERN, the accelerator laboratory of the European Organisation for Nuclear Research, two factors contribute to an increasing requirement for mass data storage. Continuing accelerator improvement programmes result in higher particle beam intensities, with correspondingly increased event (particle interaction) rates; while the progressive introduction of multi-wire proportional chambers in place of wire spark chambers for particle detection has allowed the proportion of events for which data acquisition is possible to be increased also.

In a typical experiment, about 200 16-bit words are generated for each event by the chamber read-out system, scalers, and ancillary electronics. The acquisition of these data in organised sequence is normally effected by the international standard data system CAMAC, which transfers them to an on-line computer at rates up to about 750 Kw/sec.

Using arrays of wire spark chamber detectors, dead times limited

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event rates to about 30 per second at most, so that data rates were comfortably within the capabilities of conventional 75 ips computer tape transports (about 110 events per second). With proportional chamber detectors, the typical event rate can exceed 1000 per second, so that video-tape techniques become appropriate for the recording of the experimental data.

In addition to meeting the data rate requirement, video-tape offers a welcome compactness of data storage. Since a conventional computer tape reel can store data for about 60,000 events, while the total number of events to be measured for one experiment is often in the 10^7 to 10^8 range, hundreds of tape reels have to be written by the on-line computer and mounted at the off-line central computing facility (a CDC 7600) for analysis. As a result, CERN has to operate a cumbersome and fast-growing library currently comprising over 45,000 reels of magnetic tape.

Exploiting the high single-track recording densities which become feasible when the limitations imposed by inter-track skew and NRZ1 recording are removed, and the good tape area utilisation afforded by the scanning head technique, a video recorder can write over 7.10^{10} bits on a 7000 ft reel of 1 in tape, so that all the data for an experiment can be stored in a small number of video-tape cartridges.

In view of these attractive features, a pilot project was initiated at CERN to develop a video-tape mass memory system for nuclear physics digital data recording. The system is first to be used in a high energy spectroscopy study at CERN's intersecting storage rings. A complementary project is designed to realise a dedicated hardware processor which will accept the recorded data at the high rates at which it can be read from video-tape and carry out data reduction prior to detailed off-line analysis.

2. Mass Memory Organisation

The video-tape recorder used in the mass memory system is a Type MMR-1 (see Fig. 1) by International Video Corporation. This is

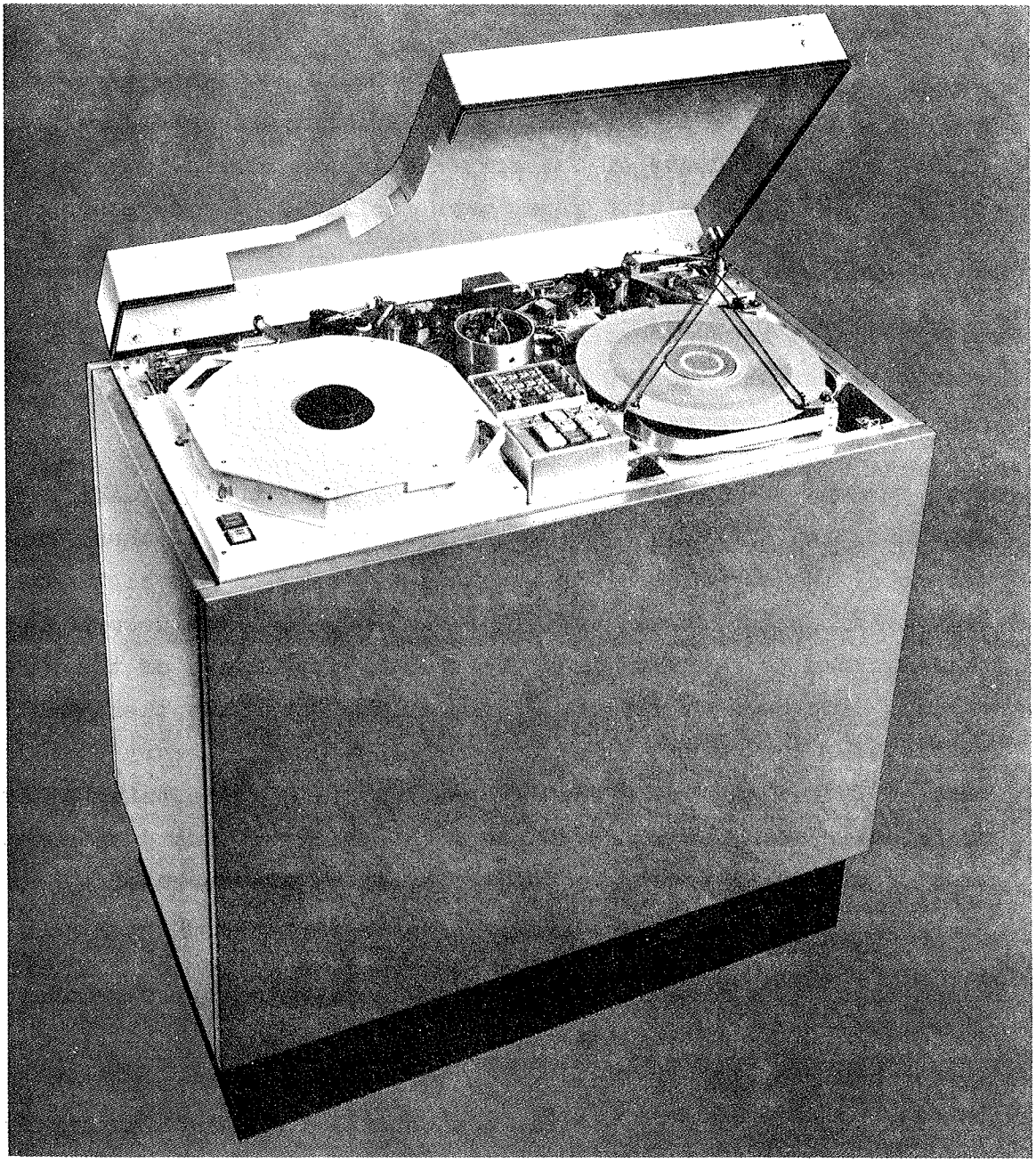

Fig. 1 IVC MMR-1 Recorder

a 1 in tape helical scan machine specifically developed for digital data recording in a computer-controlled environment. The machine has very few manual controls and is equipped with an automatic tape threading mechanism.

The MMR-1 is interfaced to a Hewlett Packard 2100A computer by a Type 7500 Controller developed at CERN, and the configuration of the main components of the system is shown in Fig. 2. The computer is equipped with paper tape facilities for development purposes - this equipment is not required in operational application - while the complete mass memory system interfaces to the external data source/destination (in the pilot project an IBM 1800 computer) through two I/O ports of the 2100A - one control channel and one direct memory access (DMA) data channel.

Nine further bi-directional I/O ports of the 2100A are used for communication with the 7500 Controller, and to one of these the second of the computer's DMA channels is assigned for high density data transmission. The Controller, which serialises/deserialises data written to and read from the various tape heads of the MMR-1, buffers data on a word basis sufficient to cope with the asynchronism of computer cycles and tape motion. The computer memory itself is used to buffer data on a scanline basis, 12K of core being assigned as a double scanline buffer. Wherever speed and timing synchronisation requirements permit, control operations are executed by software for economy and development flexibility.

The mechanical configuration of CAMAC is employed for the Controller design, which is accommodated in a single crate of 25 stations, but as the CAMAC dataway is unsuitable the backplane interconnections of this crate are non-standard. The signalling standards employed permit a Controller - Recorder separation of up to 30 m with good noise immunity, while the Computer - Controller separation is limited to 5 m. (These are normally accommodated in the same rack).

3. Recorded Data Format

When data recording is in progress, the tape is transported at a

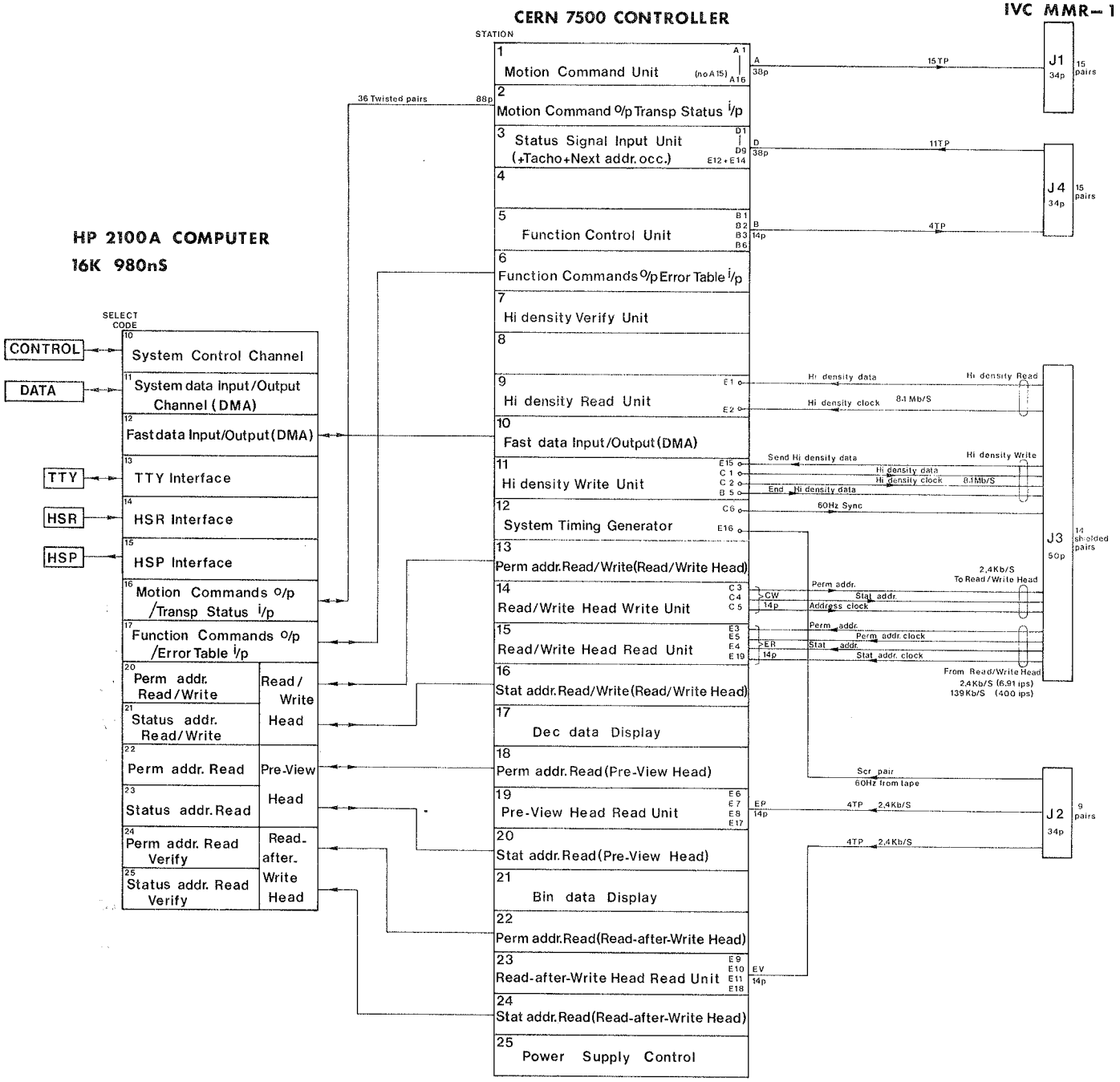

Fig. 2 Controller Organisation

speed of 6.91 ips and the head scanner rotates at 3600 rpm, both phase-locked to a 60 Hz source in the Controller. The tape format generated is shown in Fig. 3.

High density data is recorded PE in the transverse scanlines, at an angle of 4° 45' to the tape edge, at a density of 11,200 bpi. (The relative tape - head velocity is 723.18 ips). 60 Hz sync pulses are recorded RZ on the control track, and a 28 bit permanent address corresponding to each scanline is recorded NRZI in the longitudinal address track at a density of 347 bpi. Permanent address data are clocked by an additional address clock track and separated by inter-record gaps. At the opposite edge of the tape, status information is recorded at the same density as in the permanent address track but using a self-clocking PE technique.

Since the high density scanline is recorded below saturation level, and is well separated spectrally from the longitudinal data, the intersection of the preamble and postamble with the address tracks does not seriously degrade the latter. A high density data rate of 8.1 Mb/sec is used, which allows the recording of 105 Kb in that portion of each scanline (9.374 in) available for data. The address tracks data rate is 2.4 Kb/sec. Both frequencies, and also the 60 Hz control signal, are derived in the Controller timing generator from a single 16.2 MHz crystal.

4. Auxiliary Heads

During operation at the tape speed of 6.91 ips, permanent address and status tracks may be read at preview and read-after-write head stacks located in the tape path respectively 1.98 in prior to and 0.46 in after the longitudinal tracks read/write head. The preview head is used to read the current status address of a scanline before it is updated on passing the read/write head.

The head scanner carries an erase head and write level verify head in addition to the high density read/write head, each at 120 ° angular separation. Controller timing of the erase signal combined with computer control of the tape motion allows any individual

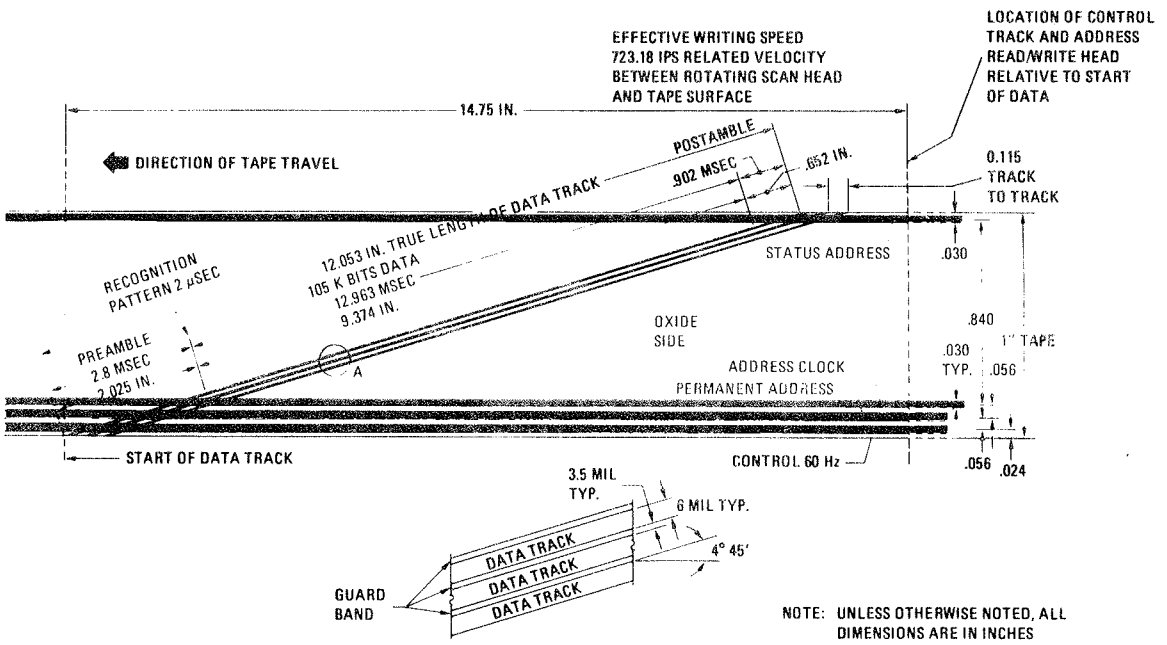

Fig. 3 Tape Format

scanline to be addressed, erased and re-written, without affecting those adjacent to it.

5. Search Mode

To permit reasonably rapid access to the mass memory, the MMR-1 tape speed can be controlled by the computer in 13 graded steps from 6.91 ips to 400 ips, either forward or reverse. Under these conditions there is of course no sync lock, writing is not possible, and the longitudinal tracks can be read only at the read/write head stack. The computer program selects an optimum motion control strategy as a function of the location (identified by its permanent address) of a desired scanline relative to the scanline currently being accessed.

Since the inter-record gap durations are a function of tape speed, the Controller address read modules use signals from the tape tachometers to identify them and decode the address words. A subdivided tachometer signal is also available to the computer, which compares actual with programmed tape velocities as part of the recorder set-up procedure.

After tape motion at search speed, a period of operation at 6.91 ips is necessary to establish capstan and head scanner phase-lock with the Controller 60 Hz clock. The time to achieve this synchronisation, which can be checked by the computer, is less than 300 mS.

6. Tape Utilisation

A tape utilisation procedure has to be established when (as in the initial application of the mass memory linked to an IBM 1800 channel), the data source supplies information at a rate lower than that required to write every scanline while the tape is advancing continuously at synchronous speed. Two procedures can be adopted.

In the first, only 1 scanline out of N is recorded per pass of the tape. In the first pass, scanlines 1, N+1, 2N+1, ... are written;

in the next pass scanlines 2, N+2, 2N+2, ... etc., and the tape is filled in a total of N passes. N is selected according to the source data rate so that most scanlines are fairly full while not too many events have to be discarded because of overflow.

The alternative procedure involves writing scanlines when the buffer becomes full, so that a variable number of scanlines is skipped. When a scanline is written, the status track is marked to indicate its non-availability on subsequent passes. The disadvantage of this scheme is the increasing delay which is experienced on later passes when several adjacent scanlines have already been written. This delay eventually makes it impractical to use a tape on further passes although a number of scanlines are still unrecorded.

7. Error Detection - Write Time

During the writing of permanent address and status tracks, the recorded data are read at the read-after-write head and a bit-equivalence comparison is made. In the case of the high density scanlines such a check is not possible, but a signal from the write level verify head generates computer interrupts should the envelope of the high density signal fall by more than 10 dB for a period exceeding 1 μS (about 8 bits). The corresponding status address is then demarked and the scanline rewritten at a later address. Since such dropouts are generally due to defective regions of tape, it is time-wasting to reverse the tape and resync to attempt a rewrite of the same scanline because the dropout will usually repeat.

8. Error Detection - Read Time

Any enabled longitudinal track Controller read module which receives between consecutive inter-record gaps a number of address bits other than 28 causes a computer interrupt and sets an error flag in the more significant word of the double precision integer transferred. The 28 recorded bits are derived from the 20 information

bits necessary to assign a unique address to each scanline by a cyclic polynomial code. Since the address data rate is relatively low, the received code is checked for zero syndrome by software.

As high density data flow via computer memory is by DMA, and at a rate approaching the maximum possible throughput of the 2100A, the generation and testing of checkbits is done by hardware in the Controller. The high density write unit generates 104,975 bits per scanline, composed of 95 blocks of 65 words of 17 bits. Each 65-word block consists of 64 data words plus an even parity checksum word, and each 17-bit word comprises 16 data or checkbits plus an even parity bit. Checkbits account for 7.3% of the useful portion of each scanline, allowing the recording of a total of 97,280 data bits per scanline, which requires 12,160 words of computer memory for a double scanline buffer.

During reading of the scanline, all parities and checksums are verified and redundant bits removed from the data. The identification numbers of blocks in which any error is detected are stored in an error address stack in the Controller high density verify unit, the contents of which are read out by the computer. The events which include data in an erroneous block are subsequently discarded.

The hardware is designed to allow the block length to be readily modified between 32 and 256 data words, to allow a satisfactory compromise between adequate error localisation and efficient potential tape utilisation to be established for a range of system error performances.

9. Conclusion

The mass memory system described features a data storage capacity two to three orders of magnitude greater than that of conventional computer tapes. This represents a compression sufficient to eliminate most of the current problems connected with magnetic tape administration and storage at a large laboratory.

In addition, the introduction of the system may eventually have a considerable impact on experimental design, since it now becomes feasible to operate an electronic detector facility with relaxed trigger conditions to generate data tapes which may subsequently be analysed off-line for the study of different reactions.

It is possible to envisage that in this way the source data from a single facility may be exploited in the various Member States of CERN by independent physics groups with differing research interests.