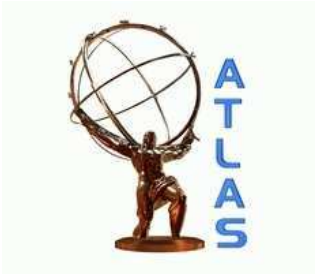

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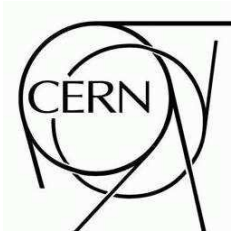

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Forward SCT Module Assembly and Quality Control at IFIC Valencia

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Abstract

This note discusses the assembly and the quality control tests of 282 forward detector modules for the ATLAS Semiconductor Tracker assembled at the Instituto de Física Corpuscular (IFIC) in Valencia. The construction and testing procedures are outlined and the laboratory equipment is briefly described. Emphasis is given on the module quality achieved in terms of mechanical and electrical stability.

1 Introduction

The ATLAS Semiconductor Tracker (SCT) together with the pixel and the transition radiation detectors will form the tracking system of the ATLAS experiment at the LHC. It consists of 20 000 silicon micro-strip sensors assembled into modules mounted on four concentric barrels and two forward detectors formed by nine disks each. The construction of the SCT involved —among other development projects and macro-assembly— the building and Quality Control (QC) of $\sim$ 4000 modules.

In particular, the assembly of the required 1976 ATLAS SCT [1] forward modules [2] plus a contingency of 20% was distributed among 13 European and one Australian institutes, divided into three clusters in order to facilitate the sharing of tasks and the flow of components. The IFIC group, as a member of the UK-V cluster, followed the complete assembly sequence and all the necessary QC tests were performed, as shown in Fig. 1, for all assembled modules. The full production was launched after a qualification period, during which the tooling and the execution of the procedures were successfully validated.

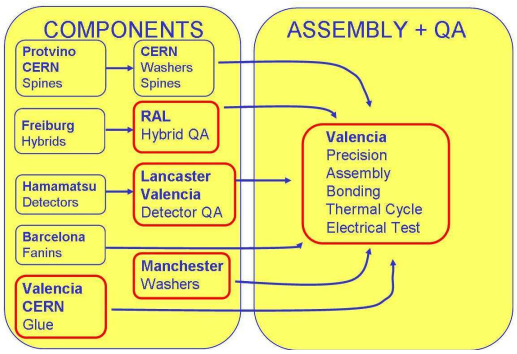


Figure 1: Flow of components for module production and list of assembly tasks and quality control tests performed in Valencia.

The IFIC-SCT group assembled and tested a total of 282 forward SCT modules; 125 outer modules and 157 long middle ones. Before the production startup, the Valencia group initially undertook the construction of 125 outer and 96 middle modules. After a re-organisation of the forward modules production, the group accepted the responsibility to assemble a surplus of 61 middle modules, which amounts to a 28% increase with respect to the initial commitment.

This note begins with a brief description of the module assembly and QC sequence in Sec. 2, followed by a report on the metrology procedure and respective measurements in Sec. 3. In Sec. 4, the front-end electronics and the electrical setup and tests are outlined, and the corresponding results are reported. Some studies performed on modules assembled in other sites are discussed in Sec. 5. An overview of the QC tests results and the conclusions are given in Secs. 6 and 7, respectively. Four appendices with the elaborate QC results for the metrology (Appendices A and B), the effect of thermocycling (Appendix C) and the electrical tests (Appendix D) are appended as supplementary material at the end of the note.

2 Module assembly and quality control overview

The forward silicon modules [2] consist of one or two pairs of single-sided p-*in*-n micro-strip sensors glued back-to-back at a 40-mrad stereo angle, as shown in Fig. 2, to provide two-dimensional track reconstruction. The 285-μm thick sensors [3, 4] have 768 AC-coupled strips implanted with a pitch of $57-94$ μm. Between the sensor pairs there is a highly thermally conductive baseboard *(spine)* [4]. The sensors are connected to the front-end electronics board *(hybrid)* [5] by means of *fan-ins*[1)] [4]. Barrel

[1)] Parts made of glass with aluminum traces, providing electrical connection channel-by-channel from the sensors to the read-out chips and mechanical connection between the hybrid and the detector part of the module. They were developed and manufactured at the Centro Nacional de Microelectrónica, IMB-CNM (CSIC), Barcelona, Spain.

modules [6] follow one common design, while for the forward ones four different types exist based on their position in the detector. At IFIC, outer and long-middle modules were built made up out of two pairs of Hamamatsu[2] silicon sensors.

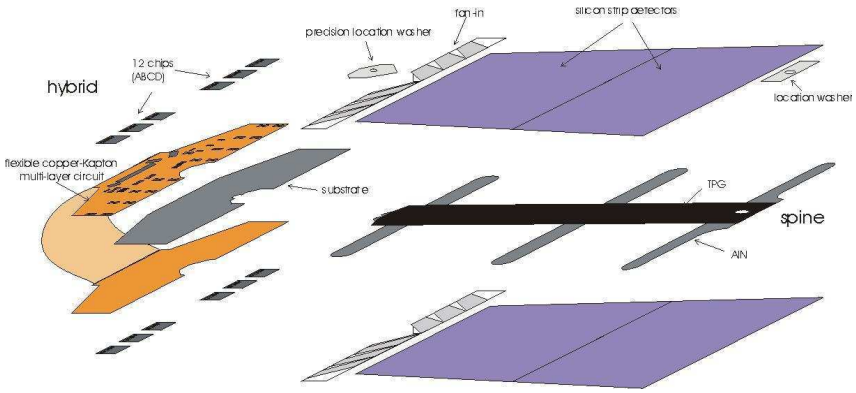


Figure 2: The module assembly scheme.

In order to carry out the module production according to the quality criteria set by the ATLAS SCT collaboration, dedicated machinery and tooling was constructed and installed in a clean room of ~ 75 m^2 at IFIC, where temperature was controlled within 0.5 °C and relative humidity within 5% (keeping it below 50%). This area was divided into two compartments: a small one (20 m^2) of class 1000 and a big room (55 m^2) of class 10 000. In the former the electrical properties of the sensors and modules were measured and the visual inspection of the components was performed, while in the latter the remaining assembly and testing tasks took place.

Besides the production-oriented infrastructure, a laser test bench has been developed aiming at various studies on silicon detectors ~~in~~cluding SCT modules. Specifically, measurements were carried out in order to detect defects on strips (e.g. oxide punch-through) [7]. Important characteristics of module performance were determined with the laser beam, such as the response dependence on interstrip position, the pulse shape reconstruction for different impact positions along the strip, the spatial resolution, etc.

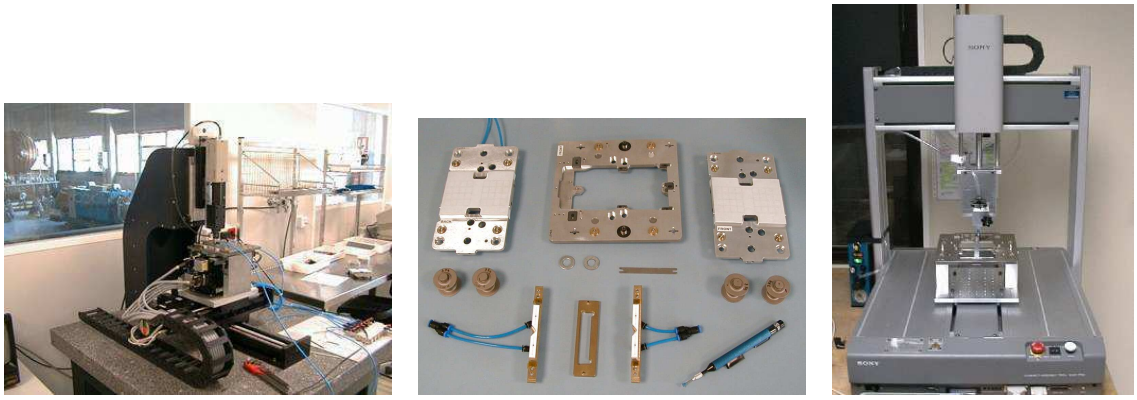
The end-cap module comprises several components [4], viz. the silicon sensors, the spine, the fan-ins, the washers and the electronics hybrid [5], assembled as shown in Fig. 2. Tests were made upon reception and during assembly to assure that the components have not been damaged during transport or in the first stages of module construction, including a first *IV* scan of the individual silicon sensors. In the following, the module assembly steps and intermediate quality checks, described in full detail in Refs. [2,8–10], are outlined and only the technical features specific to the IFIC laboratory are mentioned.

Sensor pair alignment. To achieve good tracking performance stringent requirements on the positioning of the modules are imposed. The precise alignment [9] of the detectors is achieved by employing a robot consisting of six linear stages,[3] pictured in Fig. 3a. It is equipped with an optical system for pattern recognition and stages which are commanded by the DMC-1500 controller[4] through a PC using a program running under LabVIEW developed at the University of Manchester [11]. The detectors and the fan-ins are kept in place through vacuum chucks on the assembly station and their positioning is achieved through four fiducial marks on the turn plate, shown at the centre of Fig. 3b. After the alignment, the detectors, the fan-ins and the hybrid are mounted on the turn plate, by means of the transfer plates (Fig. 3b, top left and right), and they are then transferred to the glue dispenser (Fig. 3c).

[2] Hamamatsu Photonics Co. Ltd., 1126-1 Ichino-cho, Hamamatsu, Shizuoka 431-3196, Japan.

[3] Nappless-Coombe Ltd.

[4] Galil Motion Control, Inc.



(a) Alignment and assembly stand. (b) Assembly tooling. (c) Dispenser machine.

Figure 3: Alignment, assembly and gluing apparatuses for module building.

Glue dispensing. The glue dispensing device, shown in Fig. 3c, works on a Sony Cast Pro system with a dispensing system attached and controlled by a PC using the LUNA language. The thermally conductive glue applied is a two-component, room-temperature curing epoxy labelled Araldite 2011[5)] [4]. The mixture makes an adhesive of adequate strength and high thermal conductivity.

Detector assembly and glue curing. After applying the glue, each transfer plate consecutively is inserted in and fastened to the turn plate at the same place where it was when the aligned detectors were picked up from the assembly station. The module components are then left to cure in a four-pillar stand for several hours.

Detector *IV* scan and alignment check. The measurement of the electrical properties of sensors and the visual inspection of the components [10] takes place in a probe station comprising a microscope and a position controller installed in a dark box, as shown in Fig. 4a. The electrical properties of the silicon sensors were examined using the home-designed program *Probe* [12]. It is a C++ program using the graphical user interface package *Qt*, running under Linux, which controls the measurement instruments[6)] via an IEEE488 interface.

Hybrid assembly with fan-ins and washers. The hybrid [5] is lowered onto its correct position on the turn plate by inserting small tapered pins through the hybrid holes. Conductive glue is applied underneath the HV tongues to ensure connection to the detector back-planes. These electrical connections and the absence of short circuits is checked before going to the next step. The fan-ins [4] are added later using the fan-ins chucks, shown in Fig. 3b (bottom), and the glue dispensing machine. The fan-ins chucks are positioned using location pins of the proper side of the turn plate and they are tightened with screws. The procedure is completed with the fitting of the location washers [4] on the module.

***XY* and *Z* survey.** The setup and measuring procedure [13] are described in detail in Sec. 3. After the first metrology survey, the HV line is glued and left to cure.

Wire-bonding. All the production modules are wire-bonded by the fully automatic bonder machine[7)] pictured in Fig. 4b. The laboratory is also equipped with a semi-automatic bonder[8)] used during the pre-qualification period. A pull-tester, [9)] shown in Fig. 4c, was also used during the qualification period for the validation of the bonding parameters.

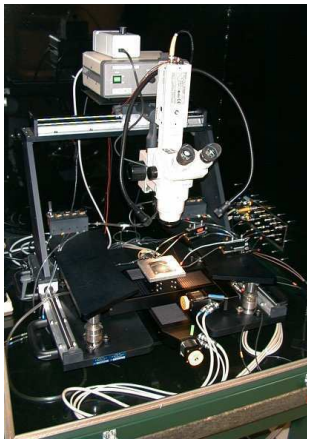
[5)] Supplied by Ciba-Geigy.

[6)] Keithley 237 HV source measure unit; Keithley 236 source measure unit; Wayne Kerr 6425 Precision Component Analyzer; Pickering 12×4 switching matrix; and Keithley 2700 multimeter.

[7)] K&S 8090.

[8)] K&S 1470.

[9)] Dage 3000



(a) Probe station.

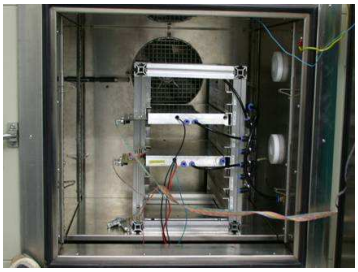
(b) Automatic bonding device.

(c) Pull-testing machine.

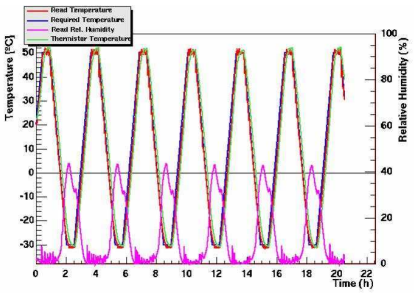
Figure 4: Devices for module testing and wire-bonding.

Thermal cycling. When the assembly is completed, the modules undergo a thermal cycling in order to verify that temperature variations do not compromise the geometrical properties of the module [14]. This task is performed in a climate chamber,[10] displayed in Fig. 5a, which operates at a temperature ranging from -30 °C to $+50$ °C. An aluminium rack positioned inside the chamber, shown in Fig. 5b, allows simultaneous thermal cycling of up to six modules. The thermistors are readout by a multimeter[11] and the system is controlled, monitored and read out by a PC. The thermistors temperature was recorded every 10 s in a data file and plotted on-line (cf. Fig. 5c). During this process the thermistors temperature varies from -30 °C to $+35$ °C for a total of ten cycles lasting about 3.5 h each.

(a) Thermocycling setup.



(b) Interior of climate chamber.



(c) Thermal cycle.

Figure 5: The thermal cycling setup and a typical monitoring plot. The oven and thermistor temperatures are plotted, together with the relative humidity. A complete process covers ten cycles.

The quality assurance plan for the forward modules foresees the following QC tests [10] for the completed (glued and bonded) module:

- final XY and Z metrology [13];
- long-term leakage current and electrical stability [15];
- electrical characterisation [15];
- IV curve of the completed module [15];
- visual inspection.

[10] Dycometal CM 40/125A.
[11] Keithley 2700.

In the following two sections, we concentrate on the procedures and outcome of the most important quality control issues: the dimensions in Sec. 3 and the electrical behaviour in Sec. 4 of the produced modules.

3 Metrology

The precision needed during construction is determined by physics requirements. For the detector to be hermetic in tracks with $p_T > 1\ GeV$, a tolerance of $\sim 100\ \mu m$ in the $r\phi$ direction and $\sim 500\ \mu m$ in radius is specified [14]. Taking this into consideration, the effective module dimensions specifications are derived [13].

3.1 Setup and procedures

The metrology process is divided into two main tasks (see Ref. [13] for a detailed description); the *XY* metrology,[12] in which relative in-plane alignment between silicon sensors and the mounting hole and slot[13] are measured, and the *Z*-profile of the detectors relative to the mounting surface. The position of sensors in the *xy*-plane is defined by a number of fiducial marks printed on its surface. The hole and mounting slot have a sharp and well-defined edge which is used for determining its position.

The *XY* metrology parameters, which refer to the relative positions of the four detectors in the *xy*-plane with respect to each other, are the following:

- $midxf$, $midyf$, which represent the front-to-back detector pair alignment in *x* and *y*;
- $sepf$ and $sepb$, which represent the separation between the detectors of each side;
- *stereo* angle, which denotes the deviation from the nominal stereo angle (40 mrad) between the two detector pairs;
- $a1$, $a2$, $a3$, and $a4$, which are the four individual detector angles relative to their nominal position; and
- *mhx*, *mhy*, *msx*, *msy*, are the hole and slot positions in *x* and *y*, respectively.

The *Z* metrology,[14] on the other hand, is performed by measuring the *Z* position of a grid of 25 points distributed over the surface of each of the four detectors, as shown in Fig. 6. From these points, the average (*zave*), the maximum (*zmax*), the minimum (*zmin*) and the RMS (*zrms*) values are calculated for the front and back side of the module. These parameters are then compared with the specified values [13].

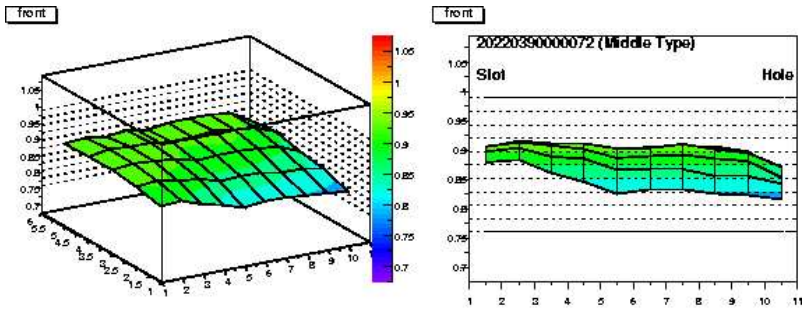


Figure 6: Typical *Z* profile of the front side of a middle module. The back-side profile is obtained likewise.

[12] The *x*-axis is defined along the strips and the *y*-axis is perpendicular to them and on the sensor plane.

[13] As hole is denoted the mounting point between the hybrid and the sensors, whereas the slot is located in the module endpoint.

[14] The *z*-axis is defined vertical to the module.

A custom-made[15)] laser interferometry metrology system, shown in Fig. 7 was employed for the mechanical survey of the module, providing an accuracy of 1 μm. It is equipped with two cameras to achieve a better accuracy in the determination of the *xy* parameters. Thus it avoids errors due to intermediate manipulation steps when turning the module upside down, as is needed with single camera systems. During the survey, the module is mounted in a frame allowing the measurement of the *xy* and *z* positions of the detectors of both sides with respect to the same reference points.

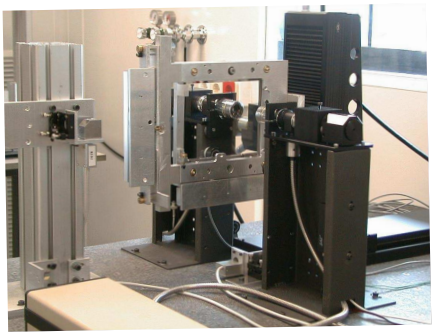


Figure 7: The metrology setup: the two cameras, the mechanical stages and the module-mounting frame are visible.

3.2 Measurements

As mentioned before, the module dimensions were measured twice: just after gluing the components together and before wire-bonding, and once more after the thermal cycling. The overall final-measurement results for all 13 *XY* parameters are shown in Fig. 8. The majority of the modules are well within the specifications, apart from some cases where parameter *midyf* exceeds the allowed limits (cf. also Fig. 26, plots in the second row, in Appendix B). These cases stand for the majority of the modules characterised as *Pass* (cf. Sec. 6.3 for the module quality classification). Detailed results for each *XY* parameter and for each module are given in Figs. 25, 26, 27 and 28 in Appendix B.

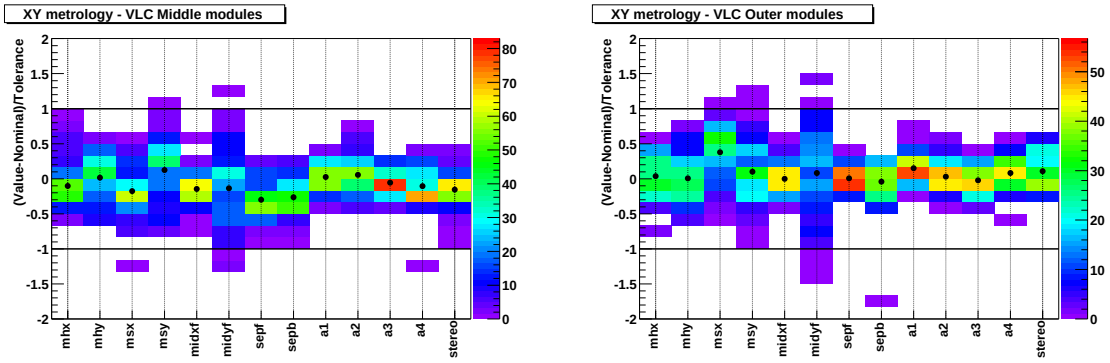


Figure 8: *XY*-parameters distributions for middle (left) and outer (right) modules.

The thermal cycling did not affect the *XY* metrology parameters, whereas, in some cases, it altered the *Z* profile. Parameters *zave*, *zmin* and *zmax* for both sides ~~in~~ particular *zminb* (cf. Fig. 23, bottom row)~~,~~ decreased after the thermal treatment in several modules, namely they appeared slightly bent in the centre. However, this effect, did not have any impact whatsoever on the production yield. The comparison of the module geometry before and after the thermal cycling is presented in Fig. 29 for *XY* and in Fig. 30 for the *Z* parameters in Appendix C. In Figs. 23 and 24 in Appendix A, the analytical results of *Z* metrology are presented.

[15)] AIDO-IFIC.

4 Electrical performance

The readout of the SCT modules is based on 12 ABCD3TA [16] ASICs mounted on a copper/kapton hybrid [5]. The ABCD3TA chip features a 128-channel analog front end consisting of amplifiers and comparators and a digital readout circuit operating at a frequency of 40.08 MHz. It utilises the binary scheme, where the signals from the silicon detector are amplified, compared to a threshold and only the result of the comparison enters the input register and a 132-cell deep pipeline, awaiting a level-1 trigger accept signal. It implements a redundancy mechanism that redirects the output and the control signals, so that a failing chip can be bypassed. To reduce the channel-to-channel threshold variation, in particular after irradiation, the ABCD3TA features an individual threshold correction in each channel with a 4-bit digital-to-analog converter *(TrimDAC)* with four selectable ranges. The clock and command signals as well as the data in binary form are normally transferred from and to the off-detector electronics through optical links [17], however during the production electrical tests, the ASICs were read out electrically using a pseudo-optical scheme. Two streams of data are read out, one for each module side (768 channels).

In this section the electrical specifications and the respective quality control procedures are outlined. Among the various functionality tests of the readout part of the module, only the more crucial ones such as the gain and the noise measurements are elaborated. Some exceptional cases are also discussed in detail. A complete description of the electronics test procedure is available in Ref. [15].

4.1 Specifications and setup

The LHC operating conditions demand challenging electrical performance specifications for the SCT modules and the limitations mainly concern the accepted noise occupancy level, the tracking efficiency, the timing and the power consumption. The Equivalent Noise Charge (ENC) is specified [18] to be less than 1500 electrons before irradiation. As far as the tracking performance is concerned, a starting requirement is a low number of dead readout channels, specified to be less than 16 for each module to assure at least 99% of working channels. Furthermore no more than eight consecutive faulty channels are accepted in a module.

A standard DAQ system has been developed within the ATLAS SCT collaboration aiming at verifying the hybrid and detector functionality after the module assembly and at demonstrating the module performance with respect to the required electrical specifications. During the electrical tests the modules are mounted in a light-tight aluminum box which supports the modules at the two washers. The test box includes a cooling channel connected to a liquid coolant system.[16)] The operating temperature is monitored by a thermistor mounted on the hybrid. The box also provides a connector for dry air circulation. Subsequently, the module test box is placed inside the custom-made, light-proof box, shown in Fig. 9 (left), and it is electrically connected to the readout system and VME crate. Up to six modules can be tested simultaneously with this configuration. The grounding and shielding scheme of the setup is of crucial importance, therefore a careful optimisation is necessary.

In all the measurements performed, the ASICs are powered with three standard SCT low-voltage power supplies, SCTLV, and read out electrically via a system, comprising one SLOG, one MUSTARD and one AERO board, installed in two VME crates as pictured in Fig. 9 (right). Two SCTHV high voltage units provided detector bias to the modules. A second complete setup including the respective readout system was also built, to serve as a backup in the event of failure of the first one. A detailed description of the SCT readout system is given in Refs. [2, 15].

The software package SCTDAQ [19] has been implemented for testing both the bare hybrids and the modules using VME units. It consists of a C++ dynamically linked library and a set of ROOT [20]

[16)] Huber chiller with antifreeze as a coolant.

Figure 9: Electrical tests setup: the light-proof box (left) and the readout boards installed in the VME crate (right).

macros which analyse the raw data obtained in each test and stores the results in a database [21].

4.2 Testing sequence

To determine the front-end parameters of the modules, an internal calibration circuit that simulates an input charge in the range $0.5 - 10$ fC is implemented in the ASICs. By injecting various known charges and performing threshold scans, the analogue properties of each channel can be determined, such as the gain, the offset and the noise. A complementary error function is fitted to each threshold scan to determine the point of 50% efficiency (vt_{50}) and the output noise for each channel. A multi-parameter fit to a set of vt_{50} points is used to obtain the response curve from which gain and offset for each channel are derived. The input noise is thus calculated by dividing the output noise measured at 2 fC over the calculated gain. The testing sequence followed in Valencia is the following:

Long-term test: This is a burn-in test, during which the ASICs are powered, clocked and triggered for 24 hours while the module bias voltage is kept at 150 V and its thermistor temperature is ~ 10 °C. The bias voltage, chip currents, hybrid temperature, the leakage current and the noise occupancy are recorded every 15 min. Moreover, every two hours a so-called *confirmation*[17] test is performed to verify the correct functionality of the module.

Characterisation: A full electrical characterisation of the module is carried out at a hybrid operating temperature of 10 ± 5 °C and a bias voltage of 150 V, consisting of the following tasks:

a) *Digital tests:* checks of the redundancy links, the chip by-pass functionality and the 128-cell pipeline circuit, executed in order to identify chip or hybrid damage.

b) *Strobe delay:* an optimisation of the delay between the calibration signal and the clock on a chip-to-chip basis.

c) *Three-point gain:* a first evaluation of the gain for three different values of injection charge.

d) *Trimming:* adjustment of the TrimDAC for each channel to allow for an improved matching of the comparators thresholds.

e) *Response Curve:* final measurement of the gain for ten values of injected charge ranging from 0.5 fC to 8 fC.

f) *Noise occupancy:* a threshold scan without any charge injection, performed to yield a direct measurement of the noise occupancy at 1 fC. The adjusted discriminator offset is applied to ensure a uniform measurement across the channels.

[17] It includes digital tests, a strobe delay setting and a three-point gain.

g) *Time walk:* a strobe-delay scan is performed to assess the sensitivity of the pulse timing to the injected charge.

Final *IV* scan: A final measurement of the detector leakage current as a function of the bias voltage (*IV* curve) is performed at ~ 20 °C to assure that the current drawn by the whole module is low enough for the safe operation of the detector. The current values at 150 V and 350 V are recorded and compared with those of previous *IV* curve measurements before and after the module sub-assembly.

The characterisation sequence is also applied as a reception test of the unassembled hybrids.

4.3 Electrical results

Collective results, as far as noise is concerned, are presented in Figs. 10 and 11, for middle and outer modules separately. Middle modules, being shorter than the outer ones,[18] exhibit a lower noise level. The noise occupancy distributions lie well below the specification of 5×10^{-4}. It should be stressed that the acquired noise measurements largely depend on the setup optimisation level (grounding, shielding), therefore these values represent an upper limit of the module noise. The noise also depends on the hybrid temperature increasing by ~ 6 electrons per degree Celsius. Since under standard conditions at the LHC the modules will operate with a thermistor temperature near -7 °C, a lower noise level than the one obtained during quality control tests is expected during running.

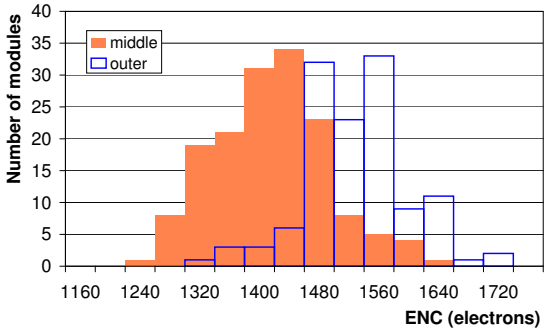


Figure 10: Average equivalent noise charge distributions for middle and outer modules.

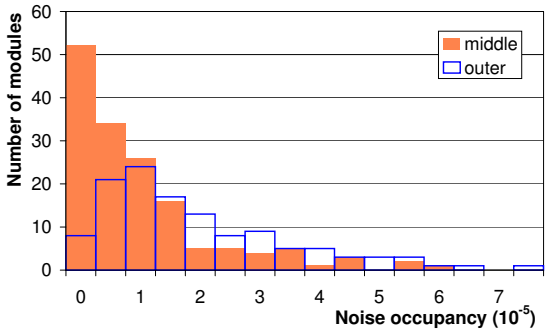


Figure 11: Average noise occupancy distributions at 1 fC for middle and outer modules.

The distributions of the number of defective channels per unassembled hybrid and per module are shown in Fig. 12. These include all types of defects, such as dead, stuck, noisy channels, channels that have not been wire-bonded to the strips and channels that cannot be trimmed. These channels are masked during normal operation and are practically *lost*. Also included in the distributions are less critical faults such as low or high gain (or offset) with respect to the chip average, which are still operational.

In Fig. 13 the number of faulty channels induced during assembly is presented, i.e. those not present during the hybrid QC. These are mostly due to sensor defects, such as oxide pinholes, strip metal shorts or opens (sometimes caused by scratches) and to a lesser extend to partly-bonded or un-bonded channels. The negative values represent trimmable channels tagged as untrimmable during hybrid testing. The detailed breakdown of hybrid/module number of defective channels is presented in Figs. 31 and 32 in Appendix D.

In Fig. 14 the average gain per module is shown for all qualified forward modules. The average gain value is about 57 mV/fC with an RMS of 2.3 mV/fC at a discriminator threshold of 2 fC and it is of the same level as the one obtained from system tests.

[18] In middle modules the total strip length is 117.7 mm, whereas in outer modules it is 121.2 mm.

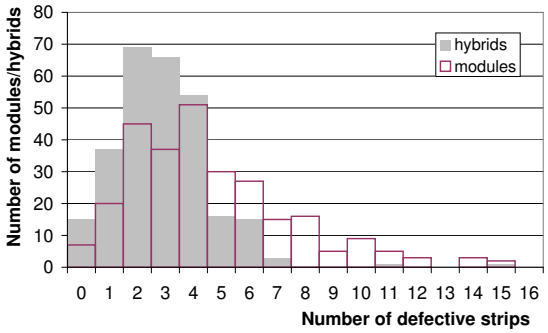


Figure 12: Number of defective strips distribution per hybrid and per module.

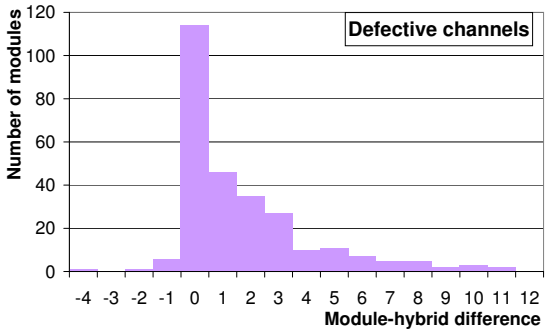


Figure 13: Distribution of number of additional defective strips introduced during assembly.

The distributions of leakage current for a bias voltage of 150 V and 350 V are shown in Fig. 15. These results, taken at a hybrid temperature of $\sim$20 °C, represent the final current measurements during module assembly and they do not include modules rejected because of high current. The values spread partly reflects the strong dependence of the leakage current on temperature, roughly doubling every 7 °C. The last 11 modules were assembled with sensors demonstrating relatively high leakage current that were designated for use during the (pre-)qualification phase. After training at progressively increasing high voltage for long periods of time (1–2 days), all of these modules, apart from one (#160), were successfully recovered delivering an acceptable *IV* curve.

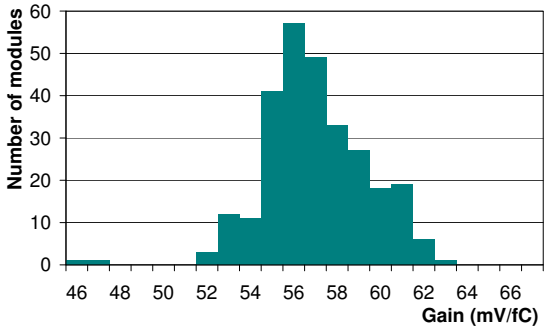


Figure 14: Average per module gain distribution for a discriminator threshold of 2 fC.

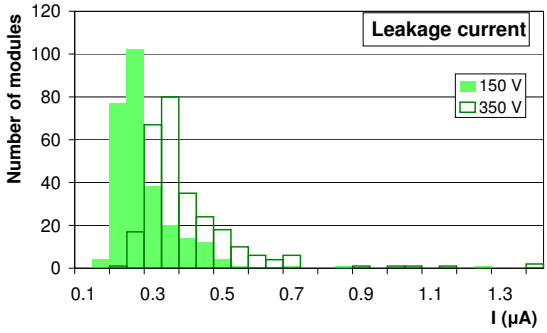


Figure 15: Leakage current distributions at 20 °C for a bias voltage of 150 V and 350 V.

4.4 Defective chips

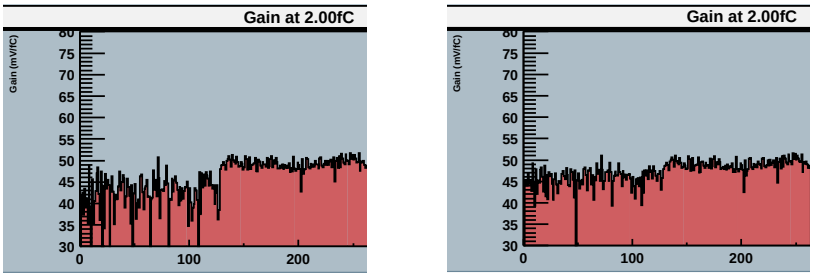
Some exceptional ASIC cases and the remedies applied are discussed in the following subsections. Apart from them, no other serious condition, as far as the module front-end electronics is concerned, was encountered and none of the modules was rejected because of poor electrical performance.

4.4.1 Large gain spread

A particularly low and Large Gain Spread (LGS) was observed in the M0 chip of Valencia module #67[19)] as shown in Fig. 16(a). Such occurrences, which are due to the sensitivity of individual chips to small

[19)] The modules assembled in Valencia are numbered as 2022039000XXXX, where XXXX ranges from #0004 to #0160 for the middle modules and #1001 to #1125 for the outer ones. Modules #1 to #3 were assembled during the pre-qualification period and they are not considered as production modules.

variations of the operating conditions, are known and they are treated by lowering the shaper current, I_{sh} [22]. The LGS chip M0 is recovered when the shaper current is lowered from the nominal value of $I_{sh} = 20\ \mu$A (cf. Fig. 16a) to $I_{sh} = 15\ \mu$A (cf. Fig. 16b).



(a) $I_{sh} = 20\ \mu$A (b) $I_{sh} = 15\ \mu$A

Figure 16: Gain vs. channel number for the front side (only the first two ASICs are shown) of Valencia module #67; M0 chip shows LGS effects.

4.4.2 Reworked bonds on chips

During the hybrid acceptance test, in one hybrid (20220554115113) no response was received by five ASICs, namely S1–E5. Visual inspection showed that contamination on pads of chip S1 caused three bond-wires to fail (see Fig. 17). The hybrid was returned to Rutherford Appleton Laboratory, reworked and passed successfully a warm characterisation test. After being returned to Valencia, it was assembled into module #1086 and tested uneventfully.

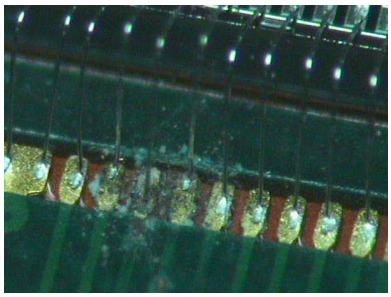


Figure 17: Pad contamination in chip S1 of module #1086, affecting the bonds quality.

In two other occasions, namely in modules #76 and #1078, bonds to detector ground in ASICs (M0 and E5, respectively) were missing and were recovered during wire bonding of the module.

4.4.3 Reworked high voltage contact

In one occasion, namely module #88, the HV line was open-circuited, causing all analog tests to fail in a consistent albeit unexpected manner. The problem was readily confirmed using a multimeter and the electrical contact between the HV finger of the hybrid and the sensor was restored.

5 Bonding of CiS modules

Apart from the standard modules assembly and testing, some additional studies were performed in Valencia, aiming to address bonding issues that arose in other assembly sites. To this effect, 11 middle

modules assembled at the Max Planck Institute (MPI) of Munich and one outer module from the University of Melbourne were wire-bonded and tested. These modules were built with sensors manufactured by CiS,[20] which differ from Hamamatsu sensors with respect to leakage current and defective strips [2].

During wire-bonding, some parameters had to be adjusted and some reworking was necessary in order to achieve rigid wire connections. For instance, one of the modules (L084) had poor metallisation on fan-in and efficient bonding was only possible by reducing the bond speed. In other cases, glue had to be injected in the central fan-in region. Furthermore, the bond rigidity was examined by performing a pull test on a CiS dummy module, i.e. without ASICs, which had been bonded at IFIC. The average pull strength necessary to remove the wire was found to be 13.8 g, i.e. well above the lower limit of 6 g, confirming the bonding firmness.

After bonding, five MPI modules and the Melbourne one were submitted to a specific test aiming at identifying strips with oxide punch-through induced during module wire-bonding. In these strips, the damaged bond-pads result in a short between the p-implant and the aluminum pad, suspending thus the AC-coupling between the strips and the readout electronics.

The identification of punch-through strips is carried out by applying the following procedure: the detectors are biased through the hybrid at 1 V in a thermistor temperature of $\sim 20\ ^{\circ}\mathrm{C}$; they are exposed to light so that a leakage current of 10 mA is acquired; and a three-point gain test is finally performed. A punch-through strip appears subsequently in the SCTDAQ results as a low-gain channel, however the outcome highly depends on the testing conditions.

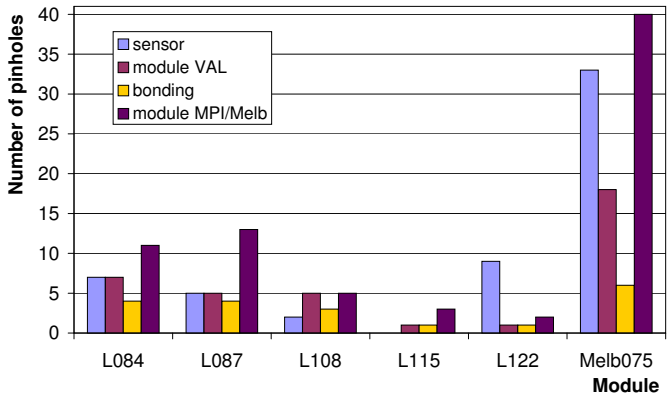


Figure 18: The number of pinholes (punch-through strips) per module observed in various measurements.

The pinhole results per module are summarised in Fig. 18 for each measurement performed: obtained during sensor QA ('sensor'), observed in Valencia ('module VAL'), induced by bonding ('bonding') and finally detected at the assembly site ('module MPI/Melb'). Due to the different setup, testing procedure and conditions, the number of pinholes detected varies between different sites. For instance, some pinholes detected in sensors were not observed in Valencia after bonding, but they were subsequently found at MPI or Melbourne. The same results were acquired at IFIC for the Melbourne module, when the test was repeated with an increased current value of 20 mA, i.e. with more light. The number of strips with punch-through induced by bonding (3.2 on average) is compatible with the respective induced in other CiS assembling sites (e.g. MPI) and seems to be correlated with the number of intrinsic pinholes present in the sensor.

[20] CiS Institut für Mikrosensorik gGmbH, Konrad-Zuse-Straße 14, D-99099 Erfurt, Germany.

6 Overall results

A total of 125 outer production modules and 157 long middle ones have been successfully built and tested in Valencia, not taking into account the various modules manufactured during the site pre-qualification period. The detailed results of the quality control tests for all these modules have been uploaded to the SCT production database [21].[21)]

The module production took place from September 2003 till June 2005 at a rate of five or eight modules per week as shown in Fig. 19. For the long middle modules only one set of assembly jigs produced mechanically stable modules, therefore only one module per day was constructed, i.e. five modules per week. The outer modules, on the other hand, were manufactured with two sets of jigs, allowing the assembly of two modules per day. Nevertheless, the time-consuming mechanical survey limited the rate to eight modules per week. The production started with the building of the middle modules, continued with those of the outer type, and finished with the extra middle ones. Before switching to another type of modules, some dummy modules were built to insure the correct configuration of the assembly and testing setups. The low rate periods of correspond mostly to vacations or to lack of hybrids (just after production startup). The few cases of device failure (wire-bonding machine, metrology stand) were dealt with successfully and did not affect the production rate.

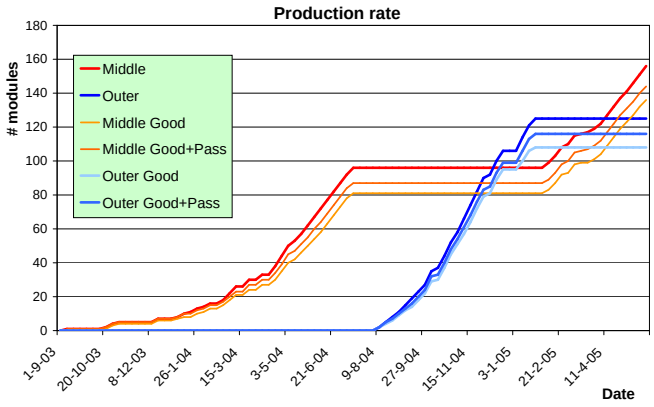


Figure 19: Accumulated number of produced modules as a function of time.

6.1 Geometry

The geometrical parameters of the produced modules are summarised in Table 1 for the XY parameters and in Fig. 20 for the Z profile. In general, the XY metrology results are clearly well within the mechanical tolerances, and only $midyf$ shown a wider distribution, as discussed in Sec. 3.2. The Z profile of the modules, on the other hand, deviates from the specified dimensions only in a handful of cases, in which however the module is still usable, as shown in the module classification that follows.

6.2 Electronics

A resume of the production performance of the Valencia modules in terms of readout is provided in Table 2. The electrical properties acquired are compatible with the ones collectively achieved by all forward module assembly sites [23]. On average, two channels per module are lost, i.e. unusable, representing 0.1% of the total. The noise occupancy was also kept well below the specified value throughout the module production.

[21)] Available in the web site: `http://ific.uv.es/sct/modules/`

Table 1: Summary of XY parameters expressed as (value-nominal)/tolerance for the IFIC modules.

Parameter	Mean	RMS	Parameter	Mean	RMS	Parameter	Mean	RMS
$a1$	0.08	0.17	mhx	-0.03	0.26	$midxf$	-0.08	0.17
$a2$	0.05	0.19	mhy	0.01	0.29	$midyf$	-0.03	0.51
$a3$	-0.04	0.15	msx	0.07	0.40	$sepf$	-0.16	0.23
$a4$	-0.02	0.20	msy	0.11	0.36	$sepb$	-0.16	0.22
$stereo$	-0.04	0.24						

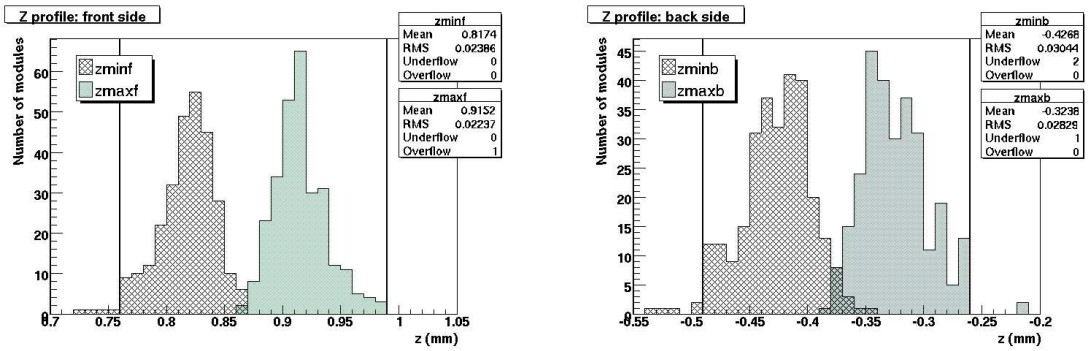


Figure 20: Distributions of minimum-z and maximum-z for the front (left) and back (right) sides. The black vertical lines designate the specified tolerances. The underflows and overflows correspond to rejected modules.

6.3 Final yield

The last step in the module assembly is the final evaluation, in which the outcome of all QC tests is taken into account. The modules are classified as:

Good: if all mechanical and electrical parameters are within the specifications.

Pass: if the metrology measurements are within 15% tolerance and a smooth IV-curve, not exceeding the current limit of 80 μA is obtained up to a minimum breakdown voltage of 350 V.

Hold: if electrical specifications are not met but at least a smooth IV curve is obtained up to 350 V and all chips are responding. It may be usable if reworked.

Fail: if the module does not match any of the above categories and cannot be reworked.

The evolution of the yield, defined over the total number of built modules, is drawn in Fig. 21 for the modules belonging in the *Good* and in the *Good+Pass* category. It is clear from this graph that although the production of both middle and outer modules started with a rather low yield, as experience was accumulated, the yield increased.

The classification of the modules produced in Valencia according to the aforementioned quality scheme is summarised in Table 3. The yield of the extra middle production is indeed significantly better that the initial one; 91.8% vs. 84.4% for the *Good* category as observed in Fig. 21.

Only four modules out of the 282 (1.4%) fall into the *Fail* category, i.e. they are not suitable for operation within the ATLAS detector. These are the following modules:

#24 Middle module in which a fan-in set of the wrong type was glued.

#27 Middle module with a broken sensor, shown in Fig. 22.

#100 Middle module with damaged wire bonds and one chip (S11) dead after an accident during manipulation.

#1006 Outer module with a fractured sensor.

Table 2: Electrical properties of Valencia modules.

	Module type	Mean	RMS
ENC (e^-)	Middle	1436	76
	Outer	1547	68
Noise occupancy	Middle	1.3×10^{-5}	1.5×10^{-5}
	Outer	2.3×10^{-5}	2.2×10^{-5}
Faulty channels	All	4.7	3.3
Lost channels	All	1.8	2.3
I_{leak} at 150 V	All	0.32	0.19
I_{leak} at 350 V	All	0.45	0.31

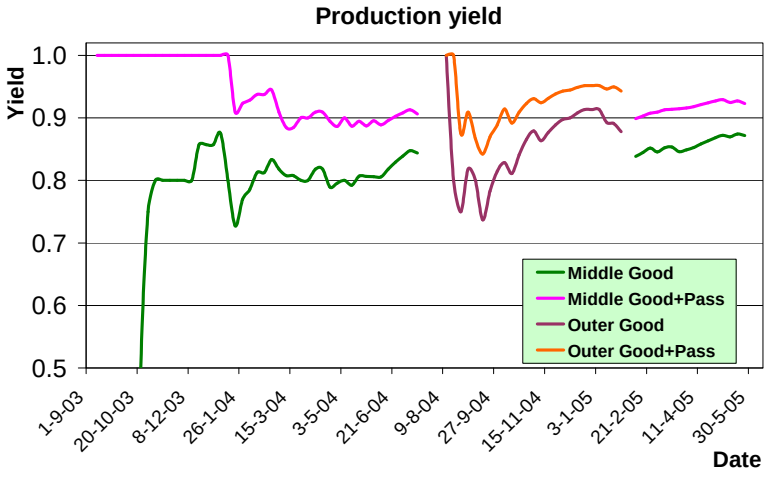


Figure 21: The production yield as evolves with time (in weeks).

The 15 modules belonging to the *Hold* class, i.e. those which may be repaired, amount to 5.3% of the total number of assembled modules. These cases were due to one or the combination of some of the following reasons:

Metrology. Seven occurrences of failure in the Z-profle and three in the XY (two with $midyf$ and one with $a4$ out-of-spec).

Scratches. Two cases in sensors, two in fan-ins and one in spine ceramic. This is mostly due to accidents while handling the components or the assembled modules. In some cases the wire bonds were also affected resulting in failed electrical tests (many unbonded or low-gain channels).

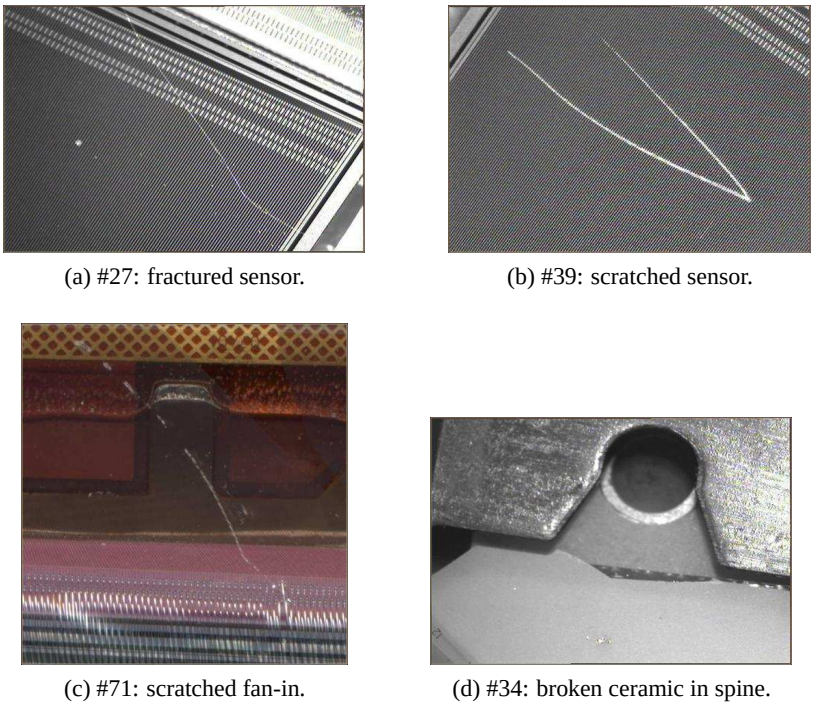
Fractures. Two cases of broken spines in the ceramic part near the hole, which is very sensitive.

Leakage current. Three cases occurred; the one was due to oil being spilled on the module while in the electrical tests box through the dry air supply. The tubes were replaced and the setup was thoroughly cleaned before resuming the tests.

The majority of the problematic modules (*Fail* or *Hold*) was due either to manipulation accidents or to the mechanical parameters not conforming to the stringent specifications set by the collaboration.

Table 3: Final yield of the Valencia modules.

Type	Good	Good+Pass	Hold	Fail	Total
Outer	109 (87.2%)	118 (95.4%)	6 (4.8%)	1 (0.8%)	125
Middle allocated	81 (84.4%)	87 (90.6%)	7 (7.3%)	2 (2.1%)	96
Middle extra	56 (91.8%)	58 (95.1%)	2 (3.3%)	1 (1.6%)	61
Middle total	137 (87.3%)	145 (92.4%)	9 (5.7%)	3 (1.9%)	157
All	246 (87.2%)	263 (93.3%)	15 (5.3%)	4 (1.4%)	282



(a) #27: fractured sensor.

(b) #39: scratched sensor.

(c) #71: scratched fan-in.

(d) #34: broken ceramic in spine.

Figure 22: Cases of accidental damage to modules.

7 Conclusions

A series of assembling, bonding and testing devices have been developed, built and installed at the silicon detectors laboratory at IFIC Valencia for the construction of ATLAS SCT silicon detector modules. The assembly and quality control of the 12% of the forward ATLAS SCT modules has been successfully completed at this site. In total 282 outer and long-middle modules have been constructed during an 18-months period. The overall yield of the modules with acceptable mechanical and electrical performance is 93.3%, amounting to 118 outer and 145 inner modules. Among these modules, about 0.2% of the electronics channels show excellent readout performance.

Acknowledgements

We acknowledge support of CICYT (Spain) under the project FPA2003-03878-C02-01 and of the EU under the RTN contract: HPRN-CT-2002-00292, “The 3rd Generation as a Probe for New Physics: Technological and Experimental Approach.”

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APPENDICES

A Z-parameters

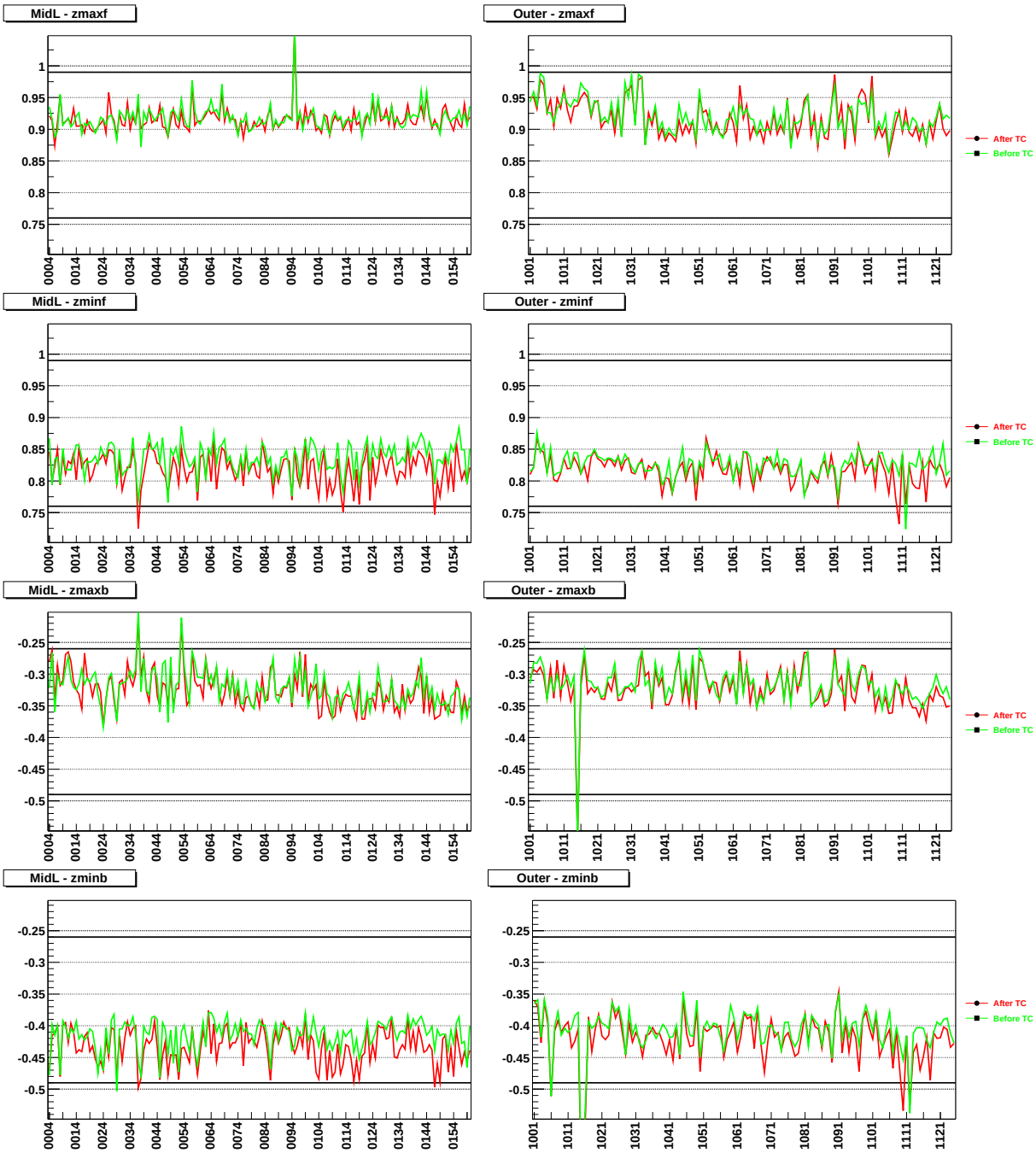

Figure 23: *Z*-parameters values (in mm) versus module number for middle (left) and outer (right) modules. From top to bottom: $zmaxf$, $zminf$, $zmaxb$, $zminb$. The thick horizontal lines denote specified tolerances.

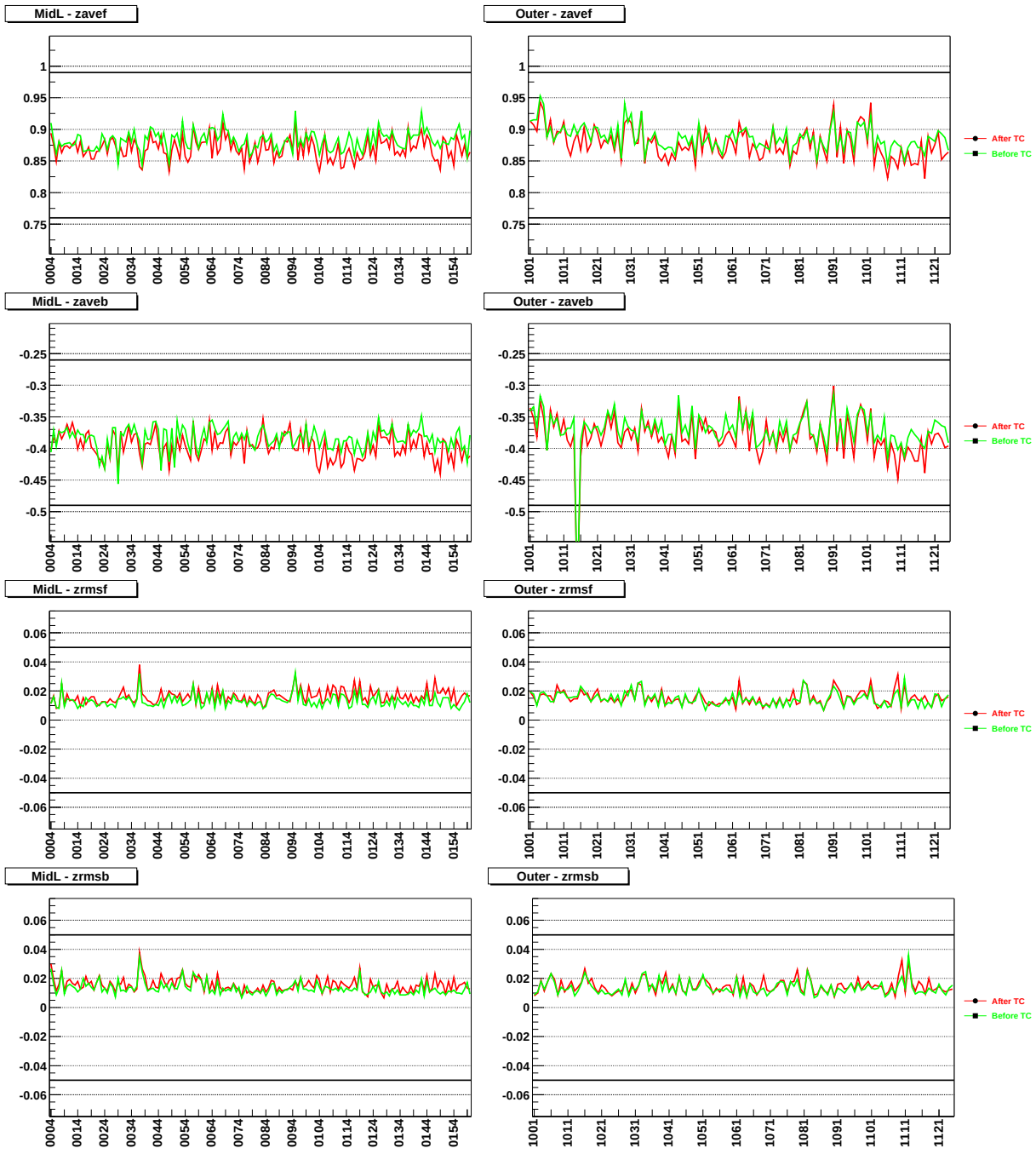

Figure 24: *Z*-parameters values (in mm) versus module number for middle (left) and outer (right) modules. From top to bottom: $zaverf$, $zaverb$, $zrmsf$, $zrmsb$. The thick horizontal lines denote specified tolerances.

B XY-parameters

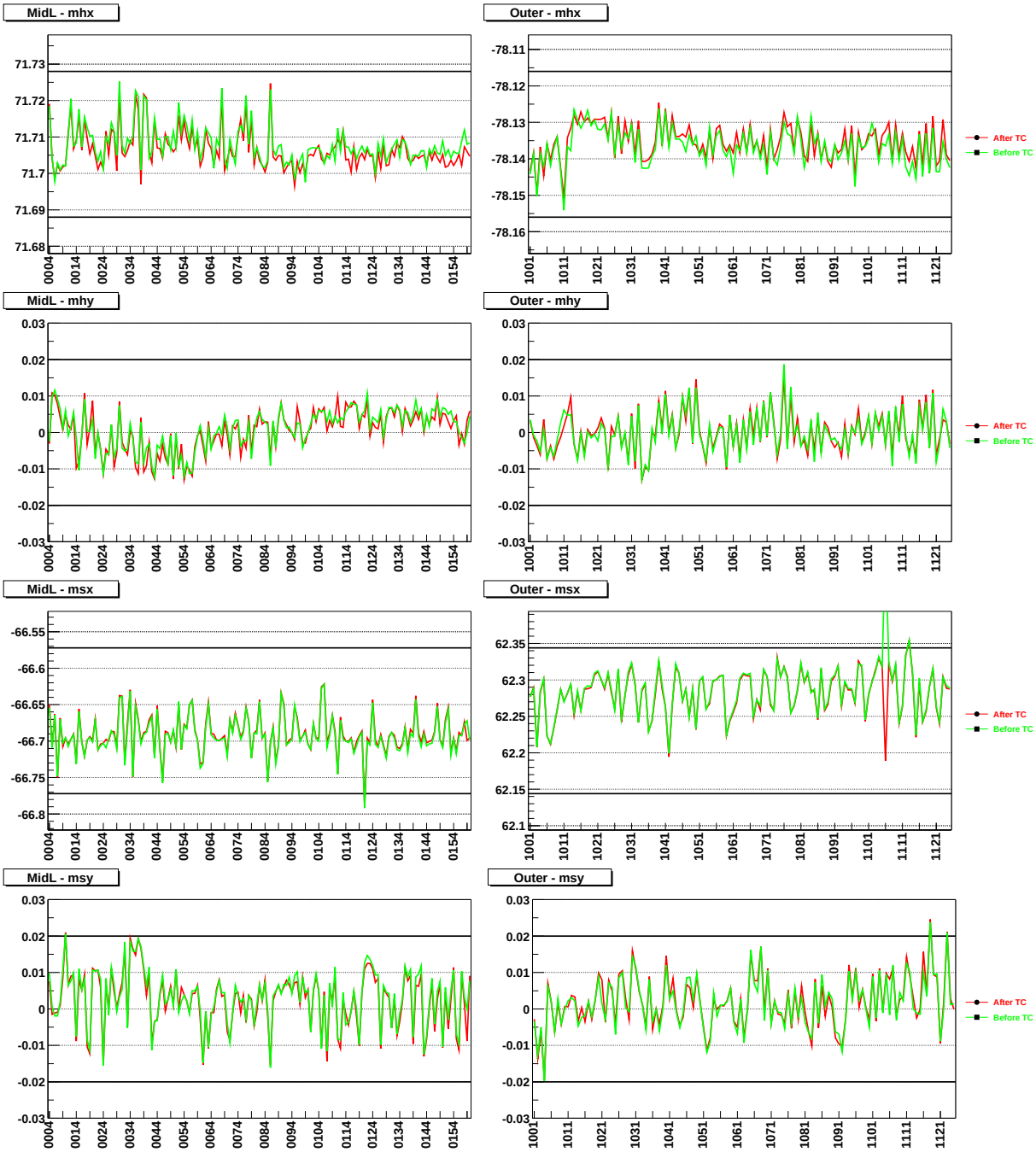

Figure 25: *XY*-parameters values (in mm) versus module number for middle (left) and outer (right) modules. From top to bottom: *mhx*, *mhy*, *msx*, *msy*. The thick horizontal lines denote specified tolerances.

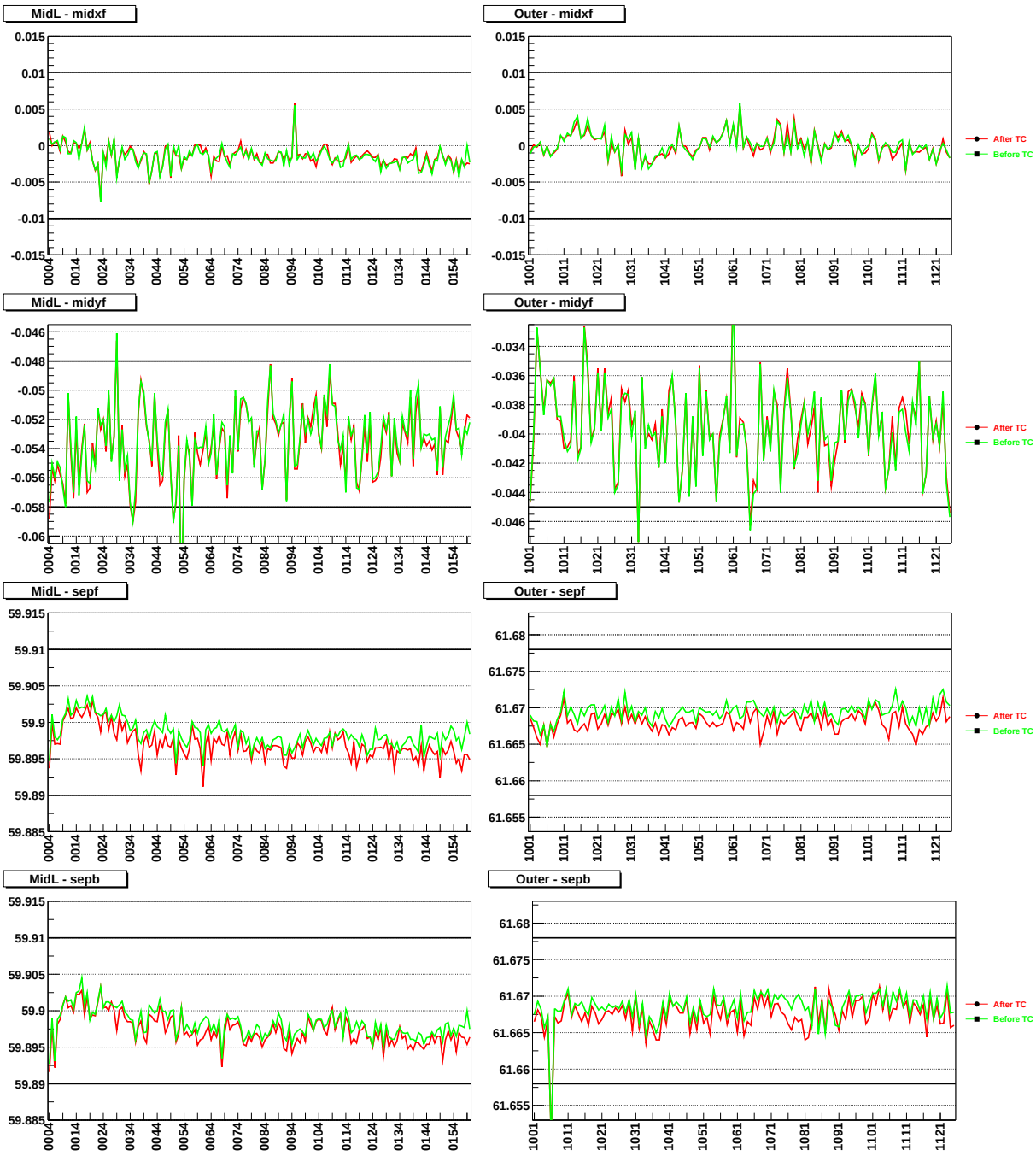

Figure 26: XY-parameters values (in mm) versus module number for middle (left) and outer (right) modules. From top to bottom: $midxf$, $midyf$, $sepf$, $sepb$. The thick horizontal lines denote specified tolerances.

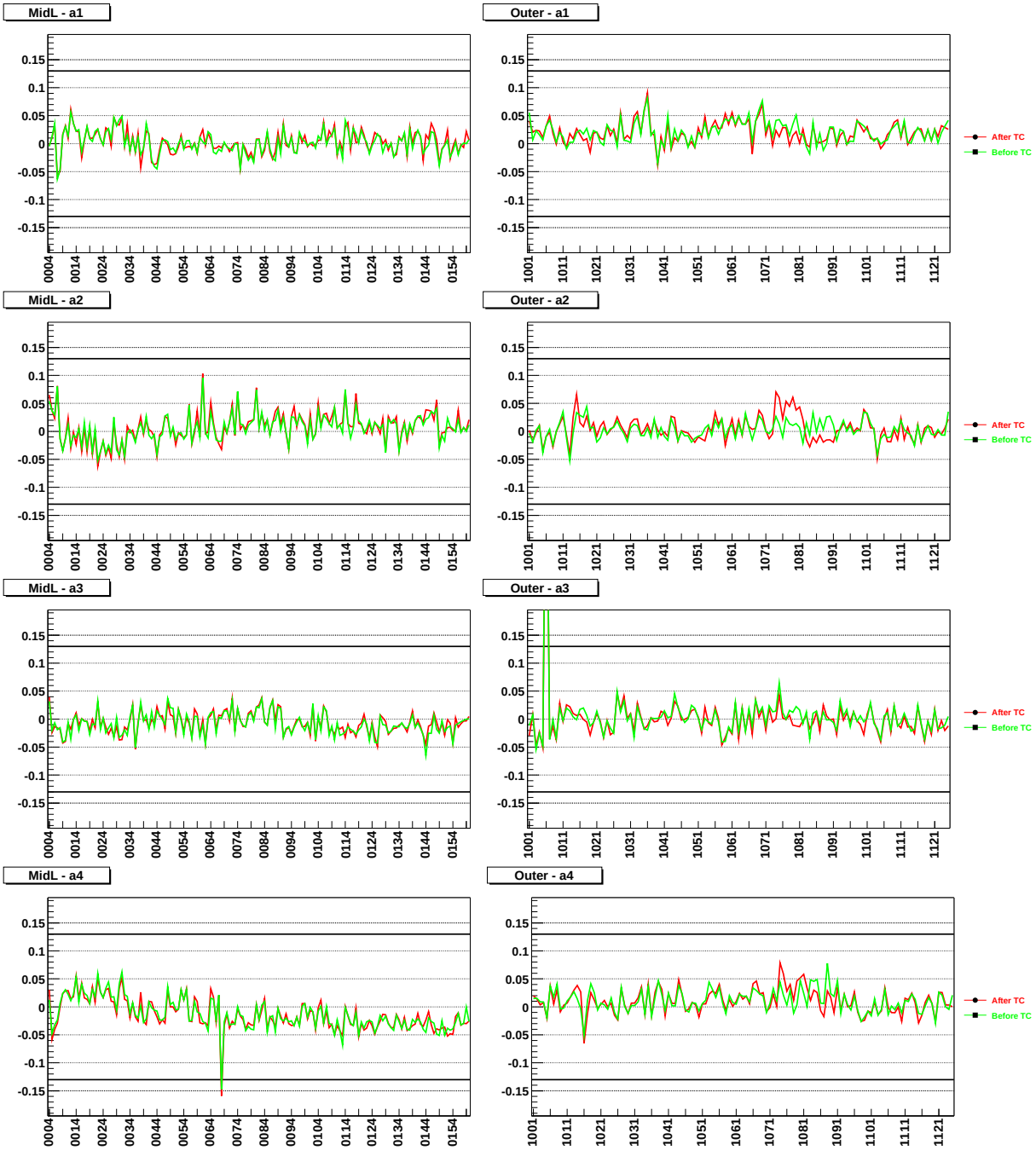

Figure 27: XY-parameters values (in mrad) versus module number for middle (left) and outer (right) modules. From top to bottom: $a1$, $a2$, $a3$, $a4$. The thick horizontal lines denote specified tolerances.

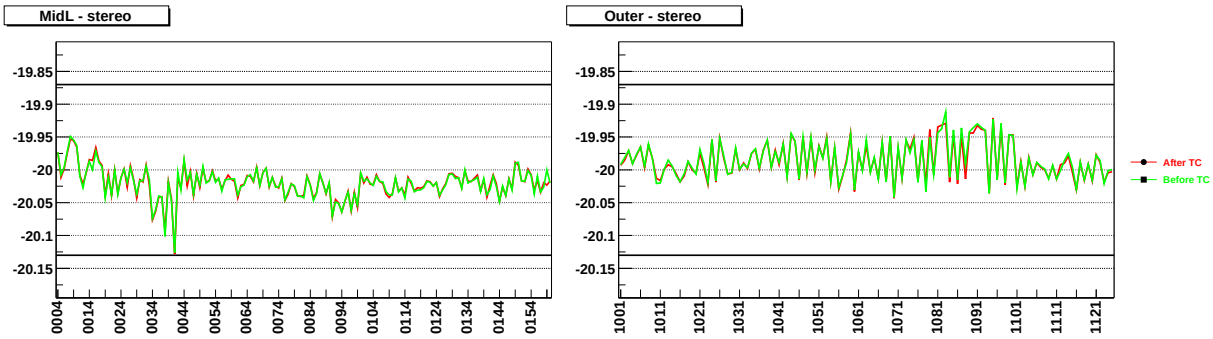

Figure 28: XY-parameter values (in mrad) versus module number for middle (left) and outer (right) modules: *stereo*. The thick horizontal lines denote specified tolerances.

C Effect of thermal cycling

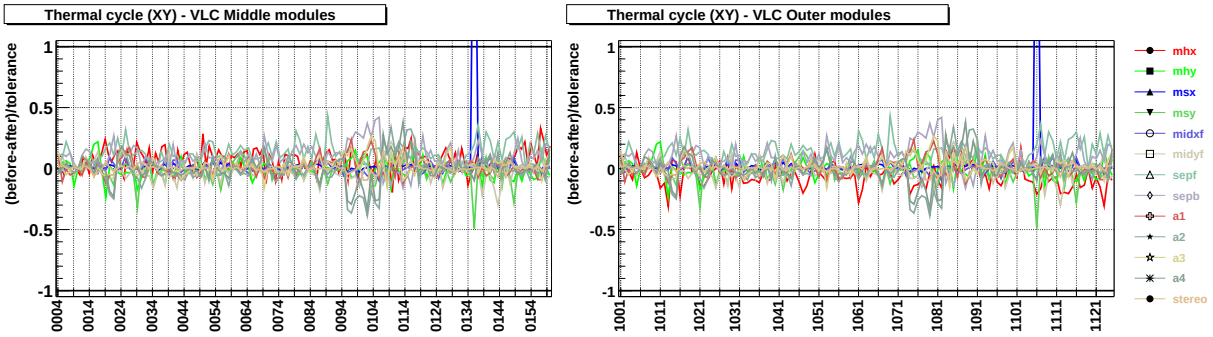

Figure 29: Fractional change in XY-parameters values after thermocycling, $(before - after)/tolerance$, versus module number for middle (left) and outer (right) modules.

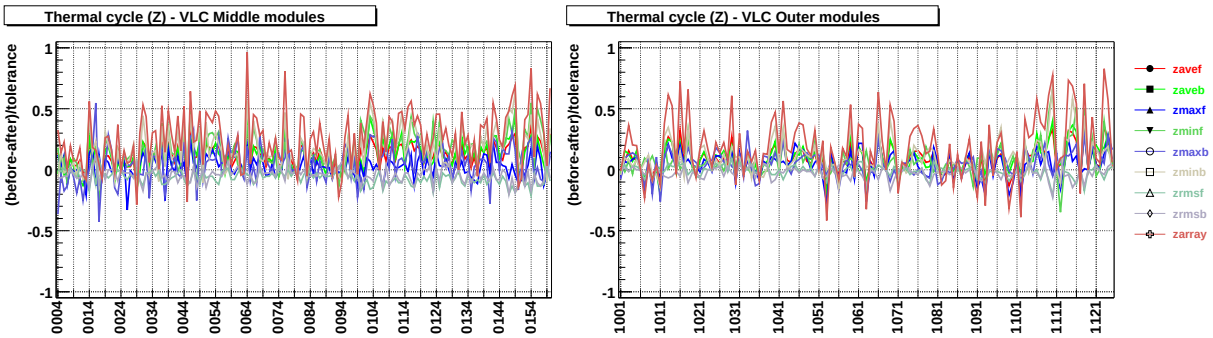

Figure 30: Fractional change in Z-parameters values after thermocycling, $(before - after)/tolerance$, versus module number for middle (left) and outer (right) modules.

D Electrical tests results

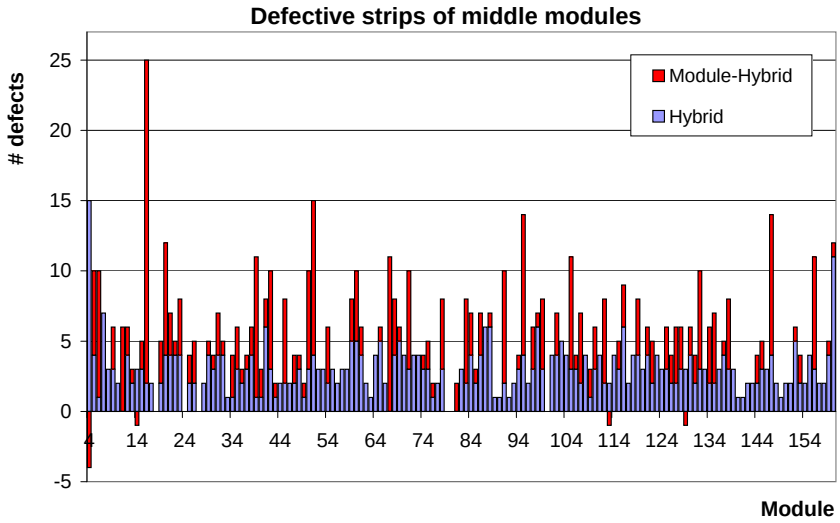

Figure 31: Number of defective strips per hybrid (blue) and module (blue+red) for middle modules.

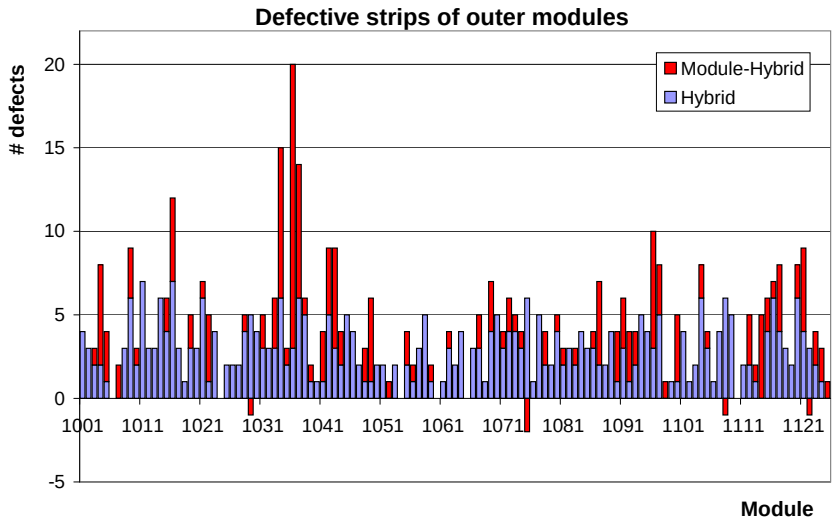

Figure 32: Number of defective strips per hybrid (blue) and module (blue+red) for outer modules.