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# A HIGH PERFORMANCE DIGITAL TRIGGERING SYSTEM FOR PHASE CONTROLLED RECTIFIERS*

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## Summary

The larger power supplies used to power accelerator magnets are most commonly polyphase rectifiers using phase control. While this method is capable of handling impressive amounts of power, it suffers from one serious disadvantage, namely that of sub-harmonic ripple. Since the stability of the stored beam depends to a considerable extent on the regulation of the current in the bending magnets, sub-harmonic ripple, especially that of low frequency, can have a detrimental effect.

At the NSLS, we have constructed a 12 pulse, phase control system using digital signal processing techniques that essentially eliminates sub-harmonic ripple.

## Introduction

The sub-harmonic ripple in a phase controlled rectifier is due to a number of causes, but the principle ones are phase to phase voltage differences and variations in SCR trigger timing.

The classicial triggering system for a 12 pulse rectifier consists of 12 ramp generators, each one being driven by a phase reference at 30° intervals. The sources of error here are the accuracy of the phase reference, and the tracking of the twelve ramp generators. Since with this method, it is essentially impossible to eliminate errors, the sub-harmonic ripple thus produced is usually reduced by means of tuned filters and negative feedback.[1]

A digital approach allows for perfect phase to phase tracking within the resolution of the system, and also allows correction to be applied to each of the 12 phases individually. This is the method which was used.

## Phase Locked Loop

At the outset of this project, some simple calculations were made to determine the characteristics of the system. The desire was to make it as high resolution as possible, but to stay within the capability of the 74LS logic family. The result was that the basic angular measurement, 30°, was made to be equal to or 4096 ($2^{12}$). Since there are twelve phases, this requires an additional 4 bits, making the resolution 15 bits (+ sign). The angular resolution, then is 4096*12 or 49152 (0.002%). Since this is a digital system, a phase locked master clock is required. The frequency of this clock is 49152*60 or 2.949 120 MHz.

The basis of this phase locked loop is a frequency source, where the output frequency depends on a binary input.[2] As may be seen from Fig. 1 a register and the A input of an adder are connected in a loop, and the B input of the adder supplies a number in the range of 0 →$2^{20}$-1. The register is clocked by the 10.5 MHz master clock. By this mechanism, the contents of the register are incremented by N each clock cycle. The larger the value of N, the faster the register will read its full-scale value and roll-over. The MSB of the register then, toggles at a rate which is dependent on the value of N. In this sytem, the clock can have a value between 2.703,360 MHz and 3.194880 MHz (55-65Hz).

Phase locking is achieved by means of a frequency discrimination and phase comparator. The outputs of these devices control a look-up table which in turn controls an up-down counter. When the loop is grossly out of lock, the phase comparator is effectively disabled, and the counter is driven in the direction which will cause $f_1$ and $f_2$ to match. At this point, the phase comparator takes over, and cause $f_1$ and $f_2$ to come into phase lock.

## Trigger Generator

The function of the trigger generator is to take a binary input in the range of 0 - 24575 and convert this to a series of 12 trigger pulse trains, each with a range of 0 - 180° and offset from each other by 30°. In addition, an arbitrary phase shift is added to displace the phase reference anywhere from 0 - 120°, in order to eliminate the need for a reference phase shifting transformer.

As may be seen from Fig. 2, the range from full rectify, phase 0, to full invert, phase 11, is 510°. This is the reason for having two counters A and B (Fig. 3). Counter A provides the instantaneous phase reference with respect to the line, having a range of 360°, and counter B provides the instantaneous phase reference as to when the SCR's are to be fired. A third counter, the phase counter, provides a pointer as to which SCR is to be fired next.

Since 30° is equal to 4096 ($2^{12}$), it follows that bits 12, 13, and 14 indicate which block of 4096 the trigger is to take place in (ie. 0 indicates full rectify, and phase 0 would be triggered at 0°, phase 1 at 30°, etc.). This fact is used to synchronize all the counters. Counter A is decoded to give a sync pulse at 24,575. This loads the contents of the A counter to the B counter, and also loads the correct value into the phase counter from a look-up table. Loading the phase counter each cycle ensures correct functioning at power up, and also immediate recovery from any noise induced errors.

The timing pulses developed in the trigger generator then go to the decoder driver. A 60 Hz phase reference pulse is loaded into a 12 bit shift register which is clocked every 30°. The 12 outputs, on for 180°, off for 180°, and offset by 30° are used to enable 12 J-K flip-flops. The J-K's, then are turned on by a trigger pulse addressed to it by the phase counter, and turned off by the removal of the enable. The output of the each J-K enables an and gate, which turns on a 20 KHz, 20% duty cycle square wave to the SCR gate driver.

## Ripple Correction

A 12 pulse phase controlled rectifier may be considered to be a DC source sampled at 720 Hz. Ideally, all the samples would be the same amplitude, and the frequency spectrum would contain only the sampling frequency. In practice, however, unbalances in phase

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to phase voltage and transformers inductance introduce voltage variations at each sample. The result is subharmonic ripple. Since the triggering system allows specifying the voltage of each phase, it is possible to modify the point at which each rectifier is triggered. The mechanism for doing this is shown in Fig. 4.

Since the transfer functions of the trigger generator is a cosine function, it is necessary to use a linear to cosine conversion so that the correction factor will have the same weight, independent of conduction angle. When no correction is applied, the correction input to the adder is 0, and each phase will trigger at the same angle. Correction is applied by enabling the output of one of the buffers. Each buffer has twelve locations, one for each phase. These locations are addressed by the phase counter. As the trigger generator cycles through the twelve phases, the contents of each consecutive buffer location is added in two's complement to the output of the A/D, modifying the trigger angle, and thus the voltage at each sample. The buffers are loaded from a voltage at each sample. The buffers are loaded from a test module at this time, but a microprocessor based controller has been designed which will perform the correction functions in real-time. The mechanism for arriving at the correction values is shown in Fig. 5.

The A/D samples at a rate of 11,520 samples per second, thereby giving 16 samples per phase. The fundamental harmonic is effectively removed by averaging these 16 samples. The 12 phase voltages are then averaged to derive the DC component $a_0$. The voltage to offset the error at each phase is calculated, and knowing the system gain (volts/degree), the correction factor is derived. This may be considered to be the equivalent of summing two sine functions of the same amplitude, and 180° out of phase.

## References


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2. Rolf Olsen, Ernst Munter, U.S. Patent 4,076,965.


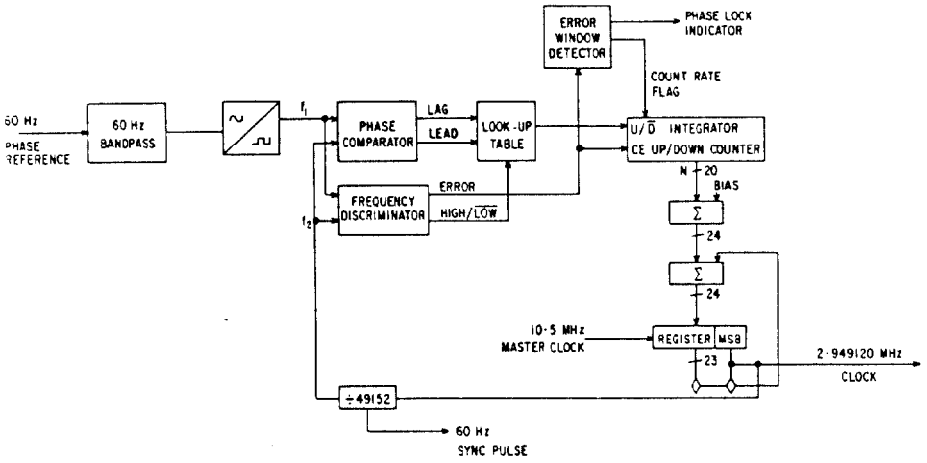


Fig. 1.

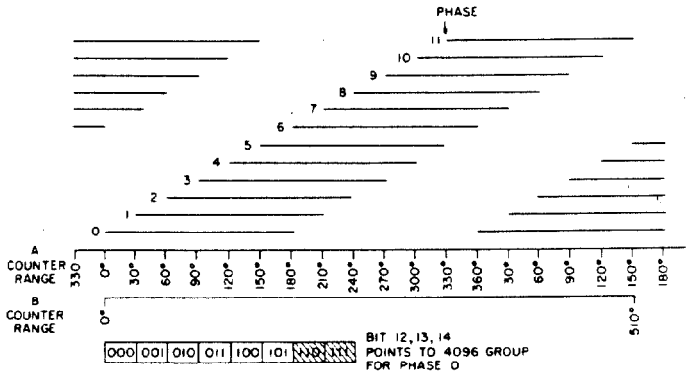


Fig. 2.

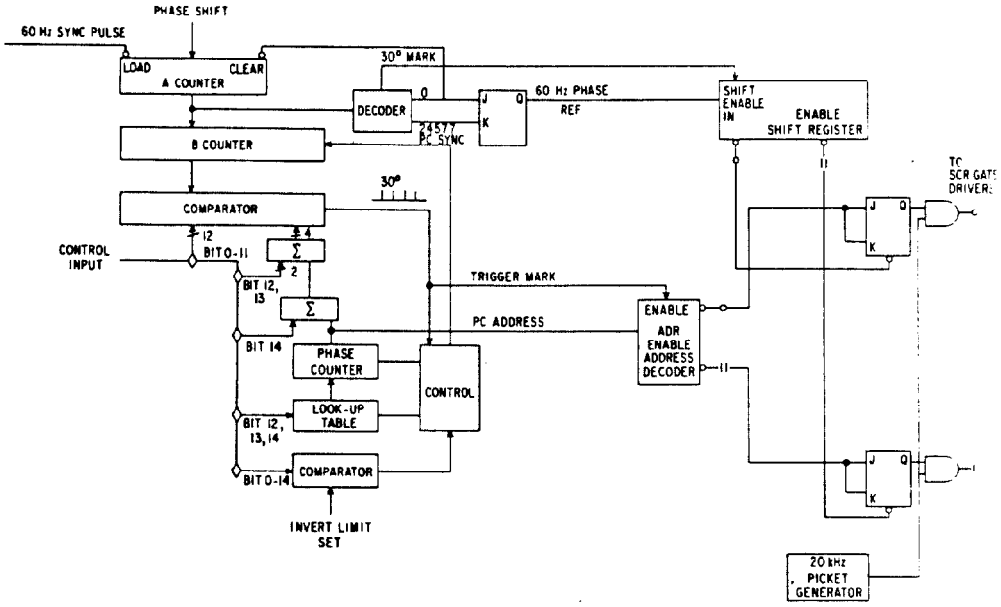


Fig. 3.

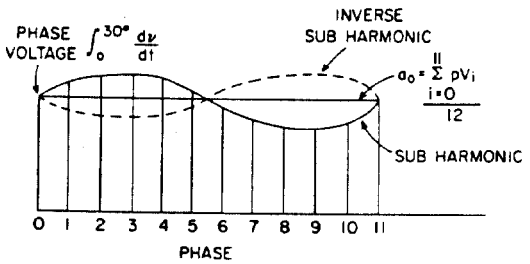


Fig. 4.

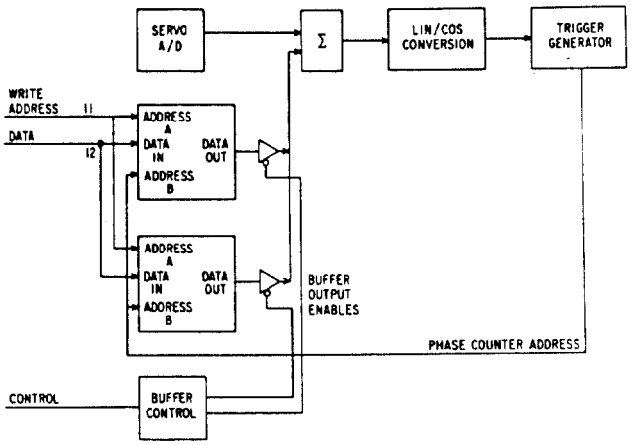


Fig. 5.