RF ACCELERATING SYSTEM AT HIRFL-CSR MAIN RING

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Abstract

A heavy ion cooler-storage ring HIRFL-CSR[1] has being constructed at IMP. It consists of a main ring (CSRm) and an experimental ring (CSRe). Two RF cavities will be employed for CSRm. One is for beam acceleration, and another is for beam RF stacking. The accelerating cavity is designed to accelerate the beam from 10-50MeV/u to 400-900MeV/u with harmonic number h=1. The peak RF voltage is 8.0kV and frequency range is from 0.25 MHz to 1.7 MHz. The RF stacking cavity with maximum voltage amplitude of 20kV and tunable frequency range 6.0-14.0 MHz is used to capture the injected bunches from injector SSC (or SFC) and to accumulate the beam to high intensity by RF stacking method. In the present paper, the measured RF parameters and the details of hardware for the RF accelerating system are described.

MAIN RF ACCELERATION PARAMETERS

The specifications for RF acceleration system of CSRm ring are shown in Table 1.

Table 1: RF Accelerating parameters

Injection Energy	10-25 MeV/u
Acceleration energy	900 MeV/u
Momentum spread at injection	$< \pm 0.15\%$
Harmonic Number	1
Acceleration frequency	0.25-1.7 MHz
Maximum RF acceleration voltage	8.0 kV

The Lowest injection energy is 10 MeV/u for $^{238}U^{72+}$ ions among various ions from the injector SSC (or SFC), corresponding to the revolution frequency 0.25 MHz. At the top energy of 900 MeV/u for $^{12}C^{6+}$, the revolution frequency is 1.7 MHz. The harmonic number 1 will be employed to accelerate the ions thus the RF frequency should cover the frequency range from 0.25 MHz to 1.7 MHz. The Maximum acceleration voltage of 8.0 kV is needed for the beam acceleration with ±0.15% momentum spread within acceleration period of 3.0s.

RF CAVITY

The RF cavity has a single-accelerating-gap structure, which consists of two ferrite-loaded quarter-wave coaxial resonators (Fig.1).

We selected the ferrite material 600HH for cavity. The dimension of ferrite rings is 480mm in outer-diameter, 300 mm in inner-diameter and 20 mm in thickness. The ferrite rings are assembled in 4 stacks, 2 stacks for each of the two halves. Totally, 80 pieces of ferrite disks are stacked in whole cavity. Two bias windings had be made, one for two stacks of the cavity. Every winding will have 12 sections, 8 turns in each section. Ends of each turn go outside the cavity wall and are accessible. It is possible to connect the turns in series, in parallel or mixed connection depending on available power supply for biasing of for other consideration. The magnetic permeability can be varied from 600 to 12. There is a margin of 20% for biasing current to compensate for temperature and other instabilities. Maximum value of RF voltage at the winding is lower than 2.5 kV.

The space between electrical conductors of the cavity is filled with silicon hermetic of VIKSINT type. It provides mechanical and electrical stability, better conditions for cooling, and excellent insulation of elements at a high RF electric field.

Fig.1 HIRFL-CSR Main ring accelerating cavity

LOW LEVERL RF SYSTEM

The low-level RF electronic system is composed of a Direct Digital Synthesizer (DDS) as the master oscillator and several feedback loops (Fig.2). Three memory modules store the ramping data: frequency, acceleration voltage and bias current as functions of bending-magnet field strength. These pre-set data are put into the DDS, magnitude modulation and bias current power supply respectively. The bias current error obtained from RF signal phase detector which get the deviate of the RF cavity by comparing the plate's and the grid's sampling signal will be used to correct the deviation of the cavity through the auto frequency control (AFC).

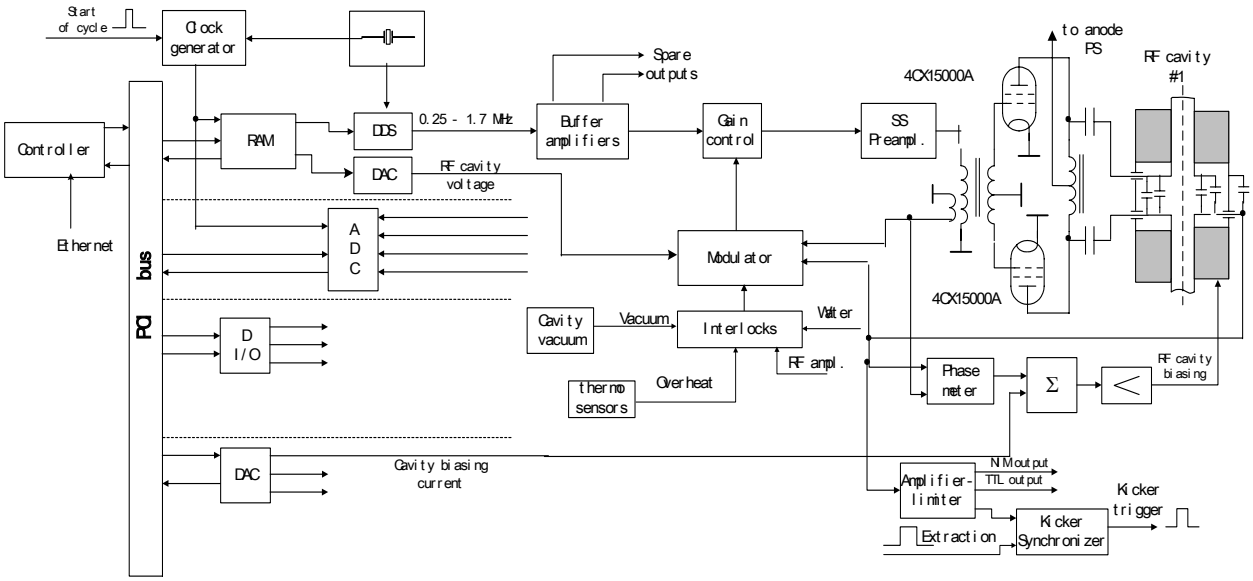

Fig.2 Block Diagram of RF control system for CSR Main Ring accelerating cavity

RF signal control unit is developed as PCI bus based modules. All these modules are independent sub-system, which have their own MCU.

DDS Circuit

The RF signal process applys the advanced DDS plan. The AD's AD9832 is functioned with the 16BIT processor in parallel connect mode to achieve high synthesis updating of signal. The local control processor sends data to DDS chip to release the RF signal. At mean time DDS receives the information from the control system to adjust the outputting frequency.

Phase Loop

Phase loop is used to compensate the deviation between the DDS and cavity voltage, achieving phase lock among RF cavity voltage and cavity voltage phase. All sample signals serving above units come from one identical detector; each of them has its own isolator to proof interference.

Bias Current Control Loop

The signal of V/F converted from the DDS synthesis's RF signal or the signal of D/A converted directly from digital data applying to DDS input is put to FREQ/RES adjusting unit to control the bios current. The offset value from MCU and the signal from phase discriminating between the cavity voltage and grid of the final stage power amplifier are also fed into this unit. The FREQ/RES correction must be a real time analogy circuit to dynamically tune the cavity. The signals after F/V converter that represents the changing of the frequency add one from the phase discriminator. The sum is put into the bios current driver to control the saturation of the ferrite so as to tune the cavity.

MCU/DAC 's data compensates the nonlinear relation between the bios current and the permit of the ferrite and offsets the bios current's initializing value.

RF Frequency Control Loop

RF system requires frequency resolution be less than 100Hz, frequency stability less than 10^{-5} thus requires non less than 16Bits control word and less than 1us update rate of frequency sweeping. The digital dividing PLL may meet the requirement, but it update speed is determined by the frequency resolution. The fact is that the higher the frequency resolution the lower the updating speed. This is determined by the LPF of the PLL loop. Furthermore at high dividing rate 1/N requiring by large frequency range, the loop gain drops to 1/N to damage the loop stability, at this situation the high stability power supply is needed to meet the critical requirement. The advanced DDS tech can resolve this problem.

Applying 16Bit/32Bit MCU or PLD to control the DDS RF signal processing circuit to attain high speed and real time control. 16Bit of amplitude data are also applied to amplitude modulation unit, which also serves as amplitude stability control to achieve 10^{-2}-10^{-3} rates. The bios current data supplying by MCU are converted by DA to feed into the bios current power supply which actuating the coil. Bios current error derived from the deviation of cavity's resonance and DDS frequency tunes the cavity through AFC. MCU connected with PCI bus receives the control word. All DAC and ADC are high-speed products.

The connection between the RF and CSR control bus applies PCI function module and particular parameter and timing network.

TESTING RESULTS

The acceptance testing had been made according to operating cycle of $^{12}C^{6+}$ being accelerated from 25 to 900 MeV/u and $^{238}U^{92+}$ from 10 to 450MeV/u. The maximum RF voltage of 8.25 kV had been obtained in the designed frequency range of 0.25 – 1.7MHz.

REFERENCES

J. W. Xia et al. "HIRFL status and HIRFL-CSR project in Lanzhou". APAC'98, KEK, Tsukuba, Japan, March 1998.