NEWLY DESIGNED FIELD CONTROL MODULE FOR THE SNS*

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Abstract

The low-level RF (LLRF) control system for the Spallation Neutron Source has undergone some recent hardware changes. The intended Field and Resonance Control Module (FRCM) design has been re-vamped to minimize functionality and ease implementation. This effort spans a variety of disciplines, and requires parallel development with distinct interface controls. This paper will discuss the platform chosen, the design requirements that will be met, and the parallel development efforts on-going.

OVERVIEW OF THE NEW FCM

Performance specifications were eased late last year for the LLRF control system for SNS. Physics simulations indicated that the field control requirement could be reduced from from ±0.5%, ±0.5° to ±1.0%, ±1.0°. In addition required functions were changed such that on-board processing for resonance control was moved to the crate controller (IOC), as well as feedforward table update and access; fewer RF channels were required (no need to provide for possible beam information via a beam diagnostics channel); no real time data link needed between the control system and the operators; and much less memory per channel was deemed appropriate. By moving the iterative learning controls onto the IOC as well, we completely eliminated the need for DSPs on the module. A collaborative effort was established between Lawrence Berkely, Los Alamos, and Oak Ridge national labs in order to develop a control system that meets these specifications [1].

Due to these relaxed system performance specifications, and a new staged approach to implementation and integration of control system functions, the original complicated, meet-all-performance-specifications-at-once FRCM de-sign has been greatly simplified. The new Field Control Module (FCM) is still a basic VXIbus-based module with multiple daughter cards. The infrastructure for a VXIbus-based RF Control System (RFCS) was already in place at the SNS: VXIbus crates had been purchased and other modules within the system are VXIbus, so it only made sense to remain consistent. However the new FCM has three new daughter cards which minimize the functionality of the FCM; and the implementation of the firmware is in a staged approach where progressive phases will be achieved as the accelerator grows from one cavity to many and functional requirements of the RFCS increase [1]. A block diagram of the module hardware is given in figure 1.

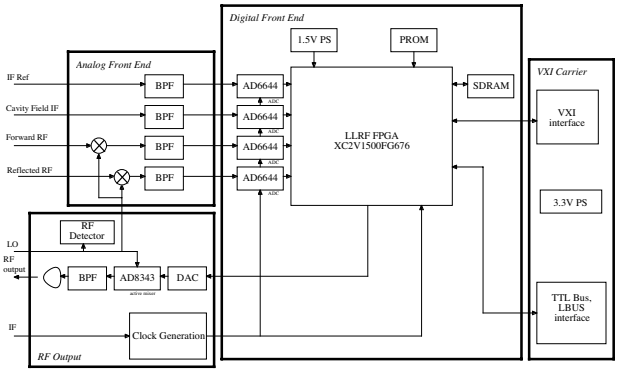

Figure 1: FCM Block Diagram

PRINTED CIRCUIT CARDS

The basis for the re-designed FCM is the successful SNS Diagnostics PCI-based electronics, specifically the Beam Position Monitors (BPMs) [2]. In that vein, we attempted to make use of as much of the foundation provided by the Diagnostics BPMs as possible. The BPMs have an Analog Front End daughter card manufactured by Bergoz Instrumentation of France. Likewise, we specified a very similar LLRF AFE for use on the FCM. The BPMs have a Digital Front End (DFE) processing card. We, too, utilize a DFE for providing the analog-to-digital conversion of the input RF and IF signals, as well as for providing an interface to the host computer. In this case, however, the LLRF system continues to utilize an MVME2101-1 slot zero controller for its CPU. Unlike the diagnostic BPM, the LLRF system requires an RF output for driving the correctly controlled signal to the klystron, hence another daughter card: the RF Output (RFO).

Two primary reasons drove us to utilize the BPMs as a foundation for the new FCM. The first is the similarity between the BPM AFE and the requirements for the LLRF AFE. By essentially removing two downconverting stages for IF channels on the LLRF AFE, and eliminating extra diagnostic switches on the BPM AFE, the design for the LLRF AFE was complete. Therefore with minimal change, we incurred very little design risks and expected to achieve performance expectations on the first pass. Secondly, by using the PCI mother board as a test platform for the newly designed LLRF daughter cards, we took advantage of the existing board tests already written for testing the BPM performance, thereby reducing extensive test development time. LabVIEW programs have already been written for easy measurement of channel isolation, ADC performance analysis and the like.

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AFE

An AFE daughter board photo is shown in figure 2.

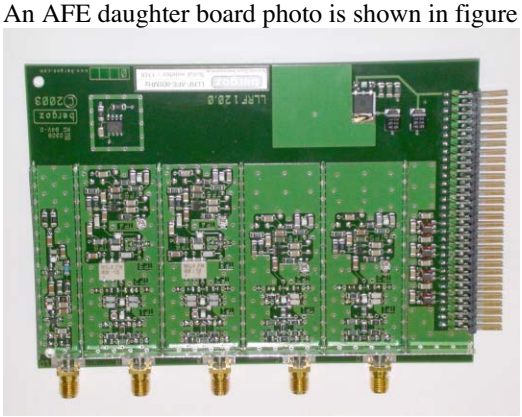

Figure 2: LLRF Analog Front End daughter board from Bergoz Instrumentation.

The key requirements for the AFE are channel to channel isolation and dynamic range (30 dB). Bergoz was able to meet all specifications on the first prototype board, with the exception of isolation on the IF channels. A simple bypass capacitor and filtering scheme on some power lines, however, solved the problem.

DFE

A photo of the DFE is shown in figure 3.

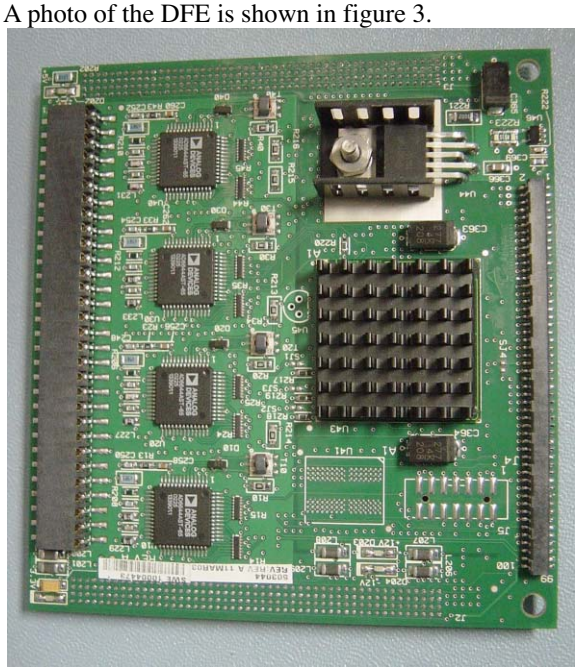

Figure 3: SNS LLRF Digital Front End daughter board.

The chief component of the DFE is a Xilinx Virtex-II XC2V1500FG676, shown in the photograph with its large finned heat sink on top. The DFE essentially receives the analog IF signals from the AFE and translates them to digital signals for processing through Analog Devices AD6644 14-bit ADCs. The FPGA provides the path through which the feedback control algorithms are implemented. In addition, it is the key component that provides an interface between the control system and the operator: registers, history buffers, data multiplexers…

RFO

A photo of the RFO is shown in figure 4.

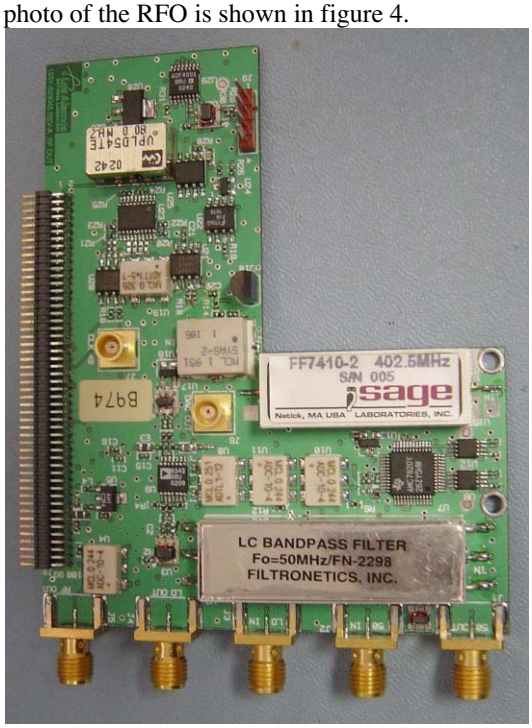

Figure 4: RF Output daughter board.

The primary purpose of the RFO is to translate the 50 MHz baseband control signals from the Digital Front End (DFE) from digital to analog signals and then upconvert them to the RF frequency. In addition it is the home for the phase locked loop clock generation circuitry, which is the basis for all of the coherent sampling on the module. Essentially the RF Output board core components are a 14-bit DAC, an upconverting Analog Devices active mixer AD8343, and some filters. However, it also acts as the distribution center for the 50 MHz Reference and the LO required by the other daughter cards

The key requirements for the RFO is its spectral response, dynamic range (30 dB from -20 to +10 dBm), and clock generation. Important to the success of the FCM is its ability to maintain tight synchronization between the external 50 MHz IF reference, and the on-board generated 40 MHz ADC clock and the 80 MHz FPGA clock. Larry Doolittle built and tested such a circuit for use on his Berkeley LLRF system [3], and it works well. This same circuit, reliant on the Analog Devices ADF4001 clock generator chip, is now in use on the RFO as well as the SNS Diagnostic BPM boards. Initially there was concern over jitter in the clock system. However, white noise averages out rather nicely on the time scales of the closed-loop-bandwidth of the cavity. Therefore a jitter goal of 2 or 3 ps RMS from 2 kHz to 40 MHz is perfectly reasonable. The low frequency, DC to 2 kHz jitter is taken out by the phase locked-loop, although here the performance is limited by the PLL phase

comparator, which itself presumably has a 1/f term. The software and phase reference line should be able to correct that error down to DC.

MOTHER BOARD

The VXIbus mother board is very basic. Its primary purpose is to provide a platform for the AFE/DFE/RFO combination, and to provide for communication with the VXIbus backplane. In addition it receives system timing signals from the Brookhaven Laboratory-designed Timing Module (model V124S) and translates them to the DFE and VXI backplane for system synchronization.

Figure 5 shows the fully populated Field Control Module: a mother board VXI carrier with mounted AFE, DFE, and RFO. Interconnect cables are not mounted, neither is the front panel. A front-panel mounted blind-mate sub D housing is used to complete the cable routing from the daughter cards to the front panel. The board is a single-wide VXIbus module.

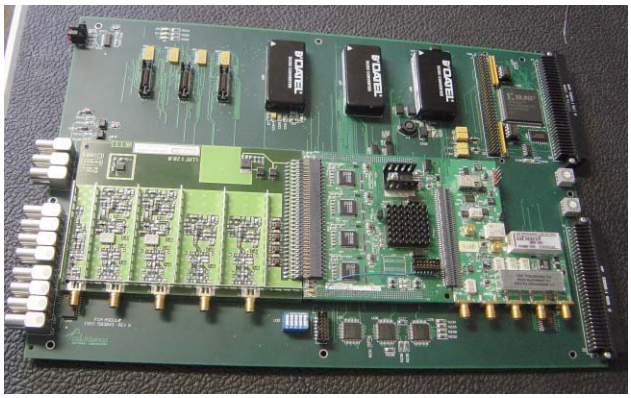

Figure 5. Field Control Module

FIRMWARE

The foundation for all of the phase I control algorithms was written in verilog for a 12-bit system by Larry Doolittle [3]. In order to produce a control system which has a common language that can be maintained by more people, these algorithms have been converted to VHDL by Craig Swanson. The hardware wrapper is also written in VHDL by Matt Stettler. A firmware specification was written at the outset of the conversion process in order to make sure that the interfaces are complete and various people can all work on the same end product. Close communication between the firmware designers has helped close any gaps. The firmware is written in a modular format and test benches have been written for a ModelSim simulation of each step.

As previously reported [4,5], we have performed extensive modeling of the SNS RF control system. This model has been developed in MATLAB/Simulink. Part of the validation of the overall firmware design is to utilize the MATLAB model to generate input test vectors for the DFE's FPGA VHDL code. Then the FPGA firmware will be simulated with ModelSim using the given input test vectors and will generate outputs. The ModelSim outputs will be compared to MATLAB/Simulink outputs. Any discrepancies between the two will be analyzed and used to modify the firmware code accordingly. This work is in progress now.

While the firmware is being developed, a register map has been created and provided for EPICS development. Because this system utilizes much of Larry's code as well has the same inputs and output, much of the EPICS screen development and some of the scripts that have been utilized in the past are still applicable.

WHERE WE ARE TODAY

At this point in time we are in the process of validating each of the daughter boards individually. The AFE and mother board have been certified. Design validation of the RFO is nearly complete. Tests on the RFO are being run via a DFE on a Diagnostics PCI mother board, and hence that interface is also being worked. The DFE hardware works, and the FPGA code is more than 70% complete and simulated. We intend to integrate the module in the lab with a dummy cavity and the EPICS global controls, and will be given a chance to try it out on a real DTL cavity at SNS this summer.

REFERENCES

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[5] Kwon, S.I., et al, "Uncertain System Modeling of the SNS RF Control System," PAC'01, Chicago, IL, June 2001.