REAL TIME, DISTRIBUTED, HARDWARE-SOFTWARE SIMULATION OF MULTICAVITY RF STATION FOR LLRF SYSTEM DEVELOPMENT IN FLASH AND XFEL

P. Pucyk, DESY, Hamburg, Germany, ISE, Warsaw, Poland
S. Simrock, DESY, Hamburg, Germany
W. Jalmuzna, DMCS, Lodz, Poland

Abstract

The paper describes the implementation of distributed (FPGA, GPP) system for simulation of multiple TESLA cavities and high power distribution chain. Applied models simulate the system behavior with the performance close to the response time of the real RF station and cryomodules. Parameterized architecture of the simulator allows to find compromise between the complexity of the model and the available FPGA resources. The results of laboratory tests and driving the simulator using the FLASH (Free LASer in Hamburg) LLRF system are presented. Proposed solution is the important tool for LLRF system development and testing, and can be alternative for the usage in the real superconducting facilities reducing the development costs and time.

MOTIVATION

For the European XFEL [3] the LLRF system is being developed. Each RF station consisting of amplifiers, klystron, high power distribution and 32 cavities will provide over 100 physical signals to the digital controller which stabilizes the vector sum of field in cavities. The LLRF system will be used not only in operation, but also during commissioning of the XFEL cryomodules. It is also required that LLRF system will handle exceptions and provide continues operation of the accelerator. In addition many control algorithms have to be automated.The development of such complex system needs a test bench. Algorithms can be partially verified using software and generated test data. However the performance of the system and hardware-software interaction requires real operation environment. The availability of the real test facilities with complete rf station is very limited. Moreover, some of algorithms and exception handling procedure require setting the machine into extreme conditions in which the exception can occur. Such tests can dramatically reduce the lifetime of the machine. For that purpose hardware, real time simulator has been developed. The aim of the project is to simulate the behavior of the RF system for LLRF control purposes. FPGA technology provides flexibility in defining the hardware functionality. Therefore the simulator has been implemented in the same hardware platform as the LLRF controller for FLASH, which is very similar in the design and technology to the XFEL.

SYSTEM MODELLING

The modelled system consists of functional blocks (Fig. 1). These blocks represent particular subsystems or components like klystron, cavity or cables. All blocks have inputs and outputs in I and Q domain. The inputs to the simulator are the I and Q signals from the output of the controller [1]. The first processing block is the klystron. Its model simulates the amplitude and phase nonlinearities using LUT and linear interpolation. After the klystron, the signal is splitted. The high power distribution system is modelled here by scaling blocks which simulate power distribution to the cavities. Since all cavities in FLASH cryomodule are fed with the signal in the phase, there is no need to add phase change in this block. The next block is the cavity. It has been simulated using electro-mechanical model [5] with Lorentz force detuning (LFD). The main adjustable parameters are: resonance frequency, loaded Q, shunt impedance and predetuning. Moreover, for each of 3 mechanical modes the quality factor, frequency of the mode and LFD constant are adjustable.

The cavity block has two additional inputs for beam signal. It can be provided through ADCs to simulate different bunch trains. However, for the simplicity of calculations, the beam signal is not interpreted as a current but as gradient induced in the cavity.

The cavity model provides three pairs (I,Q) of output signals: the field inside the cavity, the forward and the reflected power. Each of the output signals is connected to the scaling and rotation block. This block simulates the attenuation and phase change in the measurement path of the controller caused by different length of cables. The last simulation block is the IQ modulator. For FLASH operation, the 250kHz intermediate frequency is used. The multiplexer at the end of the processing chain selects the chosen cavity output and send it to DAC output.

IMPLEMENTATION

The presetned model has been implemented in SIMCON 3.1-DSP board [2]. It is the base hardware platform for LLRF system in FLASH. The board is equipped with Xilinx Virtex 2pro chip, Analog Devices TigerSHARC floating point DSP, 10 ADCs (105MHz), 8 DACs (165MHz), and optical transievers. The form factor is VME (6U). The simulator runs with 100MHz clock. The complete simu-

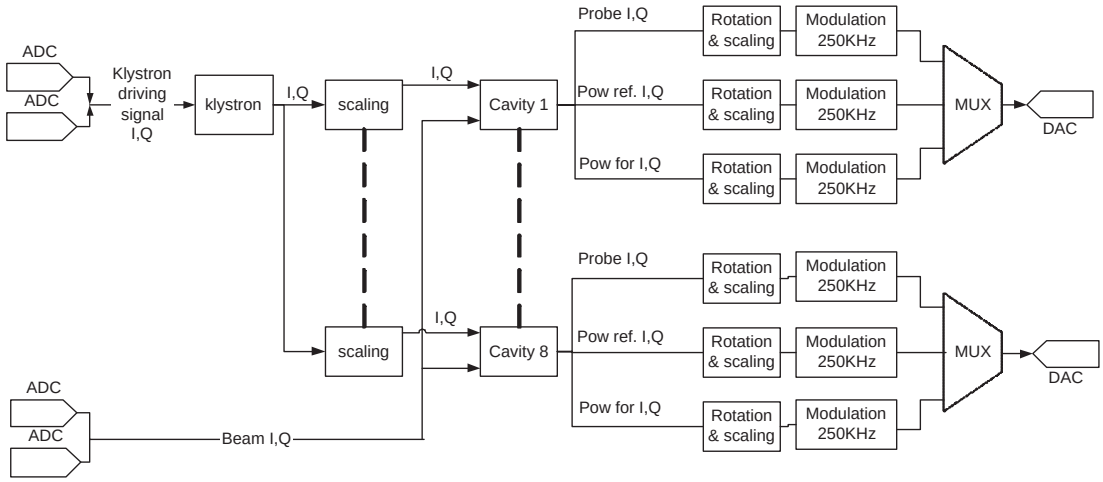

Figure 1: Block diagram of the simulator. Data processing chain consists of several blocks representing different elements of the real rf station.

lation chain is executed in 20 clock cycles (200ns). The simulator operates in CW mode. It means it process continuously data from the input.

The communication with the board is performed through VME bus. There are two ways of adjusting simulation parameters. One can use Matlab and access the hardware directly [6]. This solution gives the possibility to change parameters in wider ranges and access expert features. The second option is to use the dedicated DOOCS [4] server which integrates the simulator with the control system.

Simulator can run in various modes of operation. The mode of operation is related with source of the timing signals and the source of the driving signal. Simulator requires two clock signals. Strobe signal triggers the calculation of one sample from the input. Trigger signal starts the data acquisition the internal memory. The typical trigger frequency varies from 2Hz to 10Hz and strobe frequency is 1MHz. If the simulator is running with external timing, both signals are connected to the board. This allows to be synchronized with the FLASH timing system and record data during the RF pulse. In the laboratory one can use internal timing. In this mode the trigger and strobe are generated inside the FPGA and can their frequency can be configured online by the user. Beside the source of the timing signals one can also choose how the simulator is driven. One option is to sample signal from ADC. However there is a possibility to drive the simulator using internal software tables loaded into FPGA by the user. One can create artificial driving signal and beam signal (or one recorded in the accelerator), load it into the FPGA and use it as an input for the simulation.

RESULTS

The simulator has been tested in laboratory and FLASH. In laboratory the simulator have been driven from the signal generator or internal tables. The example response of the simulator is presented in Fig. 3. It was driven by internal tables [Fig. 2] Each of four cavities had different parameters. For the presentation purpose two cavities had Q_L adjusted to $3.8 * 10^6$ resulting the higher gradient and two cavities with $Q_L = 3 * 10^6$ (see Fig. 3, left plot).

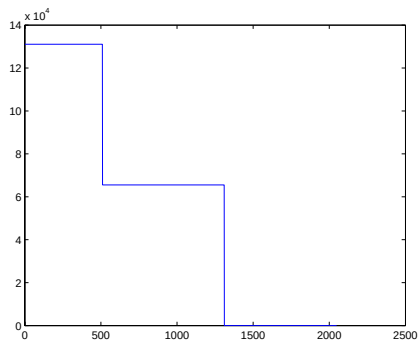

Figure 2: Driving signal for the simulator. Since the phase of the signal is zero, only I component is visible.

In the FLASH, the simulator was synchronized with the machine timing. The output of the controller has been splitted into the simulator and real machine. Next , the characteristics of the klystron have been measured and applied to the simulator. Thanks to that the real and simulated cavities were driven with the same signal. The example response of the simulator for the controller driving signal has been shown in Fig. 4.

OUTLOOK

The applications of the real time simulator are not limited to test of new algorithms and hardware. One of the possibilities is to use the simulator as an online diagnostic tool. It could work in two modes:

- In-pulse diagnostics. The driving signal can be splitted and drive the simulator and real system in the same

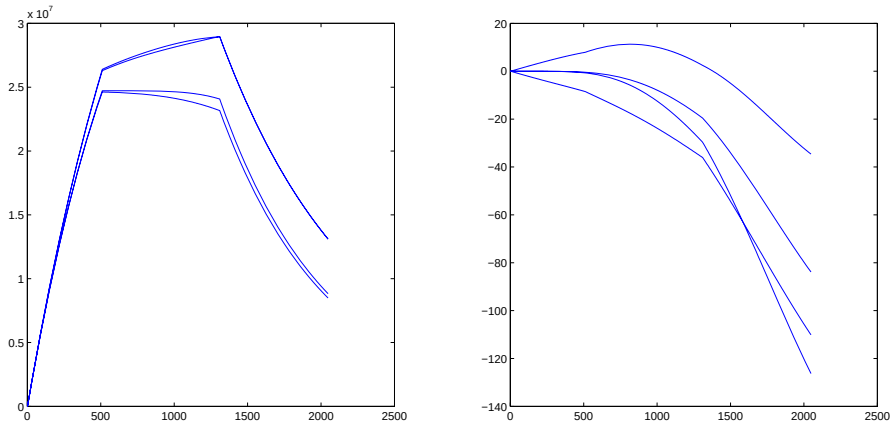

Figure 3: Simulation of 4 cavities. Left plot presents gradients. Right plot shows the phase of each cavity. On the gradient plot two upper cavities have $Q_L = 3.8 * 10^6$ and two lower cavities have $Q_L = 3 * 10^6$ Predetuning and LFD parameters are different in each cavity. Simulator was driven using internal tables [Fig. 2]

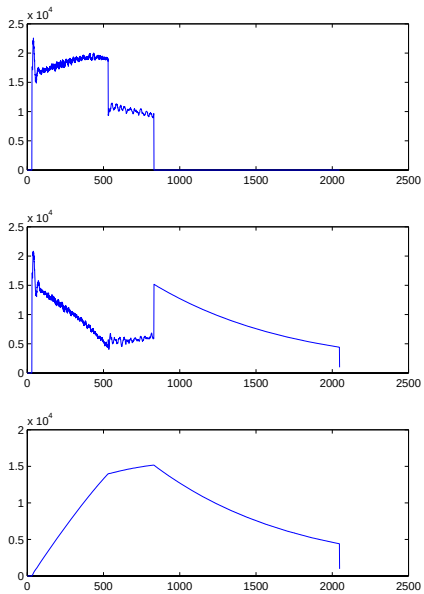

Figure 4: The response of the simulator driven by the controller. Top plot presents the input power after the klystron simulation block. Middle plot shows reflected power and the bottom plot field probe in the cavity. It is visible, that cavity filters out the noise acting like a low pass filter.

time. Assuming, that model parameters are adjusted to simulate the driven system it is possible to track the signal integrity and in case of discrepancy between the reality and simulation allow the controller to detect and handle the exception.

- "before pulse" diagnostics. It is possible to apply the driving signal to the simulator before the real RF pulse. It is especially usefull for adaptive algorithms to check if the next adaptation does not cause field quality degradation (e.g. due to corrupted input signals) instead of improvement. Such simulation has less tight time requirements because the time between pulses is in order of 20ms to 200ms.

Current development of the simulator is focused on the parameterization and automation. The goal of this effort is to allow users to build the simulated system from the functional blocks and provide toolchain for automatic code generation and compilation of the FPGA firmware and software.

REFERENCES

[1] S.N. Simrock, W. Cichalewski, M.K. Grecki, G.W. Jablonski, W.J. Jalmuzna, "Universal controller for digital RF control", Proceedings of EPAC 2006, Edinburgh, Scotland

[2] W. Giergusiewicz, W. Jalmuzna, K.T. Pozniak, N. Ignashin, M. Grecki, D. Makowski, T. Jezynski, K. Perkuszewski, K. Czuba, S. Simrock, R. Romaniuk. "Low latency control board for llrf system: Simcon 3.1", Proceedings of SPIE, vol. 5948:pp. 59482C1-6, 2005.

[3] `http://www.xfel.net`.

[4] `http://www.doocs.desy.de`.

[5] T.Schilcher "Vector sum control of pulsed accelerating fields in Lorentz force detuned Superconducting Cavities", Ph.D. thesis, Hamburg 1998

[6] "Software for Development and Communication with FPGA Based Hardware" J. Szewinski, P. Kaleta, P. Fafara, P. Pucyk, W. Koprek, K. Pozniak and R. Romaniuk, TESLA note 15, DESY 2005