

FPGA IMPLEMENTATION OF MULTICHANNEL DETUNING COMPUTATION FOR SC LINACS

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Abstract

The paper presents FPGA implementation of multichannel detuning computation for Linear Electron Accelerators. The described tool is a part of a cavity detuning compensation system which consists of a digital controller, the analog power amplifiers and the piezoelectric actuators. The previously developed algorithms were implemented in SIMCON3.1 board and allow online calculations of Lorentz force detuning only for one cavity [1]. The recent development in the field is based on pipelined computations which allow a real time detuning measurements of 8 cavities simultaneously. Moreover, the SIMCON DSP board equipped with Virtex II Pro FPGA and fast ADC channels was used to meet 10 ns latency for all performed computations. The new approach enables integrating the algorithm dedicated for cavity resonance frequency control with the LLRF control system using optical communication links. Furthermore, the programmable, multichannel function generator as well as 8-channels power amplifiers were applied to a detuning measurement subsystem. The configuration enables the possibility of online detuning computation and its active compensation for one accelerating module. The system is currently in development stage and the first results from carried out tests at FLASH [2] facility (DESY, Hamburg) using accelerating module ACC6 will be demonstrated.

COMPENSTATION SYSTEM OVERVIEW

The SC cavities operating with high gradients (~ 30 MV/m) can be deformed due to Lorentz forces. Detuned cavities reflect more RF power and therefore they need more excessive RF driving. Usually the piezoelectric actuators are used to keep constant cavity resonance frequency. However they require high voltage driving and therefore the driving circuitry must fulfil special operation requirements. The currently developed control circuit for fast frequency tuners consists of 8-channels Piezo Drivers and special control boards (see Fig. 1). The Piezo Driver units were designed using power amplifiers PB51 from APEX [3]. Moreover they are equipped with overvoltage and overcurrent circuits. The digital part of the system is based on SimconDSP controllers. The master and slave boards are used for measurements of probe, forward and reflected signals from RF probes. The measured data are used for detuning computation from each cavity in one accelerating module. Additionally, the multichannel function generator was implemented and applied for driving the Piezo Drivers. The communication between boards is performed using optical links.

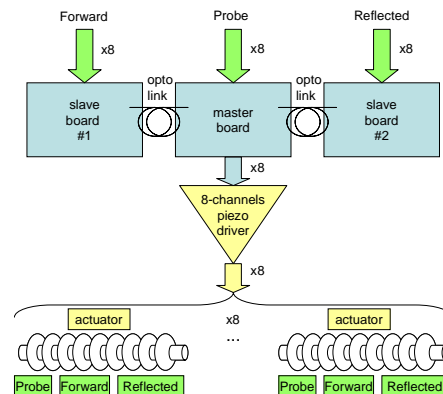


Figure 1: The block diagram of detuning compensation system.

DETUNING COMPUTATION SUBSYSTEM

The piezo control system block was implemented in xc2vp50 FPGA from Xilinx. The main part of the system is a detuning computation component. The derived detuning can be used as a feedback loop sensor that correct cavity detuning during RF pulse. The detuning of an oscillator is calculated using the cavity equation rewritten in polar coordinates [4]. In order to derive the detuning of the cavity from RF signals, one needs to measure the amplitude and the phase of the incident wave (U_f and ϕ_f) and of the field probe (U_p and ϕ_p) (see Eq. 1). The measurements need to be calibrated in a way that proper amplitudes and phases match each other. Moreover, for precise measurements it is necessary to correct the measured signals for crosstalk (incident and reflected waves calibration).

$$\Delta \omega = \frac{d\phi_p}{dt} - \omega_{1/2} \frac{U_f}{U_p} \sin(\phi_f - \phi_p) \quad (1)$$

The raw data measured using external ADCs are initially smoothed using average filters. Then data are demodulated to I (In-phase) and Q (Quadrature) components using field detection blocks. The sampling frequency of each block was set to 1 MHz. It gives four samples per period when using demodulation of RF signals with 250 kHz intermediate frequency. The distributed architecture based on fiber optic modules was used for communication between controllers [5]. The arbitrary block was added to generate the start signal for detuning computation block (see Fig. 2). Moreover, it is

used for synchronization purpose of data received from both slave boards.

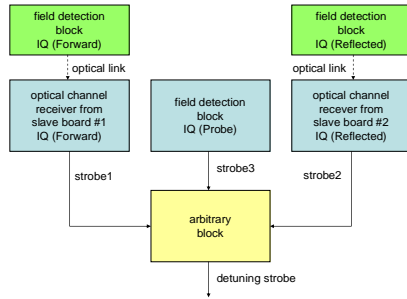


Figure 2: The block diagram of distributed architecture core.

The Main Implementation Structure

The implementation structure of detuning computation was designed to meet the multi-cavity configuration. It consists of input multiplexer, pipeline stages of the detuning algorithm and output demultiplexer. The input samples from each cavity are continuously pushed into the pipeline with system clock period. The valid signal is generated by input structure to inform the output block that valid data are presented in the pipeline. The latency of detuning computation for one cavity is equal to 36 clocks. Adequately, the latency for multi-cavity computation is the same as for one cavity but increased by the number of input channels to the multiplexer block. The additional multiplexer can be enabled for diagnostic purpose of each computation stage. The block diagram of the implemented structure is depicted in Fig. 3.

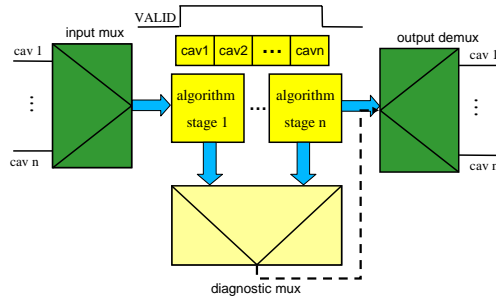


Figure 3: The block diagram of multi-cavity structure of detuning computation.

The Chosen Computation Blocks Details

The detuning equation is based on derivative of probe signal phase. The typical derivative computation seems to be a simple operation of subtraction of two samples (current and previous) multiplied by inverse value of interval time period between them. The performed measurements of probe signal phase and its derivative using typical method were very noisy. Therefore the data smoothing process was applied. The digital FIR filter was implemented for that purpose. The 32 taps length of the filter was chosen after a series of tests. The filter structure was rebuilt to meet the pipeline data from previous computation blocks. The multiplicands by coefficients

[1...-1...] were replaced by simple inverting and non-inverting buffers. The shift registers were used for collecting samples from each cavity. The implementation structure is shown in Fig. 4.

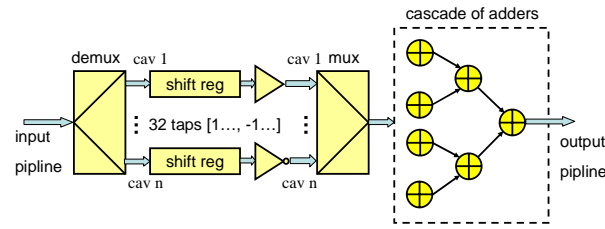


Figure 4: The block diagram of pipelined multichannel FIR filter.

The sinus and division blocks are an additional blocks for final detuning computation. The first one was implemented using memory sine approximation method with special emphasis to fact that the result should be normalized to sinus range of $[-\pi, \pi]$. Therefore the additional block for input phase normalization purpose was applied. The divider block was implemented using linear interpolator module. The input divisor is interpolated by function of $1/x$. Then the result is multiplied by dividend value. The implementation method was chosen because of the number of clock cycles needed for the computation. The latency of sinus and division blocks is 5 clock cycles. Therefore the both computations are performed simultaneously.

FPGA Resource Usage Summary

The piezo control system was compiled using ISE 9.2 designer from Xilinx. The timing constraint for the project was set to 14 ns and next to 10 ns time period of input clock. The summary of FPGA chip usage as well as achieved timing results are collected in Table 1.

Table 1: Summary of compilation tests

Resources	Usage
Slices	18465 (78%)
Flip Flops	21594 (45%)
LUTs	24427 (51%)
RAMB16s	14 (7%)
MULT18x18	23 (9%)
Timing tests	best case achievable
75 MHz	13.312 ns
100 MHz	9.994 ns

FLASH TESTS RESULTS

Described system was tested in module ACC6 at FLASH facility. The repetition rate of the RF pulse was set to 5 Hz with klystron power close to 300 kW (set point voltage of 14 MV/m). The RF pulse duration was set to 300 μ s. The single sinusoidal excitation was chosen

as a compensation pulse shape. During the first part of the tests the compensation pulse parameters (its amplitude and time advance to the RF pulse) were manually find out. The detuning for all 8 cavities was computed in FPGA. The multichannel function generator was applied for the compensation purpose (see Fig. 5).

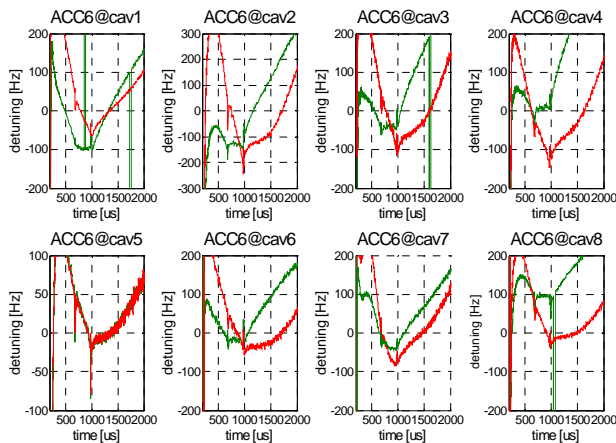


Figure 5: The Lorentz force detuning compensation in ACC6 at FLASH - without (red) and with (green) compensation.

Then the tests were repeated from set point of 8 up to 14 MV/m with single step of 1 MV/m. The dependence of compensated detuning versus pulse amplitude applied to actuator are shown in Fig. 6.

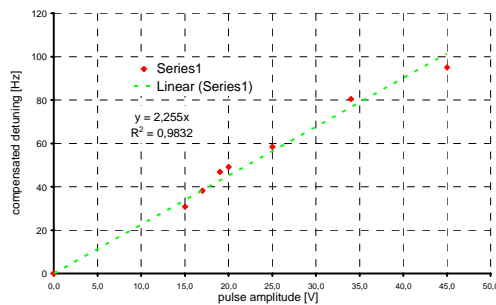


Figure 6: The dependence of compensated detuning vs. pulse amplitude for cavity 1 in ACC6.

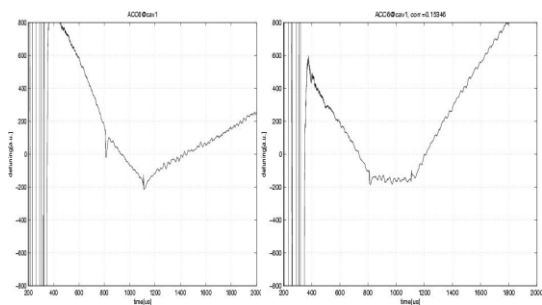


Figure 7: The automatic compensation method - without (left) and with (right) compensation.

The results from measurements were approximated by linear function with slope value of 2,3. The automatic compensation method was applied to the compensation system [6,7]. It is based on single multiplication of

measured detuning (flat top region) by the invert value of the estimated slope. The compensation result for cavity 1 in ACC6 was achieved after two correction steps (1st step 30V and the 2nd one 15V) (see Fig. 7). 300 of arbitrary units on the vertical axis corresponds to 120 Hz detuning.

CONCLUSIONS

The multi-cavity detuning computation was fitted to a single FPGA device. Its latency for 8 cavities configuration equals to 44 clock cycles. The computations were tested with system clock frequencies up to 100MHz. The detuning computation block was applied to piezo control system and then the whole system was tested in module ACC6 at FLASH. The online detuning measurements for all 8 cavities simultaneously together with active compensation of Lorentz force detuning were carrier out. In addition, the automatic compensation method for cavity 1 in module ACC6 was demonstrated.

ACKNOWLEDGEMENT

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