PERFORMANCE OF 24 CAVITY VECTOR SUM CONTROLLER WITH DISTRIBUTED ARCHITECTURE

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Abstract

The paper presents the test results of the digital vector sum control applied for 24 superconducting cavities driven by 1 klystron. The controller is based on FPGA chips and consists of multiple processing boards which communicate via optical fiber links. Flexible and scalable distributed architecture was designed and implemented to provide framework for the control algorithms. The tests were performed at FLASH (DESY,Hamburg) facility using ACC4, ACC5 and ACC6 modules. Results were compared to the existing DSP based system.

INTRODUCTION

Free Electron Lasers (FEL) are the facilities, which are able to generate femtosecond long light pulses with the wavelength of few nanometers. They are used for research, medicine and military. The most important part of such lasers is linear accelerator, which task is to provide stable, high energy electron beam. The beam is converted into the photon stream inside undulators. One of such facilities is 260 meters long FLASH laser (Free Electron Laser in Hamburg) situated at DESY research center (Fig. 1).

The linear accelerator which is part of FLASH facility consists of 6 accelerating modules. The bunches of electrons are accelerated inside 9-cell superconducting cavities filled with the electromagnetic field with the gradient of several MV/m. Each of the modules contains 8 such cavities powered from the klystron, which is source of the RF field. To get coherent laser radiation the stability of the electron beam parameters must be assured. This coverts to the stability of the amplitude and phase of RF field inside accelerating modules. The task of the stabilization belongs to Low Level Radio Frequency (LLRF) control system.

DIGITAL FIELD CONTROLLER

The LLRF control system measures the electromagnetic field inside the cavities and provides the control signal for klystron. The task requires the large number of measurement channels and appropriate computation power for data processing. In addition, small latency of the control algorithm execution is required.

The FPGA (Field Programmable Gate Array) chips are equipped with dedicated computation block, fast transmission interfaces, embedded processors and internal blocks of memory. They are capable of providing required computation power and assure small latency. The new generation of the control system is based on this chips. During the system

development, the SIMCON board family was designed. In addition to Virtex 2 Pro chip, SIMCON DSP board is also equipped with TigerSharc DSP processor, VME interface and fast optical links. It contains 10 ADC converters capable of 105 MHz sampling of the cavity field and 8 DAC converters to provide klystron with the control signal.

Figure 2: The SIMCON 3.1 system.

The basic algorithm executed by the system is presented in Fig. 3. The 1.3 GHz cavity signals are downconverted to 250 MHz, sampled by ADCs and transmitted to FPGA chip. Then demodulation of the signal is made to get I and Q components of the electromagnetic field. In case of the field control in the whole module the input calibration is performed for each input channel. Next, the vector sum of the measured field vectors is calculated.
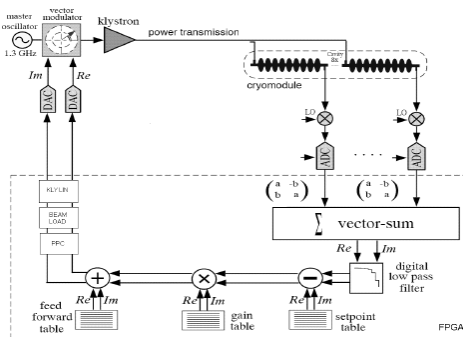

Figure 3: The algorithm performed by digital field controller.

The resulting vector is compared with the set point value to calculate error signal, which is later amplified by the proportional gain. The arbitrary Feed-Forward signal is added and the control signal is further processed by such blocks
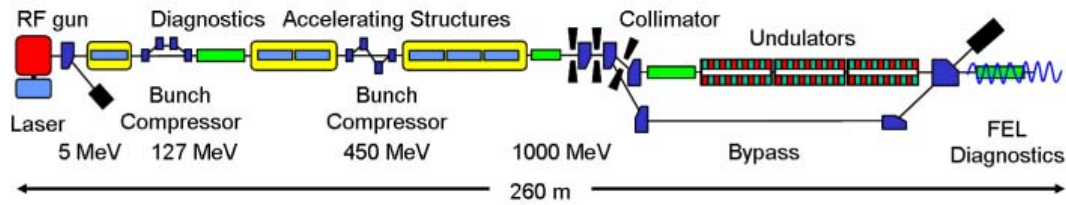
Figure 1: The FLASH facility layout [1].

as beam loading compensation, klystron linearization and other correction modules [2, 3].

STRUCTURE OF THE DISTRIBUTED SYSTEM

To control one accelerating module connected to one klystron (for example ACC1 module in FLASH) it is required to sample 8 analog probe signals. In case of RF station which consists of 3 accelerating modules connected to one klystron (for example ACC456 module in FLASH) 24 analog signals have to be sampled. This task cannot be performed by one FPGA board [4]. The partial vector sums have to be calculated by different monitoring systems and sent using fiber links to the main unit. The structure of the proposed system is shown in Fig. 4.
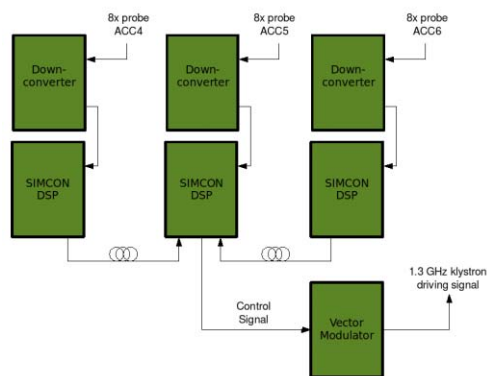

Figure 4: The structure of the distributed system.

24 analog signals proportional to the field level in each of the SC cavities are connected to 3 downconverters. After the downconversion to the 250 kHz the signals are sampled by 3 SIMCON DSP systems. Each of them is calculating partial vector sum of the field in the module according to algorithm presented in Fig. 3. The vectors calculated by slave systems are transmitted to the master board using fiber links. The control signal calculation is based on the received data and the resulting signal is provided for the vector modulator. After the modulation it is amplified in the amplifiers and the klystron.

COMPUTATION MODULE

To implement the computation modules of the described system, the universal mathematical library for high energy physics experiments was used. It consists of modules, which allows to perform basic mathematical operations using saturated, fixed point arithmetic. In such applications as accelerator control systems, the overflow on any internal value can lead to unexpected results including permanent damage of the device. The library defines the mathematical operators for the complex numbers (I-Q vectors), which simplify the process of algorithm implementation [5].

TRANSMISSION MODULES

The distributed system using described architecture requires the transmission links with the bandwidth of at least 200 Mb/s with the low and constant latency. It is related to the requirements concerning the stability of the closed feedback loop. Therefore the point to point fiber links have been used.

The transmission module is using fast RocketIO blocks placed in the fabric of the Xilinx FPGA. It supports different communication protocols, but they mostly contain features unnecessary for the described application, which reduce the bandwidth or increase the latency. Therefore the raw data transmission was used. To minimize the latency of the transceiver special low latency mode was used [6]. Fig. 5 shows the latency of the transmission as a function of the transmitted data [4].
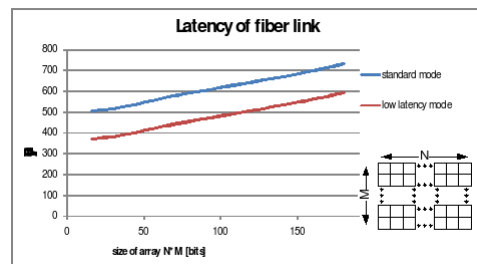

Figure 5: Latency of the data transmission [4].

TEST RESULTS

The ACC4, ACC5 and ACC6 modules in FLASH are controlled by the old generation system based on the DSP

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processors. The system is at the limit of the time for computation and available resources - no additional algorithms can be implemented. To compare old system with the system described, the measurements of the beam energy stability were performed. The results of the measurements are shown in Fig. 6 and Fig. 7.
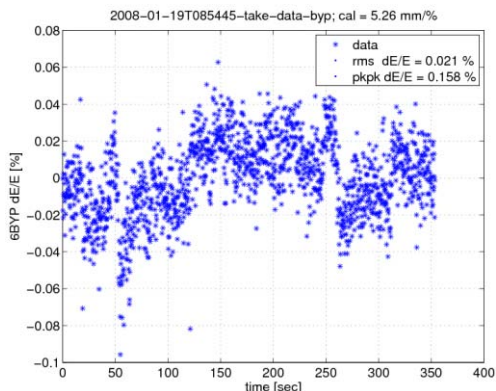

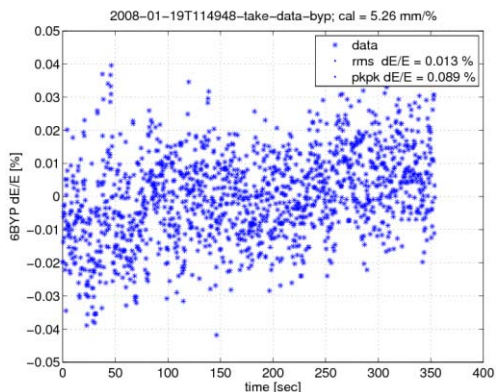Figure 6: Beam energy stability measurement using old DSP base system.

Figure 7: Beam energy stability measurement using FPGA base system.

The use of the described system resulted in performance improvement of the pulse to pulse electron beam energy stabilization. The improvement is visible both on rms error of the measured energy and peek error value. The errors were almost two times smaller than for the old generation system.

SUMMARY

The paper presents the architecture of the distributed measurement and control system. In the shown example it was used to implement multicavity field controller which allowed to achieve the performance improvement in comparison with the currently used control system. The system is scalable in terms of the input channel count, so it can be used in many different applications. Thanks to the high resources count it can be used as the universal platform for the algorithm development.

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