LLRF ELECTRONICS FOR THE CNAO SYNCHROTRON

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Abstract

CNAO, The Italian National Centre for Oncological hAdrontherapy in Pavia will start its test phase in 2008. Treatment is based on beams of proton and carbon ion provided by a 78 meters circumference synchrotron. Particle acceleration is done by a unique VITROVAC load RF cavity operating at a frequency ranging from 0.3 to 3MHz and up to 3kV peak amplitude.
In order to control this cavity a digital LLRF system has been designed at LPSC. It is based mainly on Digital Signal Processors (DSPs), Field Programmable Gate Arrays (FPGA) and Direct Digital Synthesizers (DDS). The LLRF system implements both cavity control and beam control capabilities in a compact, remotely programmable and configurable, Ethernet controlled electronic module. It also allows an easy regulation loop tuning, thanks to an embedded acquisition system that stores all input and output signals during a given acceleration cycle.

INTRODUCTION AND REQUIREMENTS

LPSC was contacted by the CNAO foundation [1] in order to develop a LLRF electronics for the synchrotron in 2004. After a state of the art study, the choice for an all digital LLRF was made, based upon that developed for CERN's LEIR [2]. The LLRF shall provide to the cavity a sinusoidal signal with a frequency varying from 300kHz to 4MHz with a resolution better than 10Hz. The sine amplitude needs to be controlled to insure a 1% or 2Vpp stability of the gap voltage in the 10V to 3kV range. The LLRF must also control the vitrovac current in order to keep the cavity tuned (less than 6° phase difference between grid and gap voltages). Beam control loops shall also be implemented in order to damp beam longitudinal and radial oscillations. Precomputed acceleration cycle curves will be transmitted in real-time by the CNAO Control & Command to the LLRF.

GENERAL DESIGN DESCRIPTION

The CNAO LLRF electronics is built around a single low cost FPGA (Xilinx XC3S400) that handles all I/O interfaces, two DSP (ADSP21262) and an Ethernet daughter board for the slow control (figure 1).

In order to enable the computation of I/Q parameters, the three following RF analogues signals are sampled at a variable rate with 16 bits fast ADC (up to 80MHz) :

- The Cavity Gap voltage
- The Cavity Grid voltage
- The Σ signal of the longitudinal beam pickup

The four radial beam position pickup signals connected to the LLRF board are already analogically processed and are therefore read by slower ADC. Out of those, two are located in low dispersion regions and two in high dispersion regions. Several combinations of those pickup can be taken into account for beam radial position calculation.

Revolution frequency, cavity voltage amplitude, polarisation current, beam phase and radial position curves are transmitted asynchronously by the CNAO Control & Command through five 32 bits serial links (GFA links) with a maximum parameter update rate of 300kHz. Since no more than 24 bits are needed for parameter coding, 8 bits per link are reserved for real time control purpose such as loop activation, timing signals, etc...

The signal provided to the cavity driver is a sinusoid generated by a commercial DDS (Direct Digital Synthesizer), the amplitude of the sine wave is controlled by a voltage controlled logarithmic amplifier in order to improve low voltage sensitivity (needed for trapping/bunching). Two other identical DDS are used to provide a beam synchronous clock and a Master clock that runs at 16 times the frequency of the revolution frequency.

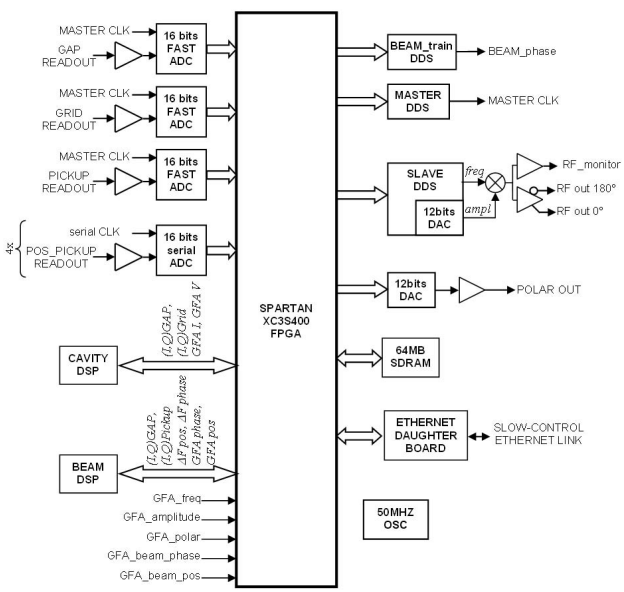

Figure 1 : Block diagram of the CNAO LLRF

I/Q COMPUTATION

In order to perform the various regulations, the digital LLRF needs to extract the following information from the input signals :

- cavity gap voltage amplitude
- cavity gap to grid phase
- Beam pickup to cavity gap phase

Those measurements are easily derived from the I/Q representation of the RF signals. The architecture of one computing module is described in Figure 2.

Cavity or pickups signals are sampled at a sampling frequency multiple of the revolution frequency (F_{Rev}). For each RF period, the FPGA provides one set of I/Q parameters by multiplying each sample by sin/cos values stored in **L**ook **U**p **T**ables (LUT) and by accumulating the result. This implementation is slightly different from the classical CIC filter since the Integrator/Comb filter is here replaced by a hardware accumulator reseted at each RF period.

For this application, the sampling clock is continuously provided by a Master DDS running at sixteen times the revolution frequency ($16xF_{Rev}$). Equations 1a and 1b, give the I/Q values computed for a sinusoidal input signal of amplitude A and phase φ.

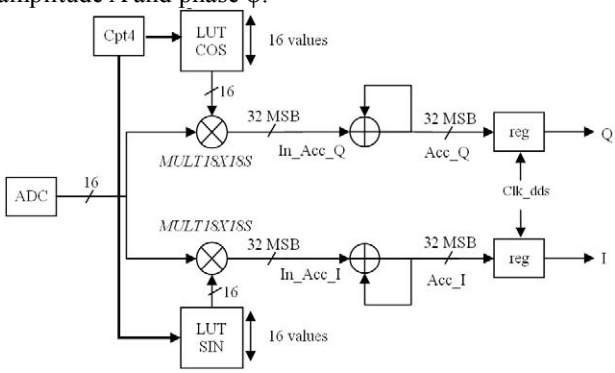

Figure 2 : I/Q measurement implementation

$$I=\sum_{n=0}^{15} A\cdot\sin(2\Pi\frac{n}{16}+\varphi)\cdot\cos(2\Pi\frac{n}{16})=8A\cdot\sin\varphi \quad (1a)$$

$$Q=\sum_{n=0}^{15} A\cdot\sin(2\Pi\frac{n}{16}+\varphi)\cdot\sin(2\Pi\frac{n}{16})=8A\cdot\cos\varphi \quad (1b)$$

CAVITY CONTROL

The control of the CNAO cavity is done by a dedicated DSP that acts on 2 signals, the RF voltage amplitude and the cavity tuning current. The absolute RF frequency, is directly transferred from the GFA frequency input to the three DDS in order to minimise delays. The master DDS clock frequency, however, is multiplied by 16 by the FPGA itself, during the transfer process.

Thanks to the I/Q modules, the RF amplitude is computed using equation 2a :

$$RF_{amp}=\sqrt{I_{Gap}^2+Q_{Gap}^2} \quad (2a)$$

The phase difference is computed by the following approximation (Equation 2b), which is consistent since the grid to gap voltage is kept close to zero by the tuning regulation.

$$\Delta\varphi\simeq\tan(\varphi_{Gap}-\varphi_{Grid})=\frac{Q_{Grid}\cdot I_{Gap}-I_{Grid}\cdot Q_{Gap}}{I_{Grid}\cdot I_{Gap}+Q_{Grid}\cdot Q_{Gap}} \quad (2b)$$

A simple PI corrector is used to control the cavity amplitude voltage where as a more complex PID has been implemented for the cavity tuning loop. Additional protection of the cavity is provided by limiting the tuning loop contribution to ±10% of the pre-calculated current (received on a GFA link).

BEAM CONTROL

Beam control is assigned to a second dedicated DSP. Two control loops are implemented (phase and radial loops) that act as correctors of the revolution frequency provided by the GFA.

Phase loop

Phase loop reduce synchrotron oscillation and damp beam instabilities. The input of the loop is the phase difference between the cavity gap voltage and the beam pickup signal. At first, software rotation of the beam I/Q coordinate is done in order to take into account delays (cabling) and pickup position in the synchrotron with respect to the cavity. The rotation angle is the sum of a frequency dependant angle for the delays and a fixed angle for the position of the phase pickup. Computer efficient rotation is performed thanks to a sine LUT and first order trigonometric approximations.

Then, in order to calculate the resulting beam phase a stable sine approximation was used (Equation 3). The computed phase feeds a IIR first order high-pass filter, and is multiplied by the phase loop Gain before being added to the programmed revolution frequency in the FPGA (figure 3). Phase loop period can be as low as 5µs.

$$\Delta\varphi_{Beam}\simeq\frac{Q_{Beam}\cdot I_{Gap}-I_{Beam}\cdot Q_{Gap}}{\sqrt{(I_{Gap}^2+Q_{Gap}^2)\cdot(I_{Beam}^2+Q_{Beam}^2)}} \quad (3)$$

Radial loop

Radial loop is used to correct errors in predicted optimal RF frequency. We are using normalized outputs of four radial pickups which are directly proportional to the beam radial position. The loop is based on a PI biquad filter implementation. Since optimal PI parameters depend on the synchrotron frequency, Direct Form I implementation of the biquad filter is used as it enables

parameters variations during cycle time without affecting the filter stability. The resulting radial loop frequency contribution is then added to the revolution frequency in the FPGA. Radial position bandwidth is much lower than beam phase and a radial loop period of 100µs is enough to ensure good correction.

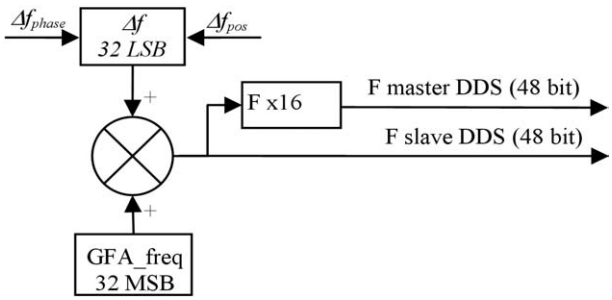

Figure 3 : beam loop frequency contributions

SLOW CONTROL

The CNAO LLRF board features an Ethernet controller board that provides commodities such as:

- Remote configuration of the FPGA and the DSP,
- Control of the embedded data acquisition system.

These functionalities are very useful in a debugging phase, where the processing algorithms have to be changed or tuned often and when a good monitoring of the system is required. Therefore, with the exception of the Ethernet daughter board, no non volatile memory is implemented on the board. The DSP and FPGA files are stored on the controlling computer.

The microcontroller boots at power up time and provides a TCP socket server that allows a slow control computer to open a client socket with the board. The communication with the board is performed via a custom protocol.

Remote FPGA configuration

The FPGA configuration file has to be sent through the communication link; the microcontroller receives the data, serializes and transfers them to the FPGA in real time. This process takes about 2 s. When it is over, the FPGA is fully functional and ready to perform.

Remote DSP configuration

Among the functionalities the FPGA features, one of them is to provide logic for DSP booting and settings, it consists of:

- One SRAM memory block large enough to fit one DSP program at a time.
- Two memory block (512 * 32 bit) for holding parameters, one per DSP.
- Individual DSP reset control

The DSP are booted one at a time by loading the targeted DSP program in the boot memory, via the slow control interface, and de asserting the reset signal. The parameters memories have to be filled with adequate values prior to the booting of the DSPs. Relevant parameter can be PID factors, timeout values, gains …

Embedded data acquisition system

This system can record 16 parameters with a user selectable:

- period in step of 3 µs
- Offset from the start of acceleration cycle, also in step of 3 µs
- Number of samples

The memory depth was selected in order to be able to record a full acceleration cycle at the maximum sampling rate. The recorded parameters are:

- I/Q for gap, grid and phase pickup
- The 4 beam position signals
- Absolute frequency, and both loop contributions
- The DSP computed beam phase
- Cavity control signals (polarisation and RF amplitude)

These data are stored in real time (during acceleration) in the SDRAM by the FPGA. Since the DSPs are not involved in this process, using this system is costless with respect of the loop latencies or the processing power. Once the acquisition is done, the slow control computer can download the data.

CONCLUSION

The CNAO synchrotron being still under construction and in order to speed up the commissioning, LLRF electronics has been first tested and validated on the cavity alone during year 2007. Then the beam loops were successfully tested with minimum system modifications on the CERN PSB [3]. At this point the hardware is ready for full operation.

ACKNOWLEDGEMENT

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