THE SSRF TIMING SYSTEM

L. Y. Zhao, C. X. Yin, D. K. Liu
SINAP, P. O. Box 800-204 Shanghai 201800, China

Abstract

In Shanghai Synchrotron Radiation Facility (SSRF), various equipments in the 150MeV Linac, the full energy booster and the 3.5GeV storage ring need to be triggered and synchronized by a low jitter timing system. An event system, based on distribution network, is implemented in the SSRF timing system. In this paper, software and hardware structure of the SSRF timing system are described and system performance is presented.

INTRODUCTION

In general, the main task of timing system is to generate and distribute all kinds of hardware trigger pulses and synchronized clocks, which are needed by various devices in Linac, Booster and storage ring.

SSRF timing system is a challenging design. For hardware design, the triggered devices are distributed in various locations of SSRF complex, the specifications of these triggers are highly different, and some hardware interlock signals for HV (high voltage) devices are needed to be integrated into the SSRF timing system. For software design, SSRF timing system must integrate into the SSRF control system, which is based on EPICS platform.

We selected the advanced event system [1] as the basic structure of SSRF timing system. The main hardware modules come from Micro-Research, and additional devices are customized. A compact fibre network is designed for timing signal distribution. From the beginning of software design, we decided the software of hardware testing bench, the software of machine commissioning, and the software of machine normal operation are based on a uniform EPICS application environments, and supported all hardware modules.

SYSTEM OVERVIEW

The operating frequency of SSRF injector is 2Hz, so the period of SSRF timing system is 500ms that is synchronized with AC line. For the SSRF hardware device, modulators, klystrons, E-Gun in Linac are firstly triggered; then the injection kicker and septum, RF system, power supplies in Booster are trigger; at last, the extraction bump, kickers and septums in Booster and injection kickers and septums in storage ring are triggered. The sequence of SSRF timing system is shown in figure 1. T_0 is the start point of timing system; T_{LEX} is the point of Linac extraction; T_{BIN} is the point of Booster injection; T_{BEX} is the point of Booster extraction; T_{RIN} is the point of storage ring injection; T_G is the point of E-Gun triggering.

SSRF timing system also provides three clocks that are synchronized with RF clock. The division factors between these three clocks and RF clock are shown in Table 1.

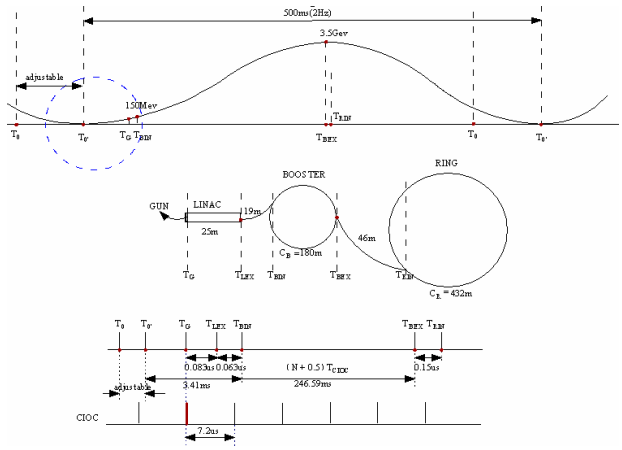

Figure 1: The sequence of SSRF timing system.

Table 1: Synchronized Clocks

Clock	Relation With RF	Frequency of Clock
RF Source	-----	499.654MHz
Booster Revolution Clock (BROC)	RF/300	1.666MHz
SR Revolution Clock (SROC)	RF/720	0.694MHz
Coincidence Revolution Clock (CIOC)	RF/3600	0.1388MHz

HARDWARE STRUCTURE

Fibre Network

SSRF timing system uses multilevel OM3 multimode fibre to build timing signal distribution network. In order to reduce hardware device of timing system, two levels' star network is implemented which is shown in figure 2.

To decrease the jitter and phase shifting of timing output signal, the distance between timing signals generator and RF source must be as short as possible. So the station of timing generator is placed in the RF station of the storage ring, which installs event generator (EVG)[2] and fibre FANOUT. EVG connects RF clock and 50Hz AC clock, and generates event codes and three synchronized clocks. After distribution in fibre network, event codes and three synchronized clocks are decoded by event receivers (EVR) to generate hardware signal. In order to align all EVR output signals, the length of fibre in each level should be equal.

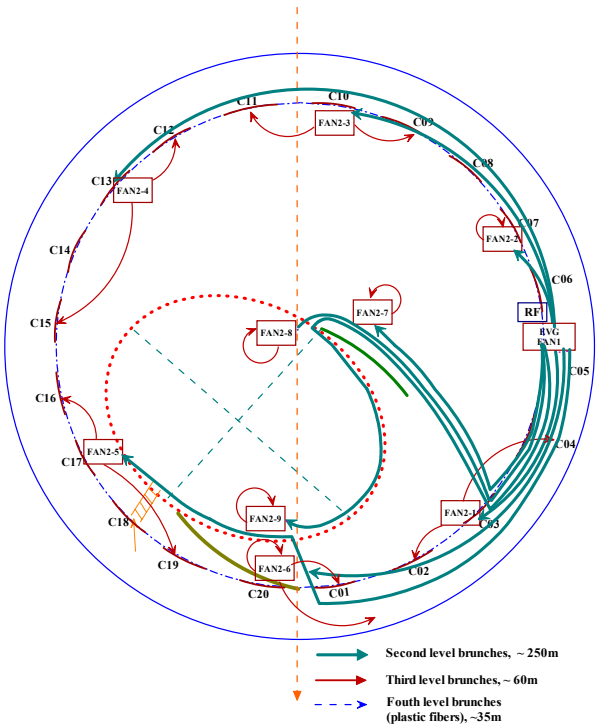

Figure 2: Distribution network of SSRF timing system.

Commercial Modules

The Micro-Research products are chose for the main timing devices, which include EVG-230, EVR-230, Fout-12, OTB-200, TTB-200, GunTX-200, GunRC-200 and UNIV-TTLIN-IL. In our case, the delay step of EVR is 8ns (four times of RF period); the delay step of GunTX-200 is 2ns. So the delay resolutions could satisfy all requirements. All modules except GunRC-200 are VME modules, which are installed in local control or beam diagnosis station. GunRC-200 is installed in E-Gun cabinet. The testing results of EVG, EVR and GunTX are presented in the following section.

Customized Modules

Customized modules are made in-house, which are single-mode O/E converter, 50Hz TTL signal converter, input interlock signal converter. Single-mode O/E converter converts EVR optical output signal to TTL signal. 50Hz TTL signal converter shapes 50Hz sine signal to TTL square signal. Interlock signal converter generate TTL signal according to input interlock switch status. All customized modules are the same size (19U width and 1U height).

SOFTWARE STRUCTURE

The software of SSRF timing system is divided into two parts. The software to control hardware is run as IOC under EPICS base 3.14.8.2 and vxWorks 5.5.1, and the software to control injection and bucket selection is run as OPI under Matlab and Linux.

For IOC software, we design the new records, device supports and hardware drivers for all modules. And we developed special low-level codes to support bucket selection.

For OPI software, we developed control panels by EDM, and cooperate with physics group to develop bucket selection software. The detailed structure of bucket selection software is described below.

In additional, the software of testing bench to measure timing system's phase shifting is run under Matlab and Windows XP.

Bucket Selection

Event codes in EVG's sequence RAM are broadcast with 125MHz event clock, EVR and GunTX output are generated by these decoded event codes. So bucket selection is realized by setting delay steps of event codes in EVG's sequence RAM and GunTX.

Figure 3 is an example to calculate the delay steps for No.11bucket. 4 divide the bucket number, so the integral result is the delay step of event codes and the remainder is the delay step of GunTX. In this case, the delay step of event codes is 2, and the delay step of GunTX is 3. By using this mechanism, the delay steps of all EVRs' output pulses are fixed, and not needed to adjust.

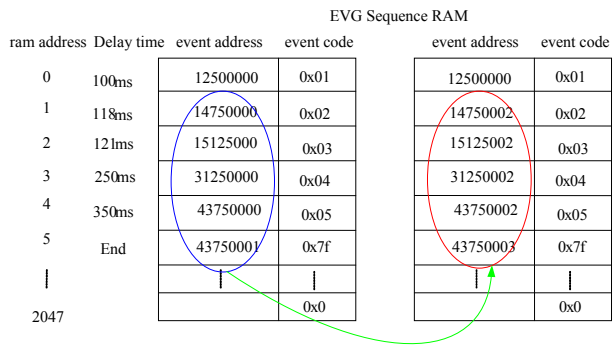

Figure 3: Example of bucket selection.

The steps of SSRF bucket selection is below:

- Bucket selection software monitor EVG sequence RAM run status by CA monitor.
- When EVG sequence RAM idle, Bucket selection software stop EVG sequence RAM.
- Bucket selection software sets desired bucket number in EVG IOC and GunTX IOC, and sets trigger time in GunTX IOC.
- IOC software calculates the delay steps.
- Bucket selection software restarts EVG sequence RAM.
- By VME interrupt mechanism, GunTX IOC software automatically stops trigger output based on input trigger time.

TESTING AND COMMISSIONING

Before the commissioning of SSRF, we development a testing bench to test all modules of timing system, including EVG, EVR GunTX, GunRC, single-mode O/E converter, 50Hz TTL signal converter and input interlock signal converter. The test contains jitter (in short term) and phase shifting (in long term) for all modules outputs.

In the SSRF commissioning, we measured timing system's performance (jitter) by WCM output.

Testing Bench

According the testing result, the jitter (RMS) of all modules outputs relative to RF source is 21ps; the jitter (RMS) of GunRC output is 10.7ps. Both of them satisfy the machine requirements.

For the phase shifting test, we developed a special testing bench, which contains oscilloscope, GPIB interface and thermal detector. The testing bench is run under Matlab and Windows XP, customized phase detecting algorithm is also realized in Matlab. The phase shifting of EVR, fibre, GunRC and customized O/E are tested. The results are shown in Table 2.

Table 2: Results of Phase Drift Tests

	Phase Shifting
OM3 Fiber	24.6ps / ℃•km
EVR	26.4ps / ℃
GunRC	0.6ps / ℃
Customized O/E	297ps / ℃

Commissioning

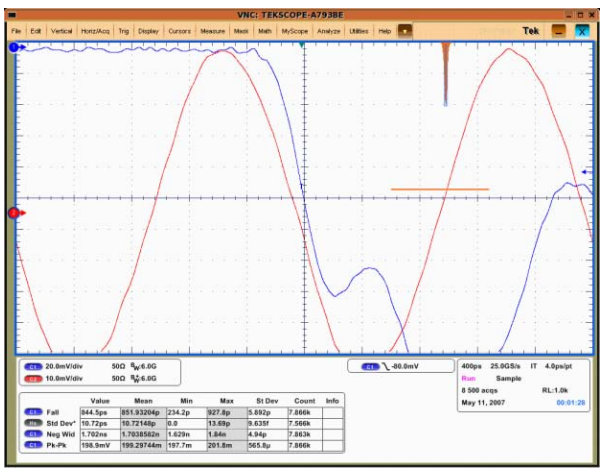

Figure 4: The jitter of WCM output.

The jitter (RMS) of Linac WCM output relative to RF source is 9.2ps, which is shown in Figure 4.

This testing result represents the jitter between RF source and Linac extraction beam, which could satisfy the machine requirement.

CONCLUSION

Currently, SSRF timing system can satisfy all machine operating modes, and are helpful for commissioning. The operating status of SSRF timing system proves that event system is a reasonable selection for timing system. In future, the hard timestamp will be developed in SSRF timing system.

ACKNOWLEGEMENT

During our design of software and hardware, we get a lot of help from experts in SLS, DIAMOND, Micro-Research, especially Dr. T. Korhonen gave us lots of valuable suggestion, and J. Pietarinen communicated with us about Micro-Research products. We appreciated for their sincere support.

REFERENCES

[1] T. Korhonen, M. Heiniger, TIMING SYSTEM OF SWISS LIGHT SOURCE, EPICS'08, San Jose, California, 2001, FRAT004, p.638-640.

[2] J. Pietarinen, Event System Manual version 2.01, 14th November 2002.

[3] Martin R. Kraimer, Janet Anderson, etc, EPICS:IOC Application Developer's Guide Release 3.14.8, 02-DEC-2005.