TIMING SYSTEM OF THE NEW ELETTRA INJECTOR

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Abstract

A new timing system has been developed to operate the new injector for the Elettra storage ring. It implements a versatile injection system to support standard and exotic fillings as well as the top-up mode of operation. Based on an in-house developed programmable counter VME board, the system provides all the needed triggers by the pre-injector LINAC, the booster injection, the booster ramping system, the booster extraction, and the SR injection. An overview of the system architecture and functionality is described and the performance of the board is reported. All the trigger signals are distributed to the timing clients by means of optical links.

SYSTEM SPECIFICATIONS

The timing system of the new Elettra injector has to provide trigger signal to drive:

- The thermo ionic gun
- The power amplifier of the 100MeV linac
- The booster injection fast magnets KIB & SIB
- The booster magnet power converters
- The booster extraction fast magnets KEB & SEB
- The storage ring injection fast magnets KISR & SISR
- The RF cavity ramp
- The diagnostic systems

The main goals for the new injector are:

- Storage Ring (SR) Refill: refill the SR at desired energy (0.7-2.4 GeV) from zero
- Frequent injection: restore the nominal operating current after it is decreased to a minimum value (beam line shutters closed)
- Top-Up: operate the SR in top-up mode i.e. maintain the current in a short range with frequent injection of low charge with beam line shutters opened.

The Elettra storage ring harmonic number is 432 while the booster one is 198; the preinjector can produce single or multibunch beam. Due to the speed of booster injection & extraction system, a maximum of about 200 ns bunches train length can be successfully operated. A typical bunch train length for the preinjector is 120ns (i.e. 60 bunches)

The Elettra standard operating mode uses a filling between 90 and 95 %.

For these reasons to fill all desired SR bucket we need more than one booster cycle to fill the SR once.

To operate the SR in top-up mode we need to choose the bucket in which inject each single bunch; to obtain this feature it is necessary to delay all the triggers at the same time by the same value.

With respect to the systems we need to trigger, we identified three trigger signal families, each one with different characteristics:

1. Slow signal trigger accepting high jitter (<20 ns)
2. Medium signal trigger accepting medium jitter (< 2 ns)
3. Fast signal trigger accepting low jitter (<200ps).

Considering the maximum jitter allowed for the first two triggers, they can be programmed with 20ns steps; while the low jitter trigger can be programmed with a 2 ns step.

The choice of the media to transmit the trigger from the source to the triggered system was between coaxial cables and fiber optics. We have chosen the second one in order to reduce the effects of EMI.

To transmit the trigger family 1) we have chosen a FOP fiber optic due to easy assembly and low costs. For trigger family 2) we chose a multimode 65/125 fiber optic driven by common transmitters used to build 100 Mbaud Ethernet network.

To transmit the low jitter triggers the media was also a MM 65/125 fiber optic but for the driver we have chosen a Gigabit Ethernet component transmitting the machine RF clock with a phase modulation for the trigger. In this way also a local RF clock is available to drive further delay board if needed.

PDELAY BOARD

The board generating the trigger signals has six channels, each of them controlled by a programmable counter.

Two channels are controlled by fast 16bit counters using a 500 MHz clock to generate the fast triggers with a 2ns delay resolution. The last 4 channels generate delay with 20ns resolution; they are controlled by 24 bit counters using a 50 MHz clock obtained from the 500MHz main clock divided by 10. The pulse length of these pulses is also programmable with 8 bit counters with 20 ns steps.

The fast 500MHz counters are realized as piggy-back units one per channel so the same components could be used stand alone or in other projects.

The main board supplies these counters with clock, the programming parallel bus and the function mode bits.

Each of these counters supply the main board with a end of count signal that can be used as trigger for the other channels.

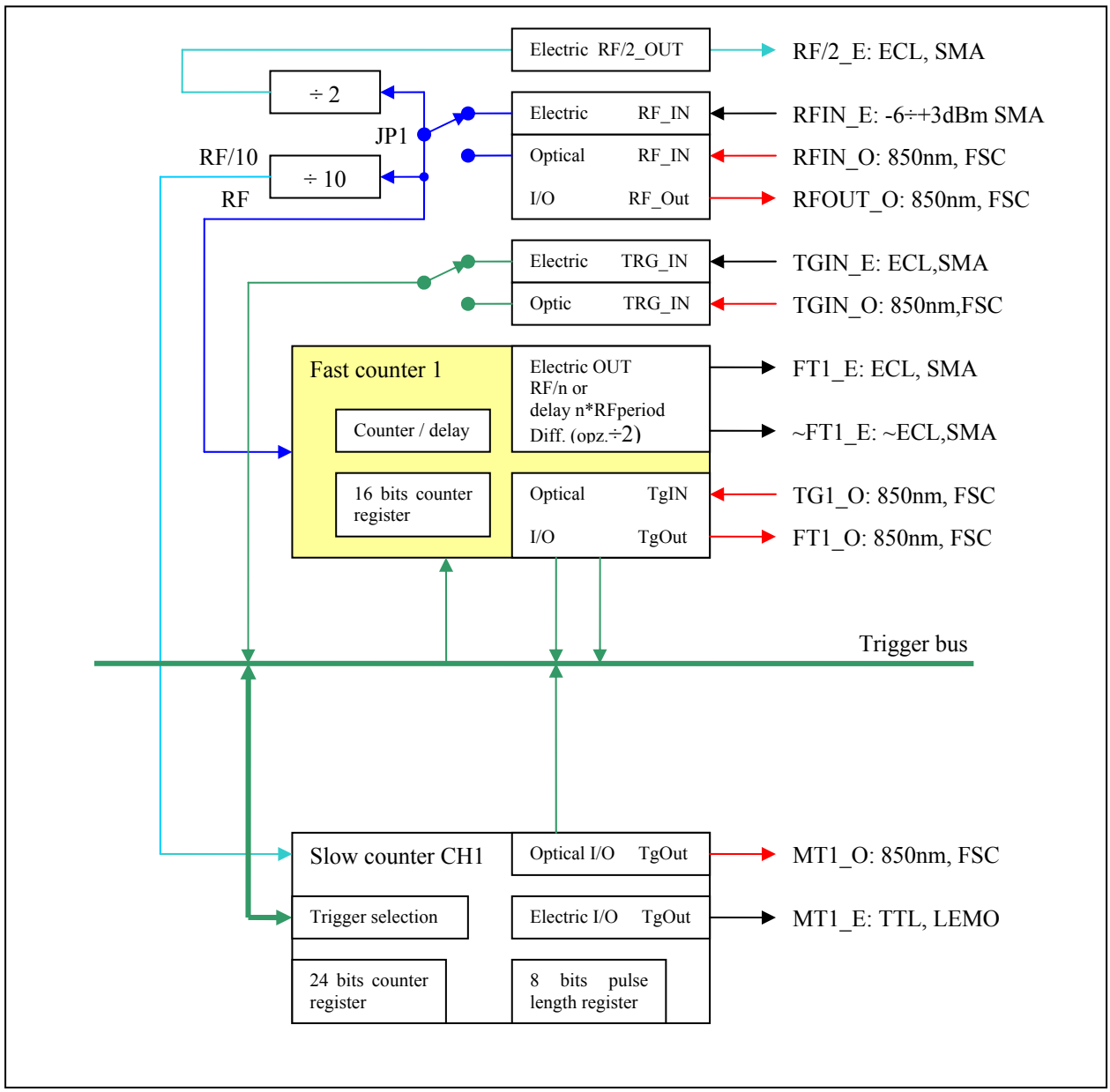

Figure 1: Block diagram of the programmable delay board: each board can hold up to two Fast counter piggy back and has four slow counter.

The fast counter modules can be used in “delay mode” to generate a delayed pulse with respect to the counter trigger or in “counter mode” to divide the clock by a fixed programmable module.

The slower counters, using a 50 MHz clock, are realized in a CPLD (Lattice LC4384V-35FN256). This CPLD implements also the trigger logic between the 6 channels making possible to start a channel after another one and so on.

Furthermore the same IC implements also the VME interface of the board and all the registers needed to program the counters.

For each channel we can choose between electric or optical output to match the requirement of the application.

Nine boards properly configured and programmed make it possible to generate all the necessary triggers to drive the linac klystron and the machines (preinjector, booster, SR)

FUNCTIONS IMPLEMENTATION

The requirements in the generation of the trigger are:

1. Each pulse has to be synchronous with the 500 MHz RF clock driving the RF cavity
2. The trigger pulses have to be synchronous with the main power supply frequency (50Hz).
3. It has to be possible to choose which of the 432 bucket of the SR will be filled

Given the harmonic number of the SR (432) and of the booster (198), the two revolution clocks will be coincident every 4752 RF cycle (9.504 μs). This period is

called the coincidence clock (CC). After this period we will find the two rings in the same bucket position.
The first requirement is obviously satisfied using as counter's clock the RF signal of the accelerator.
To satisfy the second requirement every trigger is generated with the first CC pulse after the detection of a zero crossing of the mains, supplied by a line trigger board.
If the 1st bucket is filled with a bunch fired after the CC pulse, a bunch fired with a 2 ns delay will fill the 2nd bucket and so on, by increasing the delay, each SR bucket can be filled.
After a proper setup of the pulsed fast magnets and booster ramp start triggers with respect to the master CC, we found that if the gun trigger is simply delayed by 2 ns steps after a while the gun will fire the bunch when the machine is not ready to accelerate it and hence also the other triggers have to be moved.
To minimize the number of times triggers have to be reprogrammed in order to reach a predefined bucket, a little trick was used. The first channel of the timing board generates a CC pulse synchronous with the RF and therefore with the SR; on the second channel of the same board a delayed CC pulse is generated with 2ns step and this trigger is used to generate all the triggers needed by the machine.It is clear that in this way, by changing only a single timing parameter, all the optimization is time shifted exactly when needed.
There are three main trigger signals, the gun trigger (GT) that fires the gun, the Start Injection (SI) that starts all the sequence of triggers to inject the beam in the booster, the Start Extraction (SE) that starts all the sequence of triggers to extract the beam from the booster and to inject it into the storage ring.
Since we can operate the pre-injector without injecting the beam in the booster, some trigger signals are available even if there is no SI trigger. These triggers start the thyratron and the RF pulse in the LINAC amplifier, the acquisitions of beam loss monitors, scintillation screens, and low energy transfer line beam position monitor.
The first main delay we can program is the SI delay, that is the delay between the CC trigger and the SI. The SI trigger starts the subsequent triggers:

1. KIB Booster Injection Kicker
2. SIB Booster Injection Kicker
3. Bending ramp start
4. Quadrupoles ramp start
5. Sextupoles ramp start
6. Correctors ramp start
7. BPM booster
8. Tune measurement
9. RF ramp start
10. Bumper start

The second main delay we can program is the SE delay, that is the delay between the CC trigger and the SE. The SE trigger starts the subsequent triggers:

1. KEB Booster Extraction Kicker
2. SEB1 1st Booster Extraction Septum
3. SEB1 2nd Booster Extraction Septum
4. KISR Storage ring Injection Kicker
5. SISR Storage ring Extraction Septum
6. High Energy transfer line BPM
7. DCCT

SYSTEM LAYOUT

All the trigger signals are generated in three VME crates, each one serving one part of the machine.

The first VME crate is located in the pre-injector service area; it generates the coincidence clock (CC), the main SI and SE trigger, the gun trigger, the trigger to drive the linac power amplifier and some triggers used by the diagnostics systems in the low energy transfer line.

The second VME crate is located in the booster service area; it is driven by the SI trigger and it generates the triggers used by the injection into the booster, to start the ramp of the booster magnets, the ramp of the booster RF cavity and to start the bumpers used in the extraction at high energy.

The third VME crate is located in the storage ring service area; it is driven by the SE trigger and it generates the triggers used to extract the beam from the booster, to inject the beam into the storage ring and some trigger used by the diagnostics system in the high energy transfer line.

The distribution of the trigger to the driven equipment is obtained using fiber optic media to avoid EMI.

CONTROL SOFTWARE

A linux device driver has been developed to provide board resources both for real time (RTAI) and user space applications.

A real time module is in charge to modify shot by shot the injected bucket and, at the same time, to control, through a real time serial link, the bunch train length and the grid voltage in order to control the injected charge for top-up injection mode. This way the timing Tango server integrating the board into the booster control system will permit to develop algorithms in the foreseen top-up mode operation of the injector.