KLYSTRON "EFFICIENCY LOOP" FOR THE ALS STORAGE RING RF SYSTEM

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Abstract

The recent energy crisis in California has led us to investigate the high power RF systems at the Advanced Light Source (ALS) in order to decrease the energy consumption and power costs. We found the Storage Ring Klystron Power Amplifier system operating as designed but with significant power waste. A simple proportional-integrator (PI) analog loop, which controls the klystron collector beam current, as a function of the output RF power, has been designed and installed. The design considerations, besides efficiency improvement, were to interface to the existing system without major expense. They were to also avoid the klystron cathode power supply filter's resonance in the loop's dynamics, and prevent a conflict with the existing Cavity RF Amplitude Loop dynamics. This efficiency loop will allow us to save up to 700 MW-hours of electrical energy per year and increase the lifetime of the klystron.

1 INTRODUCTION

ALS Storage Ring RF system is equipped with two 500MHz single cell re-entrant cavities powered by single YK 1305 PHILIPS 330kW (c.w. output power) klystron. The YK 1305 klystron has four internal cavities, a high stability dispenser-type cathode and an accelerator anode electrode that is used to control the klystron cathode current. During an ALS operational cycle the rf power requirements for the ALS Storage Ring can change from 120kW (RF "ON"-no beam) to as much as 260kW (1.9GeV, 400mA beam current). The klystron's collector efficiency expressed by this simple equation:

$$\eta_c = \frac{P_{out}}{I_{c0} \bullet U_{c0}} \bullet 100\%$$

where:

P_{out}	RF Output Power
U_{c0}	Cathode to Body (ground) Voltage (collector is on the ground potential).
I_{c0}	Cathode Current

The above equation shows that for a constant U_{c0} one would need to vary I_{c0} to maintain high efficiency as P_{out} varies.

Up to now, the U_{c0} and I_{c0} were constant during the entire operational cycle, which resulted in poor efficiency for low output power. The klystron's efficiency could be significantly improved by controlling the klystron beam current as a function of the required output power. By changing the dc potential on the accelerator anode electrode from –33kV to –12kV we can change the klystron beam current from 4 to 12A. (4A is the minimum value of the klystron beam current allowed by the manufacturer, which mitigates the deposition of barium on the ceramic cylinder support structure of the electron gun and accelerator electrode).

2 CONCEPTION

Our goals when designing the Klystron Efficiency Loop was to maintain a constant high-level of klystron drive while varying the klystron beam current during the entire storage ring cycle (in order to achieve high efficiency) and to reserve drive power for good dynamic performance of the Cavity RF Amplitude Loop. The Klystron Efficiency Loop, (a PI loop with a bandwidth 1-2 orders of magnitude lower than the Cavity RF Amplitude Loop) will maintain a constant power gain across klystron-cavity system by controlling the klystron cathode current as a function of the beam loading on the cavities.

$$G_{KC} = \frac{\Sigma P_{cav}}{P_{drive}}$$

where:

ΣP_{cav}	Cavity Cell Power Sum
P_{drive}	Klystron RF Drive Power

The existing Cavity RF Amplitude Loop will remain and is responsible for removing higher frequency disturbances caused by phenomena such as high voltage power supply ripple. In order to implement the Klystron Efficiency Loop we will utilize existing RF signals and a logarithmic identity.

Since subtraction in the logarithmic domain corresponds to a ratio in the linear domain, two identical logarithmic amplifiers followed by a differential amplifier could perform the required task. During our design effort we found a new Analog Devices product, an AD8302 RF/IF Gain and Phase Detector [1], which fit our application perfectly. The chip accepts two RF signals and creates two outputs:

$$V_{MAG} = V_{slp} \bullet \log\left(\frac{V_A}{V_B}\right)$$

$$V_{PHS} = V_{\Phi}\{\Phi(V_A) - \Phi(\Phi(V_B)\}$$

where:

V_{SLP}	Magnitude Slope (default value 30mV/dB)
V_{Φ}	Phase Slope (default value 10mV/deg)

The AD8302 has 60dB dynamic range in the gain subsystem, which is inversely related with the output slope (changing the slope to 60mV/dB will decrease the dynamic range to 30dB). Following the gain detector we designed a simple analog PI controller and an output voltage limiter using an Analog Devices AD8036 [2]. The voltage limiter implements a soft klystron beam over-current protection circuit. The control board is equipped with the manual switch, which allows using the same board as a phase controller for other applications. The loop can be controlled locally from the klystron high voltage power supply equipment rack or remotely from the ALS main control room. The klystron beam current control signal from the control board is sent via an existing fiber-optic link to the Mod-Anode deck where a Thomson TH5186 air-cooled tetrode (operating in a triode configuration) is used to regulate the potential at the klystron accelerator anode electrode.

3 DESIGN AND TESTING

Our main concern during the design process was the possibility of interference (due to an overlap in the frequency domain) between our new Klystron Efficiency Loop and the Cavity RF Amplitude Loop. Backed-up by the positive theoretical analysis and software simulations (PSPICE in frequency and time domain) we finished the design and built a prototype board, which was installed and tested in the ALS Storage Ring main RF system. Tests proved the loop regulated the klystron-cavity system gain correctly, however during each RF power trip or storage ring beam loss the klystron HVPS over voltage protection interlock tripped. The over voltage was due to a resonance at about 18Hz between two main reactive elements of the HVPS filter (11Hy choke and 6uF capacitor). A sudden change in the HVPS current due to the above-mentioned trips created a transient, which in turn generated a HVPS trip. The problem was solved by decreasing the closed loop bandwidth of the Klystron Efficiency Loop from 100Hz to about 2Hz. This modification didn't have any negative effects on the efficiency improvements nor on the RF system's performance since the changes in the RF power requirements are very slow (storage ring fill time is ~10-20 minutes and the beam decay or lifetime is in order of hours).

An additional adverse effect of modulating the klystron's gain via its cathode beam current is that the phase of the RF voltage across the klystron changes significantly, approximately 15deg/amp for YK 1305, so over full current variation (4A-12A) we could expect the total phase shift across the klystron to be as much as 120°. To maintain a constant phase shift across the klystron we re-instituted and modified the Klystron Phase Loop, a fast analog phase loop (closed loop bandwidth ~10kHz). This circuit uses a newly developed (in our lab) phase detector

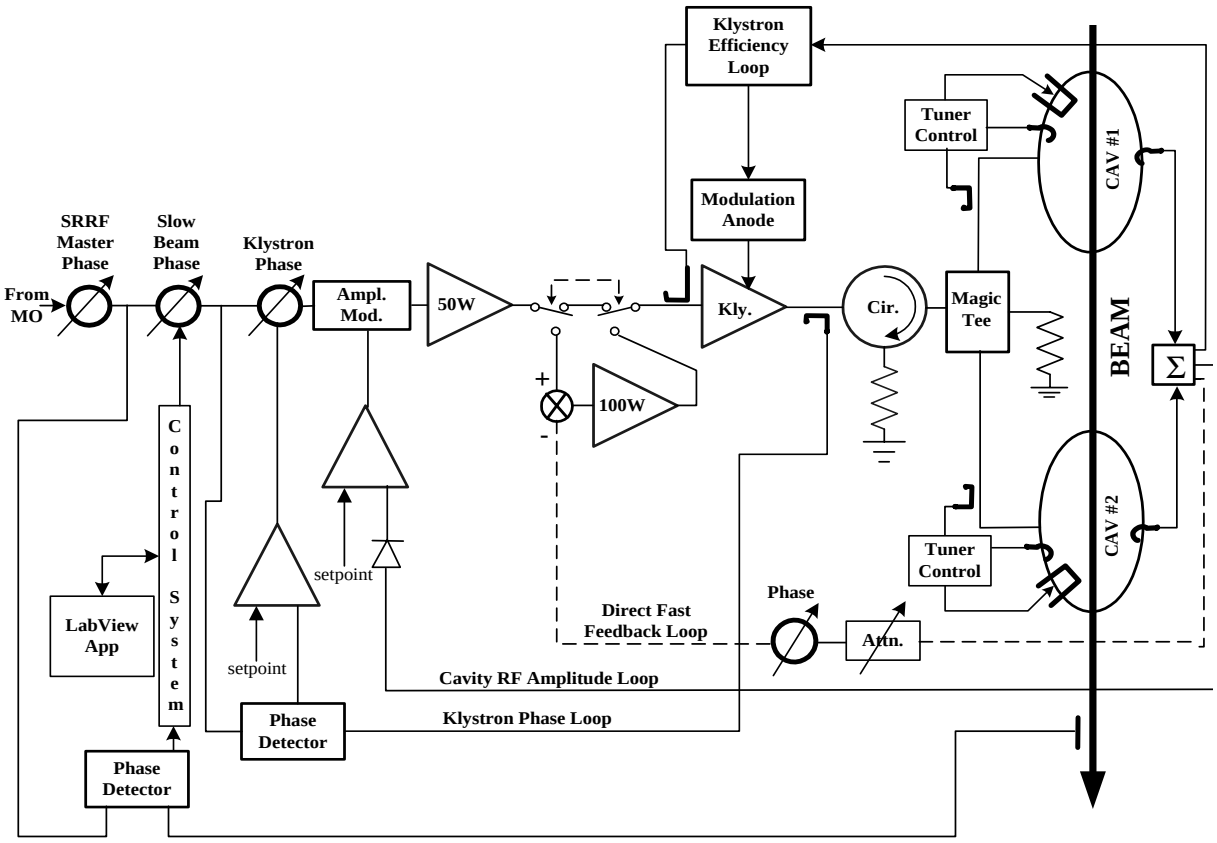

Figure 1: Simplified Block Diagram of Storage Ring RF System.

built with two Analog Devices AD8309 logarithmic amplifiers [3] and a Motorola MCK12140 detector chip [4], which has a 60 dB dynamic amplitude range and a ±360° dynamic phase range. The large dynamic phase range of this detector is important to our application since an ordinary phase detector, which is based on an analog multiplication technique and has a ±90° phase range, could not handle the large klystron phase shift. A simplified block diagram of the fundamental Storage Ring RF system for the ALS is shown in Figure 1.

Figure 2 compares the monitored changes in the klystron beam current, before and after the installation of the Klystron Efficiency Loop, in relation to the stored beam current over one full cycle (8 hours) of the ALS Storage Ring Multibunch Operation.

4 CONCLUSION

The ALS Klystron Efficiency Loop has been fully operational since February 2002 and is proving itself by decreasing the power consumption and therefore the utility bill for the ALS. We met our design goals of holding constant the klystron drive power while varying the klystron gain in order to compensate for stored beam loading. However, as stated we had to adjust the frequency response of the Klystron Efficiency Loop in order to avoid driving the HVPS filter's resonance. We found that the new efficiency loop cohabitated with the existing Cavity RF Amplitude Loop without need for modifications or adjustments. Lastly, based on the year 2001 operating schedule, which had 923 operational shifts, the klystron cathode power consumption at U_{c0} = -52kV & I_{c0} = 10.5A would be approximately 4000MWH. Since February, our measurements for the same operation modes: 1.5GeV Multibunch, 1.9GeV 2 bunch, and 1.9Gev Multibunch have shown power consumption reductions of 0.67 MWH, 0.94 MWH, and 0.43 MWH respectively. These figures equate to an annual reduction of approximately 440 MWH or an 11% reduction

5 REFERENCES

[1] ANALOG DEVICES "AD8302, LF-2.7GHz RF/IF Gain and Phase Detector" –Preliminary Data Sheet

[2] ANALOG DEVICES "AD8036, Unity Gain Stable - Low Distortion, Wide Bandwidth Voltage Feedback Clamp Amps" –Data Sheet Rev. B, 1/01

[3] ANALOG DEVICES "AD8309, 5-500 MHz, 100dB Demodulating Logarithmic Amplifier with Limiter Output" –Data Sheet Rev. B, 8/99

[4] MOTOROLA "MCK12140, Phase-Frequency Detector" –Data Sheet Rev. D, 1997

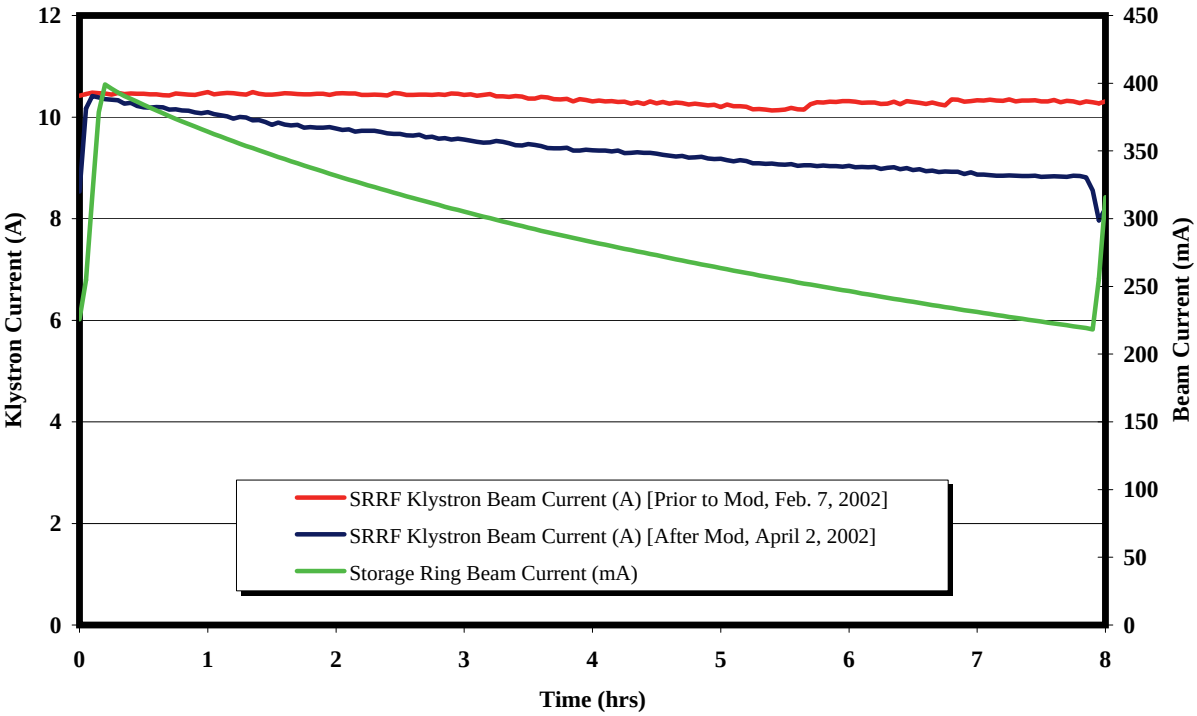

Figure 2: SRRF Klystron Efficiency Comparison for 1.9GeV Multibunch Operation.