

A LOW-LATENCY SUB-MICRON RESOLUTION STRIPLINE BEAM POSITION MONITORING SYSTEM FOR SINGLE-PASS BEAMLINES

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Abstract

A low-latency, sub-micron resolution stripline beam position monitoring system has been developed for use in single-pass beamlines. The fast analogue front-end signal processor is based on a single-stage RF down-mixer and is combined with an FPGA-based system for digitisation and further signal processing. The system has been deployed and tested with beam at the Accelerator Test Facility at KEK. Performance results are presented on the calibration, resolution and stability of the system. A detailed simulation has been developed that is able to account for the measured performance.

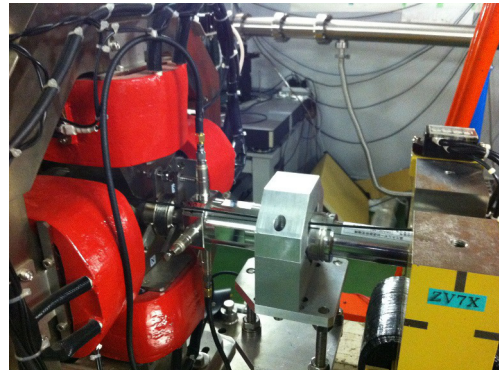


Figure 1: Stripline BPM FONTP1 at the ATF.

INTRODUCTION

The designs for the International Linear Collider (ILC) [1] and the Compact Linear Collider (CLIC) [2] require beams stable at the nanometre level at the interaction point (IP). In support of this, the goal of the ATF2 collaboration based at KEK, Japan is to achieve position stability at the notional IP of approximately 2 nm. To this end, the Feedback On Nanosecond Timescales (FONT) [3] project operates a position and angle feedback system [4] in the extraction line of the Accelerator Test Facility (ATF) [5]. In order to achieve the required level of position stability at the IP, the FONT feedback system needs to stabilise the beam to 1 μm at the entrance to the final focus system; this requires a BPM processing scheme capable of delivering position signals accurate to the sub-micron level on a timescale of the order of 10 ns.

The FONT beam position monitoring system makes use of 6 12 cm stripline BPMs (Fig. 1), 5 of which are located in the diagnostics section of the extraction line (FONTP1, FONTP2, FONTP3, MQD14X and MQF15X). The remaining BPM, MFB1FF, is situated approximately halfway down the final focus section of the ATF. The BPMs are connected to specially developed analogue processing electronics [6] in order to deliver appropriate position signals to an FPGA-based digital hardware module [7] that digitizes the signals and returns the sampled data to a computer where it may be logged.

BPM PROCESSOR DESIGN

A schematic of the processor module is shown in Fig. 2 and a photograph in Fig. 3. The operation is as follows: the top (V_A) and bottom (V_B) stripline BPM signals are

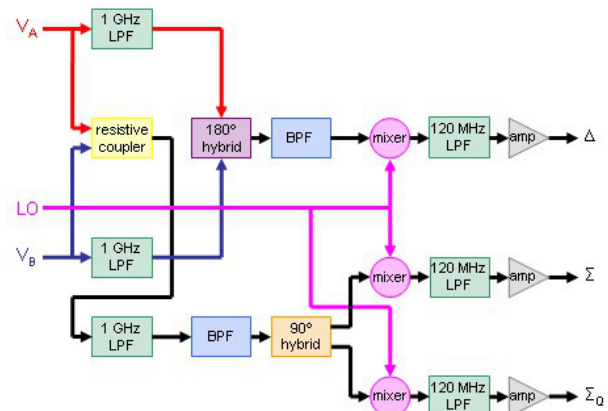


Figure 2: FONT analogue signal processor design.

subtracted using a 180° hybrid to form a difference (Δ) signal and are added using a resistive coupler to form a raw sum signal. This is then sent to a 90° hybrid, the output of which is a pair of signals 90° out of phase with each other known as the sum (Σ) and sum quadrature (Σ_Q). The resulting signals are then band-pass filtered and down-mixed with a 714 MHz local oscillator (LO) signal phase-locked to the beam before being low-pass filtered and amplified using 16 dB low-noise amplifiers. The hybrid, filters and mixer were selected to have latencies of the order of a few nanoseconds in order to yield a total processor latency of 10 ns (Fig. 4).

The maximum amplitude of the output signals (and hence the best signal-to-noise ratio) is achieved when the

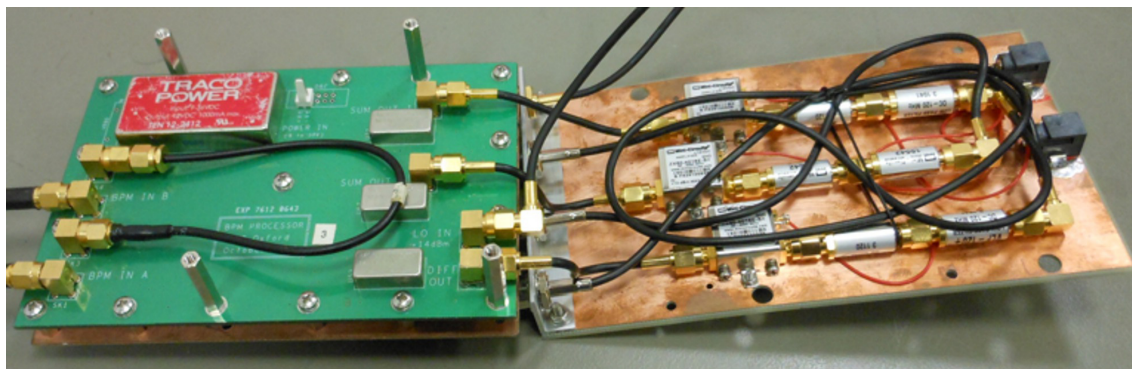


Figure 3: FONT analogue signal processor module with support plate detached.

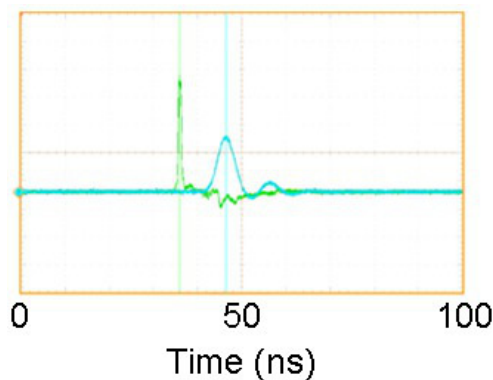


Figure 4: FONT analogue signal processor output (blue) for a test input pulse (green) in volts vs. time.

local oscillator signal input to the mixer is phased to be at peak amplitude; to this end, adjustable phase shifters are used to maximize the peak of the output Σ signal. As the LO is sinusoidal and Σ , Σ_Q are 90° out of phase the Σ_Q signal is maximally sensitive to variations in the phase of the local oscillator signal and may be used to compensate for the effect such variation has on the measured position.

POSITION DETERMINATION

The Σ , Δ and Σ_Q signals output by the processor modules are digitized using analogue-to-digital converters (ADCs) on the FONT5 digital board [7]. The ADCs have 14-bit resolution and are clocked at 357 MHz using a source synchronized to the machine; the ADC clock may be delayed in increments of 70 ps to allow sampling at the exact time the bunch arrives. There are 9 ADCs in total and so a single board is able to fully record the data from 3 BPMs. The position of the bunch is proportional to the ratio Δ/Σ and is, to first order, independent of the bunch charge. The phase of the LO with respect to the beam (ϕ_{LO}) in radians is equal to the ratio Σ_Q/Σ for small deviations; as illustrated in Fig. 5, the ϕ_{LO} is subject to both jitter and a slow sinusoidal oscillation, the combined effect of which is an RMS value $\sigma_{\phi_{LO}} \sim 0.5^\circ$.

This variation of ϕ_{LO} manifests itself as an apparent

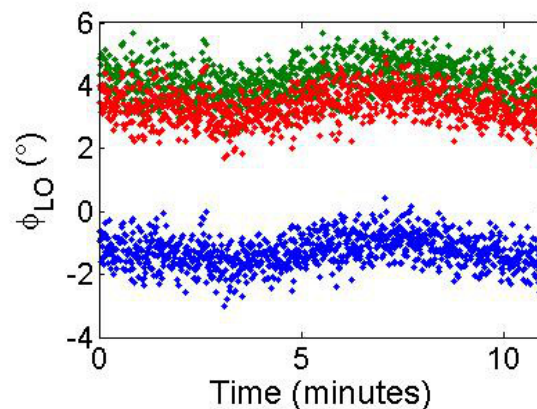


Figure 5: Stability of the LO phase as measured by the processor on FONTP1 (blue), FONTP2 (green) and FONTP3 (red).

change in the measured position of the beam (Fig. 6). To compensate for this effect, the true position in each BPM is assumed to be given by the expression:

$$y_{true} = y_{meas} - \alpha \phi_{LO}$$

and the parameter α is determined by a least-squares fit of the measured position to the phase from any data run with good statistics. The typical value of this parameter for each BPM is given in Table 1.

Table 1: Sensitivity to LO Phase Variation ($\mu\text{m}/^\circ$)

BPM	α
FONTP1	-7.0
FONTP2	-0.3
FONTP3	0.1
MQD14X	-1.6
MQF15X	0.6
MFB1FF	-1.0

The BPMs may be calibrated by scanning the current in an upstream dipole corrector magnet and using knowledge

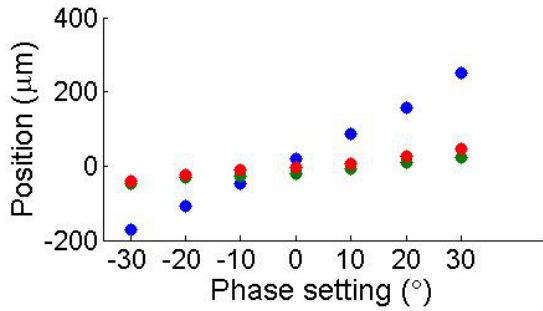


Figure 6: Effect on measured position of a change in the LO phase for FONTP1 (blue), FONTP2 (green) and FONTP3 (red).

of the optical transfer between that corrector and the BPM in question to calculate the displacement of the beam expected for each magnet current setting. Fig. 7 shows an example of such a calibration. For beam offsets within a few hundred microns of the electrical centre of the BPM, the BPM processor responds linearly with beam offset and the calibration constant is obtained from the gradient of a linear χ -squared fit.

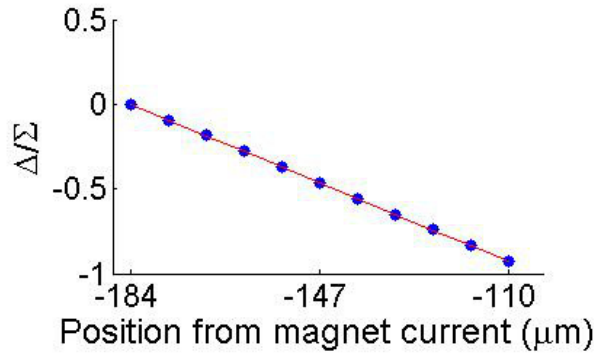


Figure 7: Example BPM calibration: mean ratio of Δ and Σ measured in BPM MQD14X for each current setting of dipole magnet ZV8X (blue); linear fit to data (red).

RESOLUTION DETERMINATION

The BPM resolution is calculated from the system of three BPMs by removing the contribution from the LO phase, performing drift subtraction and then using the measurements from two of the BPMs to predict the position in the third. It is assumed that the three BPMs have similar resolution. The position at the third BPM, y_3 , is then predicted as:

$$y_3 = Ay_1 + By_2$$

where y_1 and y_2 are the positions in the first and second BPMs respectively and A and B are coefficients determined either from the beam transport matrices or by a least-squares fit to the data. The BPM resolution, σ_y , is then given by:

$$\sigma_y = \sigma_{res} / \sqrt{1 + A^2 + B^2}$$

where σ_{res} is the standard deviation of the residual when the predicted position is subtracted from the observed position. The best result obtained to date is shown in Fig. 8 which suggests the resolution of the combined system of BPMs FONTP1, FONTP2 and FONTP3 is $0.43 \mu\text{m}$.

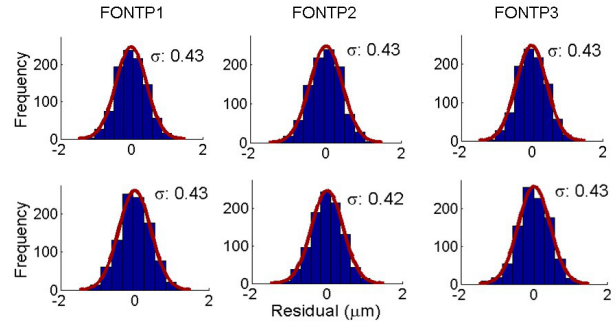


Figure 8: Histograms of residuals for BPMs FONTP1, FONTP2 and FONTP3 (blue) obtained by predicting the position using the transfer matrices (top) and by a least-squares fit to the other two positions (bottom); a Gaussian fit to the data is plotted in each case (red) and the width is given (in μm).

CONCLUSIONS

A stripline BPM monitoring system has been developed capable of providing position signals with resolutions less than $0.5 \mu\text{m}$ within a timeframe of 10 ns. This is achieved for bunch charges of $\sim 0.5 \times 10^{10}$ electrons with the beam approximately centred in each of the three BPMs. Performance is degraded by a reduction in the effective charge or if the beam orbit includes large displacements from the centre of the BPMs. The phase compensation procedure described has been adapted for use in the digital logic of the FPGA in order to provide a real time improvement in the performance of the FONT feedback system.

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