CERN's FMC KIT

Matthieu Cattin*, Evangelia Gousiou, Javier Serrano, Erik van der Bij, Tomasz Włostowski,
CERN, Geneva, Switzerland

Abstract

In the context of the renovation of controls and data acquisition electronics for accelerators the BE-CO-HT section at CERN has designed a kit based on carriers and mezzanines following the VITA FPGA Mezzanine Card (FMC) standard. Carriers exist in VME64x and PCIe form factors, with a PXIe carrier underway. Mezzanines include an Analog to Digital Converter, a Time to Digital Converter, a fine delay generator and a Digital Input/Output. All of the designs are licensed under the CERN Open Hardware Licence and commercialised by companies.

This paper discusses the benefits of this carrier-mezzanine strategy and of the Open Hardware based commercial paradigm. It also explains the design of each layer of the FMC kit, from the hardware to the gateware and the Linux device driver. In addition, several tools to help designers developing gateware for mezzanines and new concepts such as the Self-Describing Bus (SDB) and the fmc-bus are presented. Lastly, some of the plans for the future of the FMC kit and Open Hardware Repository (OHWR) are brought up.

INTRODUCTION

One of the missions of the BE-CO-HT section is to specify, design and provide electronic modules for the control systems of all accelerators at CERN. The section supports a large variety of hardware among which digital and analogue I/O, level converters, serial links and timing boards. Replacing obsolete modules and upgrading the control systems to new technologies requires a continuous flow of design work.

Motivations

Many of the electronic modules used in the control systems, either COTS (Commercial Off The Shelf) or specifically designed at CERN, have become difficult to maintain for several reasons. In particular, most of those modules contain obsolete components or are discontinued products. Some of the modules are twenty years old and often the documentation and the knowledge is scarce or lost, making the debugging or repair very hard and time-consuming. For modules developed at CERN, there was no design strategy to help re-use existing blocks. Also a very limited team has to maintain a large variety of modules. Finally some modules are maintained in operation with a limited stock of spares and therefore cannot be deployed in new installations.

* matthieu.cattin@cern.ch

New Approach

In charge of renovating the catalogue of electronic modules, we decided to develop new hardware based on the following principles:

- Openness of designs
- Modularity and re-usability
- Compliance with existing standards

The carrier-mezzanine concept was chosen to reduce the number of different modules and to increase the modularity. The carrier boards are platform-dependent and meant to be as generic as possible while the mezzanines are platform-independent and specific to a particular task. The carriers are built around a central FPGA (Field Programmable Gate Array) and include an interface to the host bus, some data storage memory, a clock distribution and PLLs compatible with White Rabbit (WR) [1] requirements, a few Gigabit links to communicate between carriers and finally one or more FMC slots. The mezzanine is interfacing with the external world and contains mostly analogue and signal conditioning electronics.

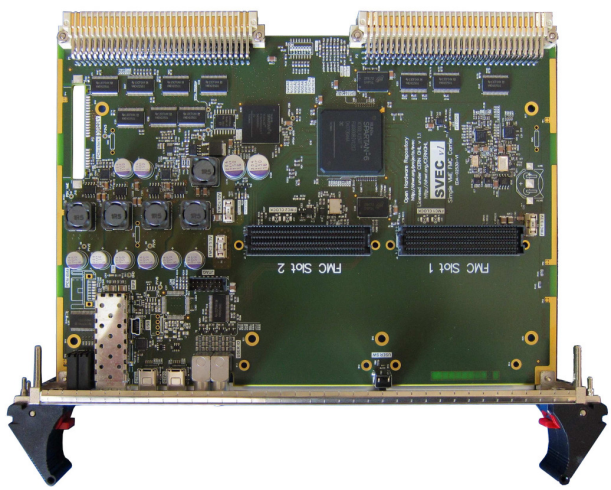

Figure 1: VME64x FMC carrier (SVEC).

The standard that best fits our requirements in terms of carrier-mezzanine approach is the ANSI/VITA 57.1 FMC standard [2]. For instance, the FMC standard is very flexible as the connections between carrier and mezzanine are mostly unaware of the signal direction, electrical level and protocol.

In order to improve the modularity and re-usability of the HDL (Hardware Description Language) designs, the Wishbone [3] bus was chosen as the standard to interconnect the diverse logic blocks inside the carrier's FPGA. To enhance the HDL code re-use, generic Wishbone cores and

ISBN 978-3-95450-139-7

other utility cores were created and gathered in libraries. Moreover, to automate the design flow (dependencies solving, synthesis, simulation, place & route), tools and scripts were developed.

The same modularity concept applies to the Linux device driver layer for which new concepts like the software fmc-bus [4] and the ZIO framework [5] have emerged and are making their way to the official Linux kernel.

To allow sharing of design information the Open Hardware Repository (OHWR) was created [6]. It is a collaborative web-based platform that hosts the boards, the HDL and the software development of Open Hardware projects. All the boards of the FMC kit have a project on the OHWR website and the hardware designs are licensed under the CERN Open Hardware Licence (CERN OHL).

DESIGN

The FMC kit is designed based on well-established standards and in a modular way. This flexible approach is applied on every layer, from the hardware with the schematics and layout to the software with the driver, including the gateware and the test environment. The idea is to have a wide and solid base of building blocks that can be re-used in many different designs. As those modules are meant to be used by many people, also outside of CERN, the code and the documentation should be of good quality. We believe that feedback from users will help to improve shared modules. Finally, new developments can be made more efficient as most of the required blocks are already available, documented and tested.

Modularity: The Wishbone Case

The most explicit example of modularity and block reuse is probably the gateware design. The gateware is the HDL code used to generate the bitstream that configures the FPGA on the carrier. The gateware is designed around one or several Wishbone buses. The Wishbone standard is well adapted to inter-block communication because it is simple, easy to implement and versatile. In order to fulfill the high throughput of certain designs we proposed a new pipelined mode to the Wishbone standard maintainers. The new mode was accepted and is now part of the latest revision of the standard.

Several bus master modules from OpenCores [7] are used to communicate with components outside the FPGA that have standard serial interfaces (SPI, I2C or 1-wire). Thanks to their Wishbone interface, those modules can be integrated to the design without any modification.

For other bus interfaces like VME64x and PCIe, for which no OpenCores modules were available, new HDL components were created.

A small helper tool called wbgen2 [8] was developed to design specific registers that have to be interfaced to the Wishbone bus. It generates HDL (VHDL, Verilog), C headers and documentation (html, tex, texinfo) from a single description file. The generated module can directly be connected to a Wishbone bus while the other side is connected to the application.

Another important component in the Wishbone topology is the crossbar switch. It allows to connect and arbitrate several masters and several slaves. The development of this essential component was carried out in GSI (Helmholtzzentrum für Schwerionenforschung GmbH).

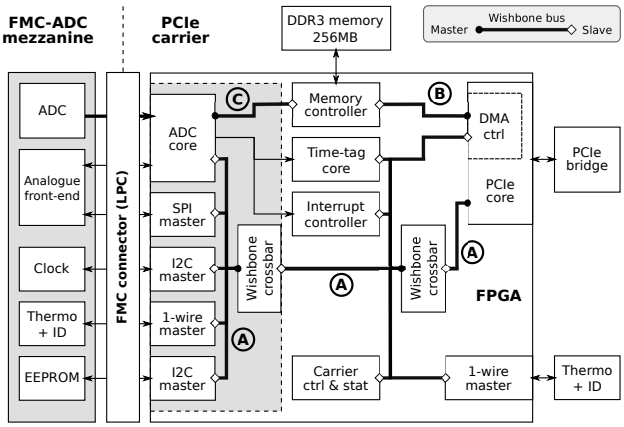

Figure 2: FMC-ADC gateware architecture.

A good example of the flexibility offered by the Wishbone bus interconnect is the HDL architecture of the FMC-ADC [9], illustrated in Fig. 2. Wishbone bus A is mapped in the PCI BAR0 address space. It allows access to the configuration and control peripherals. Buses B and C are separated from the other bus and used only to transfer data to and from the DDR memory. Due to its size, the DDR memory is not directly mapped in the PCI address space. The only way to access it is through DMA using the controller in the PCIe interface module.

New Tools and Concepts

To make the reuse of the blocks easier, the helper tool hdlmake [10] was developed and is available on the OHWR. The designer only has to write *Manifest* files describing the project structure and dependencies. Then hdlmake automatically fetches the required libraries from different locations (remote repositories, local folders) and generates Makefiles for synthesis and simulation.

In order to let the driver automatically discover the gateware architecture and load the corresponding modules, the SDB (Self Describing Bus) concept [11] was developed. It consists of series of structures that describe the Wishbone blocks and their mapping in the address space. Additionally, SDB meta-information records allow to uniquely identify the gateware. Those meta-information records contain, among other things, the synthesis date, repository URL, commit ID, etc...

Prior to loading the final bitstream to a carrier's FPGA, the driver has to make sure the expected mezzanine is plugged in the FMC slot. This is to avoid any hardware damage that could occur if an incompatible bitstream is loaded. Therefore, at startup the FPGA is loaded with

ISBN 978-3-95450-139-7

a *golden* bitstream that only allows access to the carrier peripherals and to the mezzanine standard EEPROM. By reading the IPMI information in the EEPROM the driver can verify that the correct mezzanine is attached.

The mezzanine EEPROM does not only contain the IPMI part as defined in the FMC standard, but also other mezzanine specific data such as calibration values. To elegantly handle the different data in the EEPROM, a simple file system was created. This file system is called SDBFS [12] as it is based on SDB data structures.

A test environment was developed in Python and interfaced with the hardware via a simple I/O driver and a library to verify the boards after manufacturing. Such an environment significantly reduces the testing time and eliminates the risk of mistakes by automating the process. The same environment is also used to test the gateware.

Porting Made Easy

With such a modular HDL architecture, porting a design from one carrier to another has become straightforward. For example, porting the FMC-ADC HDL from the SPEC (PCIe carrier with one FMC slot) to the SVEC (VME64x carrier with two FMC slots) took just one week of work. This only involved changing the bus interface to the host from PCIe to VME64x and duplicating the FMC-ADC block. Note that designing a VME64x ADC board from scratch would have taken several months.

The same applied to the Python testing environment. Most of the code written to test the FMC-ADC on the SPEC carrier was re-used to test the corresponding gateware on a SVEC carrier. Again, only the bus interface layer needed to be changed from PCIe to VME.

OPEN HARDWARE

For the last three years CERN's controls group designed all its new projects in a fully open fashion using the OHWR platform to improve collaboration and sharing. Based on our experience of collaboration with other groups at CERN, external partners and companies we can tell more about the advantages and drawbacks of Open Hardware designs.

Towards Better Designs

Some of the main advantages of an open hardware design are the peer review and user feedback. Publishing the design, even during the development phase, allows for peer review and early detection of bugs or misdesign problems. Giving the production task to companies that design their own products (as opposed to production companies) is also an important point of the whole process, as they will not only spot manufacturing issues but also design problems. This additional stage of checking helps to avoid producing faulty prototypes or series.

The feedback from users is also very valuable. Having access to the source helps users to better understand the design and give useful comments or propose improvements. Moreover, some people are installing our designs in different, sometimes unexpected, conditions. In closed designs, customers can only report bugs and are not able to look themselves into the schematics or HDL to find out what is going wrong.

Those additional steps, even if they extend the development phase, are crucial to find issues before a module is deployed in the CERN installations. In the end, the additional time spent will be counterbalanced by a lower down-time of the accelerators.

More Collaborations

The BE-CO-HT section collaborated with other groups at CERN as well as with external associates and companies to develop the FMC kit. For example, the PCIe, the VME64x and the PXIe carriers were specified by CERN and the schematics and layout were sub-contracted to companies. An important part of the software framework was also developed by companies outside CERN.

As the boards are produced and tested by companies, it offloads our team at CERN and allow us to concentrate on other tasks like the development and integration of the new modules to the existing control systems. In addition, the boards come with a warranty that includes the repair of faulty devices. Like the hardware, the HDL core libraries are developed in collaboration with other institutes.

Open Hardware considerably facilitates collaborations and design re-use. The OHWR already counts several boards that were used as a basis to design new ones. For example, the PCIe FMC carrier (SPEC) has already served as a starting-point to develop two other boards, a PXIe FMC carrier and a PowerPC FMC carrier. Besides, other groups at CERN or outside are integrating boards from the kit, mainly FMC carriers, in their own projects. These external partners also contribute to the OHWR with new hardware or HDL designs.

A Few Drawbacks

Even though the open hardware model perfectly fits our needs, we can still list a few disadvantages. One is the additional effort needed to give support to collaborators and users. This consists mainly in replying to questions and sometimes in helping setting up a system. But we believe that this extra workload can be mitigated with additional quality in the project, essentially good and up-to-date documentation. Furthermore, we expect companies selling Open Hardware design to progressively take over the work of assisting users.

Finally, we can mention the fact that the first collaboration with a company to produce an Open Hardware board took more time than through the conventional work-flow. The additional time can be explained by the design iterations following the feedback from the company producing a board and sometimes by PCB or assembly quality issues in pre-series. In general, it takes about one year between the order and the series delivery. It includes a pre-series of a limited number of boards to validate the production process.

ISBN 978-3-95450-139-7

PERSPECTIVES

Even though the first Open Hardware designs are now commercially available, there are still some points that can be improved in the OHWR projects.

Improving Documentation

The last few years were dedicated to the development of boards and the production of the first series in collaboration with industry. Now that the basic building blocks of the kit are released or will soon be, an effort will be made on the project's quality. In order to facilitate users and new developers to start with OHWR projects, the documentation should be completed and the projects and repositories structure should be cleaned and unified.

In the meantime, FAQ pages were created to centralise the questions received and answered by e-mail. Moreover we expect the companies selling Open Hardware products to be able to give support to the users.

Universal PCB Design Tool

Different institutes, laboratories or companies might use various PCB design tools. Currently there is no common file format to transfer projects between those EDA tools. This is a serious limitation to re-usability. Unfortunately Free Open Source Software (FOSS) alternatives are not adequate to be used in complex, multi-layer PCB design projects. For those reasons the controls group at CERN decided to encourage the improvement of KiCad, one of the FOSS EDA programs. The objective is to help enhance KiCad in such a way that it becomes an efficient tool for PCB design that people can use to share their design information without compromising productivity.

Next Front-end Computer Platform

Another concern is the choice of the future platform for the front-end computers at CERN. Currently, the two platforms supported by the BE-CO group are VME64x and PICMG 1.3 (industrial PC with PCI and PCIe slots). So far, FMC carriers were developed for both platform and a PXIe version is underway. The latter is supported by the EN-ICE group at CERN.

The two supported platforms have their limitations. For example, the PC form-factor is not well suited regarding on-site board replacement. A VME64x board on the other hand can easily be replaced but here the concern is more on the backplane bus throughput. In addition, both standards are missing clock and trigger distribution lines in the backplane, which is an important feature in a distributed control systems. Therefore CERN's controls group is looking for a new standard for its front-end computer. Whatever the next front-end platform will be, it is just a matter of designing a new carrier. All the mezzanine kit and development framework is already there.

CONCLUSIONS

As a service provider, the BE-CO-HT section at CERN has to support a large variety of electronic modules and continuously design new boards to replace the obsolete ones. In order to fulfil this mission with limited human resources the next generation of control boards have been developed in an Open Hardware way, sometimes in collaboration with external partners. The new kit was designed to be modular and based on standards such as FMC and Wishbone in order to promote re-usability and sharing.

The FMC ecosystem developed over the last few years is now getting mature. All the basic pieces like carriers, mezzanines, HDL libraries, Linux device drivers and several helper tools are available on the OHWR website. With this framework the development of new project and the porting of existing mezzanines is made easier and faster. However, most of the OHWR project will require a consolidation effort in the coming years.

With Open Hardware designs, the feedback and the suggestions from users improve the quality and therefore reduce the risk of discovering problems during operation. In addition, openness encourages to have a good documentation in order to limit the time spent to assist users.

The Open Hardware paradigm changed the way we work with industries. The production, testing and support tasks were handed over to companies which are now selling Open Hardware boards as their own products. This new model not only allowed to unload CERN from some work but also favored knowledge transfer to industries of CERN member states.

REFERENCES

[1] J. Serrano *et al.*, "The White Rabbit Project", ICALEPCS 2009.

[2] "FPGA Mezzanine Card (FMC) Standard", ANSI/VITA 57.1-2008 (R2010), ISBN 1-885731-49-3.

[3] "WISHBONE Revision B.4 Specification", OpenCores Organization, 2010.

[4] A. Rubini, "FMC Bus Abstraction for Linux", 2013, `www.ohwr.org/projects/fmc-bus`

[5] `www.ohwr.org/projects/zio`

[6] E. van der Bij *et al.*, "Open hardware for CERN's accelerator control systems", ICALEPCS 2011.

[7] `opencores.org`

[8] `www.ohwr.org/projects/wishbone-gen`

[9] `www.ohwr.org/projects/fmc-adc-100m14b4cha`

[10] hdlmake, `www.ohwr.org/projects/hdl-make`

[11] A. Rubini, W. Terpstra, M. Vanga, "Self-Describing Bus (SDB), Version 1.1", 2013, `www.ohwr.org/projects/fpga-config-space`

[12] A. Rubini, "SDBFS, A Flash File-system based on SDB data structures", 2012, `www.ohwr.org/projects/fpga-config-space`

ISBN 978-3-95450-139-7