CONTROL, SAFETY, AND DIAGNOSTICS FOR FUTURE ATLAS PIXEL DETECTORS

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Abstract

The ATLAS pixel detector completed successfully the data-taking period during run 1 of the LHC. To ensure its excellent performance during next run periods with increasing demands two upgrades of the pixel detector are foreseen. One takes place in the first long shutdown of the LHC, which is currently on-going: an additional most inner layer will be installed, the Insertable B-Layer (IBL). The second upgrade will replace the entire inner detector of the ATLAS experiment by the Inner Tracker (ITK) and is planned for about 2020, when the LHC will be upgraded to HL-LHC.

We present a concept for the control of the ITK pixel detector at the HL-LHC. While this requires completely new strategies, the control system of the IBL includes only single new components, which can be further developed for the long-term upgrade.

ITK DETECTOR LAYOUT

The pixel detector consists of four barrel shaped layers in the central part and six disk on each side covering a pseudo rapidity of $|\eta| = 2.5$. The basic unit is a detector module, built by one pixelized sensor with up to six front-end chips bump bonded to the sensor cells. In the central part modules are mounted on support structures, called staves, which include a cooling pipe. At the ends of the support structure the End of Stave (EoS) cards route all connections to the outer world: power lines, physical data, trigger, monitoring and control signals. A data transceiver multiplexes the physical data stream onto an optical interface. All optical and electrical services are passed to a service cavern, ca. 100 m far away from the detector.

Detector elements, which require monitoring and control by the Detector Control System (DCS) are the detector modules themselves, the electronics on the EoS card, the optical interfaces, the environment, and the cooling of the detector [1].

New powering schemes are under development to reduce the services. The parallel powering scheme with local DC-DC converters helps to reduce the cable diameters. The serial powering scheme reduces the number of LV cables and is the current base line. If the modules of one support structure (e.g. a half stave) share one LV line, this reduces the services significantly, however a local control unit is required to disable mal-functioning modules.

DCS CONCEPT

The DCS has to ensure the safety of the detector at all times. It has to supply the detector with all entities required for operation. It must provide the operator with tools to ensure a safe and reliable operation and the expert with additional information to diagnose the detector's behaviour and the DCS.

As once installed in the experiment, no access is possible over years, a highly reliable control system is required. Design constraints are the high power density inside the detector volume and the sensitivity of the sensors against heat-ups. Material reduction and radiation hardness of all components installed inside the tracker volume are further requirements. DCS subjects are the detector modules (sensor and front-end electronics), the opto-electrical transceivers, further on- and off-detector electronics, and the detector environment.

Depending on availability and reliability all DCS functionalities are grouped into three categories. Figure 1 gives an overview on the three independent paths of DCS.

Safety must be ensured at all times. Therefore the highest level of reliability is required for items of this category. Control is required for all use cases including assembly and commissioning phases of the detector, its start-up as well as its on-going operation. A high reliability is mandatory for items of this category. Diagnostic information should be available on request. It allows for tuning the detector performance to its optimum.

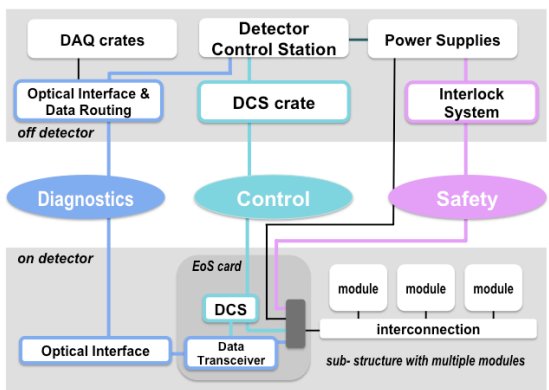

Figure 1: Three independent paths of DCS.

Safety

All elements, which are responsible for the safety of detector or human being, should be completely independent from any other functionality. A purely hardwired system is envisaged, which does not rely on initialising procedures or loading of software. As the highest level of reliability is required, no active components should be located inside the tracker volume.

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A location of the equipment further outside makes it accessible for repair.

As heat up can cause irreparable damages to the detector modules, they are the main safety risk. Therefore temperature monitoring and a fast reaction to over heats are essential for the health of the detector. This can be realized by temperature sensors, which are attached to the cooling pipe. The sensors have their individual services directly connected to the outer world, where a hardwired interlock system can be installed. As there are no active circuits inside the tracker volume, such a system can run at all times. Neither high precision nor a fine segmentation is required.

A similar hardwired interlock system is already in use for the actual pixel detector and is also under construction for the IBL.

Control

The control path must be available for all use cases. Its functionality should be independent from the Data Acquisition (DAQ) system. This part of DCS will mainly be responsible for all powering units and must therefore operate with a high reliability. Depending on the power supply type the segmentation will vary. The operation will partly take place at the level of the power supplies, partly control individual detector modules.

The control path should always include a parallel monitoring, which gives feedback to the operator on the success of any kind of operation.

Concerning the high voltage all operation are foreseen at the level of the power supplies. This includes changing of voltages set, monitoring voltage and current, and switching outputs on and off. The HV system should have dedicated interlock inputs by which the interlock system can overwrite any commands.

Concerning the low voltage a control only at the level of the power supplies is not sufficient. Just the interlock will act directly on the power supply with a coarse segmentation. However especially in the case of serial powering a local DCS entity, close to the detector modules, will be necessary to disable individual modules, which share all one common low voltage line. As the available place is very restricted such entity can only be achieved by an ASIC. The very special needs of such a DCS chip require a dedicated chip design. More details follow in the next chapter.

Diagnostics

Diagnostics information will only be required on demand. However as diagnostics data will be used to tune the detector to its optimum, a fine segmentation and high precision are necessary. To handle the high amount of data, the monitoring values will be processed locally and sent through the optical data path as it is used by the DAQ system. As no additional lines are necessary, this is an efficient method to reduce the material inside the tracker volume. An ADC plus an analogue multiplexer, which are integrated into each front-end chip, can measure various voltages, currents and the temperature. On the receiving part a special mechanism must exist to separate DCS and DAQ data again. The FE-I4, as it will be used for the IBL, already includes such circuits and first experience can be gathered soon using this new path, see below.

DCS NETWORK

Commands, coming from the detector control station must be distributed onto individual modules; vice versa data must be collected locally and sent back, informing the operator on the success of a command. These tasks are fulfilled by two ASICs, DCS chip and DCS controller, which are the main ingredients to realize the control path of the pixel ITK.

Each detector module is supervised by its own DCS chip, while the DCS controller connects to the outer world. In this way a tree shaped network is built, shown Figure 2.

Common requirements to the DCS chip and the DCS controller are high reliability, reduction of services and radiation hardness. As both chips will be located inside the pixel detector volume, they must withstand the same radiation levels as the front-end readout chips. Simulations have shown that for a scheduled integrated luminosity of 3000 fb^{-1} a radiation dose of 7.7 MGy must be expected at the center of the innermost layer. Besides the radiation dose, also the flux of charged particles inducing single event effects must be considered. As the volume of DCS data is small compared to the physical data, speed is not a problem. Additional check sums or other protection mechanisms can be included to enlarge the reliability of the communication protocol. Due to the serial powering and related different voltage levels an AC coupling of the data lines is necessary. Designing the DCS ASICs in the same technology as the front-end chips profits from the experience already gathered with the development of the front-end electronics.

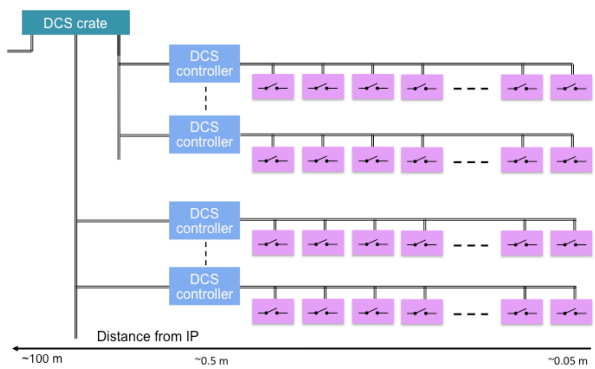

Figure 2: The DCS network.

DCS chip

Besides the common requirements to all DCS electronics installed inside the tracker volume, special constraints must be considered for the design of the DCS chip. Its main task is the switching of individual detector modules of the serial powering chain. So the DCS chip

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has to fit into the serial powering concept. This means that each DCS chip will be operated at a different DC level, consequently the communication must be AC coupled. The DCS chip should provide feedback on commands, which it executed. Further a communication interface is required, which receives commands and sends data to the outer world. A separate powering should ensure availability of the DCS chip for all use cases.

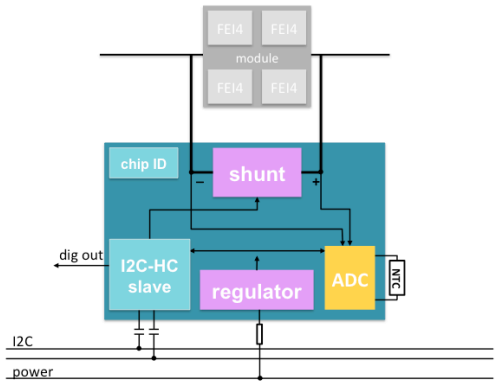

Figure 3: DCS chip.

Figure 3 shows the main components of the DCS chip as it is currently under construction. The main component is the shunt, which allows for switching the module. A similar device was already developed for the ITK strip detector by M. Newcomer, see [2]. This shunt is adapted to the power needs of the pixel modules. The feedback to this control unit is provided by an ADC combined with a multiplexer, which allows for local voltage and temperature measurements. As such ADC is already developed and successfully tested for the front-end readout chip of the IBL [3], the ADC of the DCS chip will be based on this design. To reduce the power, the DCS chip will have no own clock generator, the clock will be provided by the SCL line of the I2C interface (see below). This limits the sampling rates of the ADC to some kHz, but this is sufficient for the few monitored values.

The communication to the DCS chip is implemented by a modified I2C protocol, which is additionally Hamming protected against communication errors. It corrects single bit flips, dual bit flips can be detected. Furthermore every register in the chip logic is made up with triple modular redundancy (TMR). This means that every register has two clones and a majority voter. In case of a bit flip, the voter writes the correct value of the two unchanged cells back in the flipped one. These protection mechanisms were already successfully tested and irradiated in previous prototype chips [4]. To make the I2C bus suitable for serial powering, it will be - differing from its standard specification - AC-coupled. Various simulations have proven this approach.

Further it is essential that the DCS chip has its own regulator, which allows for separate powering and ensures in that way the independent availability. This requires just one line per serial powering chain, as the return of the DCS chip will be linked to the overall power return. In total this gives three additional lines per serial powering chain for DCS instead of individual control, voltage and temperature monitoring lines per detector module. In this way the DCS chip helps to reduce the material inside the tracker, while at the same time the special constraints of serial powering are solved.

The DCS chip will be submitted in 130 nm CMOS technology by November this year.

DCS Controller

The DCS controller is the link between the DCS chips mounted on the detector sub structures and the DCS PCs, installed ca. 100 m away from the detector. Therefore on one side it requires a communication interface, which is capable for longer distances. On the other side the DCS chips must be supervised.

Based on the good experience with the CAN (Controller Area Network) protocol in the current ATLAS detector, CAN was chosen for communication to the outer world. Its inherent high reliability was the main criterion for its choice. To steer the DCS chips the DCS controller includes an I2C Hamming protected master, which transmits commands to the DCS chips and receives monitoring data from them. Besides that a bridge module translates CAN messages into I2C and vice versa. For the AC coupled transmission over the I2C-HC bus the DCS controller holds physical layers for the SDA and SCL lines. Again all logic cells of the DCS controller are made up with triple modular redundancy. A prototype of the DCS controller was developed in 130 nm technology. Communication and first irradiation tests were performed.

The complete design of the DCS controller will also contain an ADC to allow for measurements at the end of stave card. DCS controller should also provide digital signals, which can be used to control other units, which are mounted on the EoS card, e.g. a reset to the data transceiver. These components will be added in the next generation of DCS controller.

DCS OF THE INSERATBLE B-LAYER

During the first long shutdown of the LHC, which is currently on-going the beam pipe inside the ATLAS tracker will be replaced by a pipe with a smaller radius. This allows for installing an additional fourth pixel layer directly on the beam pipe, called the Insertable-B-Layer. Its detector modules are mounted on local support structures, called staves. Fourteen staves form a cylindrical shell with an average radius of 33.25 mm covering a pseudo-rapidity of $|\eta| < 3$. Each detector module consists of the pixel sensor and two front-end chips, whose readout channels are bump-bonded to the sensor cells. The front-end readout chips, the FE-I4s, are developed in a 130 nm bulk CMOS process. Each pixel cell has a size of (50 x 250) μm^2, altogether the IBL provides 12 million readout cells. Via an optical transceiver, which is located close to the detector modules, data is transmitted to the control room. Due to

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the high power dissipation of the modules an efficient cooling system is required and a cooling pipe is integrated into each stave [5].

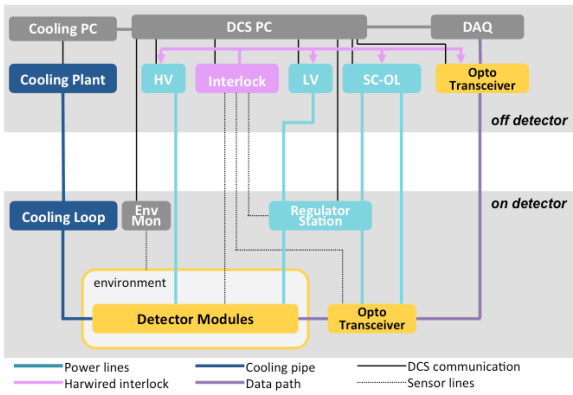

Figure 4: DCS of the Insertable B-Layer.

Figure 4 gives an overview on the IBL DCS hardware. Detector modules, the opto transceivers, and the detector environment are subject to DCS. Several power supplies (HV, LV, SC-OL) provide all units with the power they need. On the other side the heat dissipation is compensated by a CO_2 evaporative cooling system [6]. Several monitoring units are in place, most critical elements are connected to the interlock system in parallel, see below. All components are steered by the DCS PCs.

Control and Feedback

As the power lines are routed up to the control room in parallel, most of the control of the detector modules can be provided at the level of the power supplies. To protect the sensitive front-end chips against over voltages a regulator station is additionally installed close to the detector. Key components of the regulator station are the radiation-hard LHC4913 regulator and a digital trimmer, which allow for remote control per module.

Safety

Main risk to the detector modules is over-heat, which can destroy the modules irreparably. Therefore the detector modules are equipped with NTCs, which are monitored and in parallel directly connected to an hardwired interlock system. Its inputs consist of discriminator circuits, which create a logical signal in case a given threshold (temperature) is exceeded. In the same way other sensitive equipment is connected to the interlock system. Core of the interlock system is a CPLD. It collects signals from all detector elements, combines the information and sends signals to the related power supplies. Typically all modules of a half stave are controlled together or even larger groups of the detector. Such a system is completely independent from other entities and therefore gives the highest level of reliability.

Diagnostics

The FE-I4 already contains an ADC and analogue multiplexer, which can provide detailed information on the front-end level. It measures the leakage current, several voltages and the temperature per front-end chip and – on request - sends these data via the optical DAQ path. The off-detector decoder extracts DCS data and passes it via Ethernet to the DCS PC. Further an OPC-UA server receives the date and provides it for WinCC.

These data are only available when the DAQ is running however they are a powerful tool to diagnose the detector behaviour. It is the most detailed information, which is available to the DCS. For the first time DCS values are sent through the optical path offering the possibility to collect experience with this approach for the longer term future.

SUMMARY

Two new pixel detectors will be installed in the ATLAS experiment. The assembly of the IBL is just on-going, while the pixel ITK will be installed in the beginning of the next decade. We presented a new DCS concept, which is based on three independent paths: control, safety, and diagnostics. While the interlock system of the IBL ensures safety of the detector, a similar approach can be used for the ITK. Diagnostics data is sent through the optical link, first experience can be already gained with IBL. Control is in the IBL still provided by individual services. This will require completely new methods for ITK, where just custom designed ASICs fit. There design has started and its status was reported.

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