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THE «**KATOD-1**» STRIP READOUT **ASIC** FOR CATHODE STRIP CHAMBER

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1. Introduction

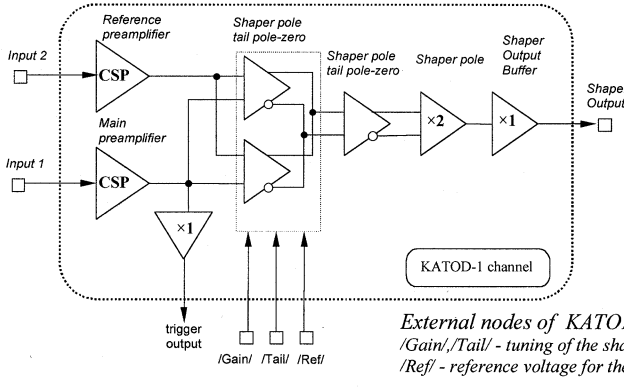
Experimental conditions of the forward muon station ME1/1 demand specific requirements for the front-end electronics. ME1/1 is located behind the endcap hadron calorimeter (HE) in the nonuniform magnetic field up to 3.5 Tesla and background rate order of 1 kHz/cm^2, what corresponds to the rate of 100kHz per cathode readout channel. ME1/1 station is required to provide the spatial resolution order of 75μm for muons Pt measurements with the aim of a good matching of the track information between muon system and central tracker.

Azimuth coordinate of the track hit in each layer from 6 of the chamber is obtained from the measurement of the charge induced on the several adjacent cathode strips. To achieve the required spatial resolution the charge has to be measured with an accuracy of about 1%. Such precision demand very rigid requirements to the electronics channels of the charge measurement from the cathode strips and particularly to the input preamplifier-shaper which should be very low noise with signal to noise ratio of > 100.

Different types of the head transistor were studied for optimization of the noise performance and pulse shaping time. As a result of development 16-channels Application Specific Integrated Circuits (ASIC) KATOD-1 has been designed. KATOD-1 is a charge sensitive preamplifier-shaper with tail cancellation. Head *n-p-n* transistor of ASIC optimized by the noise performance and peaking time (T_p=100ns). Each channel of the ASICs has additional preamplifier output for triggering.

2. Schematics

One channel of the KATOD-1 ASIC consists of the pair of preamplifiers, multistage shaper with gain and tail cancellation control, output followers and single bias circuit (Fig.1). The input signals from the cathode strips are amplified and shaped into the output voltage pulses which have a semigaussian shape with 100ns peaking time.



External nodes of KATOD-1 ASIC:
/Gain/,/Tail/ - tuning of the shaper gain and Tail Cancellation.
/Ref/ - reference voltage for the first stage of shaper.

Fig.1. KATOD-1 ASIC Block Diagram.

After preamplifier signal is split up in two passes: one via voltage follower to the trigger output (connected to the input of Trigger ASIC) and the other to the first stage of the shaper which provides controlled variation of the gain and rejection of the chamber current pulse tail.

Second and third stages of the shaper provide the additional amplification of the signal and rejection of the preamplifier tail. The output voltage follower is employed to increase the capacitive load driving capability.

In order to simplify the bias circuit of ASIC microwave *BJT-jFET* technology [4] has been supplemented with the lateral integrated *p-n-p* transistors.

2.1 Preamplifier

Main and reference preamplifiers have identical circuits (Fig.2) except output buffer (Q7,Q8). Charge Sensitive Preamplifier (CSP) is a single-stage common emitter cascode amplifier with active load (J1,Q1). Lateral *p-n-p* transistor Q1 provides simple adjustment and stability of J1 drain current which is set in the bias block by low-noise current mirror common to all channels.

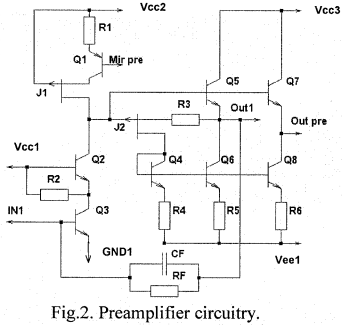


Fig.2. Preamplifier circuitry.

The nominal input transistor collector current 600μA is selected in order to minimize the noise and to provide the acceptable slew rate of the preamplifier output signal with the shaping time of 100ns and detector capacitance up to 200pF. The size of Q3 transistor is optimized in order to provide the low base resistance (r_{bb}<30 Ω). Values of the feedback elements (C_F=1.5 pF, R_F=50 kΩ) were obtained from the *Spice* circuit optimization in order to maximize the gain and in the same time to preserve stability, to speed up the response with the large enough amplitude range of the output signals. Q7 and Q8 transistors have the enlarged emitter areas to provide the pulse load current up to 25mA. The separate power supply buses V_{CC2} and V_{CC3} are used to decrease the undesirable on-chip stray feedback loops.

2.2 Shaper

Detector tail cancellation is realized as the subtraction of the low-frequency component of the preamplifier signal. In order to provide control of such function, the first stage of the shaper (Fig.3) is composed from the differential amplifiers (Q3,Q9 and Q6,Q12) coupled in parallel via the *Gilbert cells* (Q1,Q2,Q7,Q8 and Q4,Q5,Q10,Q11 respectively). The shaper First *Zero* is formed by the network (C3=7pF, R4=R5=R13=R14=500Ω and R6=R15=10kΩ) connected to emitters of Q3,Q9. The second amplifier (Q6,Q12) provides the DC amplification. The gain of amplifiers is controlled separately by the variation of the differential voltage on ASIC nodes (Cent1,2 and Side1,2), what in the same time depends on the voltages applied to the external pins /Gain/, /Tail/ and /Ref/ (Fig.1). According to the full symmetry of the schematic, the output signal of the second amplifier can be subtracted from the first one to provide the tunable rejection of the slow fraction of the detector signal.

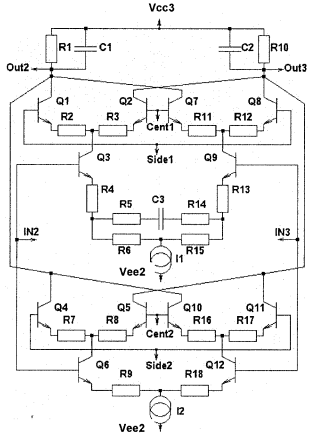


Fig.3. Shaper circuitry. Gain and Tail Cancellation control stage.

The first integration is achieved at the collector nodes OUT2 and OUT3 with the time constant t_{i1}=R1×(C1+C_{str1}+C_{str2})≈26.3ns. Where C_{str1}=0.502pF is the sum of the collector-base and collector-substrate capacitance of the Gilbert cells transistors. C_{str2}=0.0475 pF - is the distributed stray capacitance of the load resistor (R1 or R10). The stray capacitance of the MOS integrated capacitors C1,C2 is not affected on the integration time constant as soon as the semiconductor regions are connected to the V_{cc3} power supply bus. The t_{i1} dependence on the control voltages (because of the stray capacitance variation at the internal nodes OUT2 and OUT3) is small due to the voltage drop on the collector resistors. The stabilization of the DC collector voltage (and t_{i1}) could be achieved by application of the cascode transistors between the *Gilbert cells* and the output nodes, but in that case the supply voltage and power consumption would increase significantly. The differential signal from nodes OUT2 and OUT3 via the emitter followers is applied to the second stage of the shaper, formed by the differential amplifier Q6,Q11 (Fig.4). The shaper second *Zero* is formed by the network R6=R12=6kΩ, R7=R13=10kΩ, C4=3.75pF. The second integration time constant is equal to 24.8 ns. The third stage of the shaper consist of the differential amplifiers (Q7,Q9), (J1,J2) and the current mirror (Q4,Q8). This part of the shaper provides the third integration (27,9 ns), voltage amplification by the factor of 2 and conversion from the differential to the common-mode voltage.

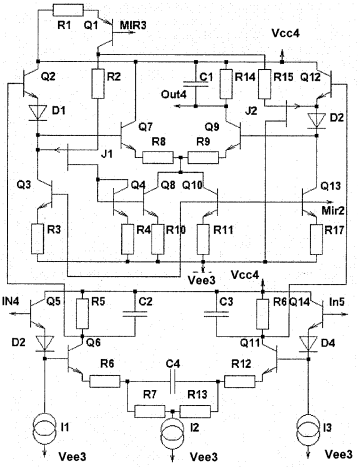


Fig.4. Shaper circuitry. Second and third amplifiers.

2.3 Output Buffer

The output stages of the shaper and preamplifier have identical circuitry (Fig.5). The main task of the shaper buster is to provide the desirable voltage slope both for the negative and positive output pulses with the load capacitance up to 50 pF and relatively low power consumption. The buffer has low input stray capacitance provided by the *J1* small area. In order to reduce the output impedance for the negative output pulse total transconductance both for the top and bottom gates of J1 is used as well as the additional amplification in the current mirror (Q1,Q3,R3,R4). The idling current is defined mainly by the resistors R2-R4. It is not affected by the DC output signal and weakly affected by the *p-jFET* static parameters dispersion.

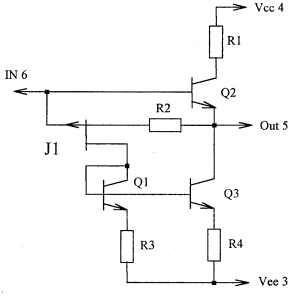


Fig.5. Output buffer circuitry.

3 Layout design, technology, fabrication

KATOD-1 is the full custom ASIC implemented with the 1.5μ microwave analog *Bi-jFET* technology [4], which have a feature allowing realization of the vertical *n-p-n*, vertical *p-jFET* and lateral *p-n-p* transistors without additional lithography steps. The passive components are include: Metal on Semiconductor (MOS) capacitors (with tolerance less than 20%) and active base *p+* resistors. The pad frame of the KATOD-1 is equal to 4,85×4,2 mm and die size to 5,2×4,6 mm (Fig.6). The size of the one channel is 220×4330 μm^2 (without pads). The channel width is limited by the pad size 100×100 μm^2 and by the admissible spacing between pads <60μm. For the best matching of the output DC levels of main and reference preamplifiers the active components as well as the integral resistors were placed in parallel with the minimal spacing.

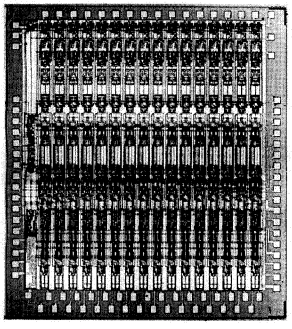


Fig.6. Layout of "KATOD-1" ASIC.

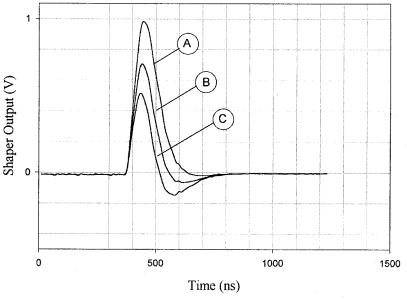


Fig.7. Measured delta current response to injected charge of 200fC, C_D=150pF.
A) U_{TAIL} = -2.4V; B) U_{TAIL} = -2.8V; C) U_{TAIL} = -3.2V.
U_{GAIN} = -2.4V and U_{REF} = -3.0V.

KATOD-1 topology design is based on the study of the components stray parameters influence on the CSP and Shaper characteristics [5,6]. In order to provide the best isolation of the channels and to minimize the substrate influence on the waveform, the following approaches was implemented:

- the MOS capacitors at the emitter nodes of differential amplifiers were formed in p+ region which was placed in the n^- well;
- the MOS capacitors at the collector nodes of all integrators were formed in the n+ region of the deep collector connected to the power supply bus;
- the special substrate contact was designed and placed around of each channel and around of some functional blocks (preamplifiers, shapers, output voltage followers). It was connected to the negative power supply bus in one point located close to the pad;
- all reference buses were shunted by the MOS capacitors with the maximal value. The MOS filter capacitor is more preferable than the other one which is based on the *p-n* junction, as soon as the significant *p-n* junction leakage current may affect on the bias block operation performance;

- to extend the field of the application, the most important resistors and capacitors, which define the gain, integration and differentiation time constants have been made as the component set. So in order to obtain the ASIC with the different shape of the output signal, gain *etc,* simple re-design of the only one metallization mask is required.

KATOD-1 ASIC was placed in the planar four-side 100-pin oxidized aluminum package.

4. Measurements

Fig.7 shows the delta current response of the ASIC to the injected charge of 200fC. Measurement was done with equivalent detector capacitance C_D=150pF. Voltage on the node Tail (U_{TAIL}) was adjusted to -2.4, -2.8 and -3.2V (traces A, B and C respectively) and the other control voltages were fixed: U_{GAIN}=-2.4V, U_{REF}=-3.0V (voltages on the external nodes GAIN and REF respectively).

Gain variation of KATOD-1 ASIC is possible in the range from –4.2mV/fC to +5.0mV/fC which can be optimized for the specific application (Fig.8). The gain ranges (for example between ~2mV/fC and 5mV/fC) is determined by external voltage U_{GAIN}. Another control voltage U_{TAIL} can be used to obtain desirable waveform of output signal. The output pulse voltage versus input charge is plotted in Fig.9. Measured non-linearity is less than 1% for the output pulse range of (0÷1.5)V.

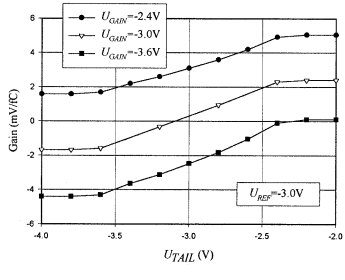


Fig.8. "KATOD -1" ASIC Gain vs. U_{TAIL}, for different gain ranges.

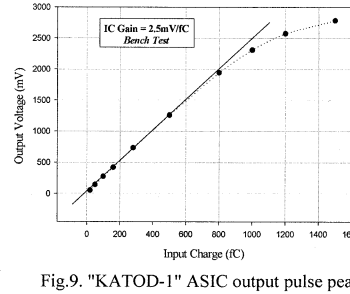


Fig.9. "KATOD-1" ASIC output pulse peak amplitude vs. input charge. (*Bench test*).

In order to model detector tail of the ion current, passive RC network is applied (Fig.10). The step response of the network, according to the *Spice* simulation, is a sum of the exponentially decaying current pulses (i_1 and i_2) which parameters can be calculated as:

$$i_1 \approx \frac{U_1}{R_1} \times \frac{C_3}{C_5} \quad (10)$$

$$i_2 \approx \frac{U_2}{R_2} \times \frac{C_6}{C_2} \quad (11)$$

$$\tau_1 \approx R_1 \times C_1 \quad (12)$$

$$\tau_2 \approx R_2 \times C_4 \quad (13)$$

where:

$U_{1,2}$ - the amplitude of the input voltage pulse;

$i_{1,2}$ - the peak amplitude;

$\tau_{1,2}$ - the time constant.

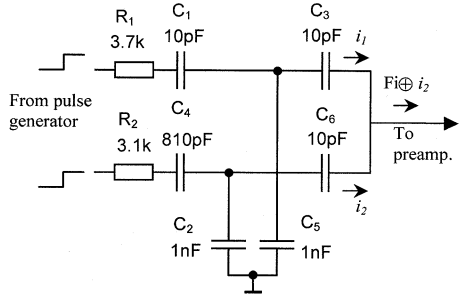


Fig.10. RC network for injecting a sum of two exponential current pulses into the ASIC input.

KATOD-1 ASIC response to the input current pulses (i_1/i_2=1%) and (i_1/i_2=10%) is shown in Fig.11 and Fig.12 respectively.

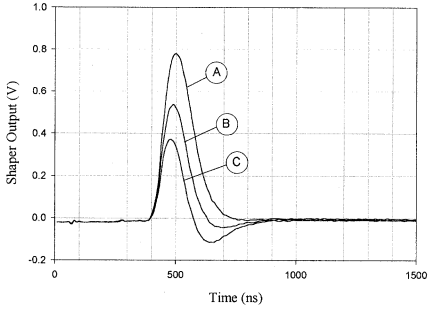


Fig.11. Measured output response to exponential current pulses.
i_1/i_2=1%. C_D=150pF; U_{GAIN} =-2.4V; U_{REF}=-3.0V.
A)U_{TAIL} =-2.4V; B)U_{TAIL}=-2.8V; C)U_{TAIL} =-3.2V.

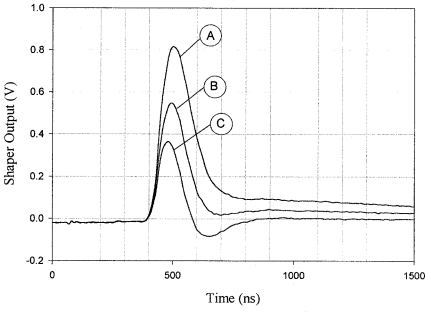


Fig.12. Measured output response to the exponential current pulses.
i_1/i_2=10%. C_D=150pF; U_{GAIN} =-2.4V; U_{REF}=-3.0V.
A)U_{TAIL} =-2.4V; B)U_{TAIL}=-2.8V; C)U_{TAIL} =-3.2V.

Detector tail cancellation tuning for desirable channel gain is realized by the adjustment the U_{GAIN} /U_{TAIL} ratio. For example, for the ratio of i_1/i_2=1% the pulse recovery time 600ns with overshoot ≈5% could be obtained when U_{GAIN}=-2.4V and U_{TAIL}≈-2.5V. For the ratio of i_1/i_2=10% the pulse recovery time of 600ns with overshoot ≈30% could be obtained with U_{GAIN}=-2.4V and U_{TAIL}≈-3.2V.

The typical performance characteristics of the KATOD-1 ASIC are summarized in Table 1.

Prototype of the 96 channels readout board was designed and tested on P0, P3 and P4 ME1/1 CSC prototypes of Endcap CMS muon station with cosmic rays in JINR (Dubna), and in the H2 and GIF beams at CERN.

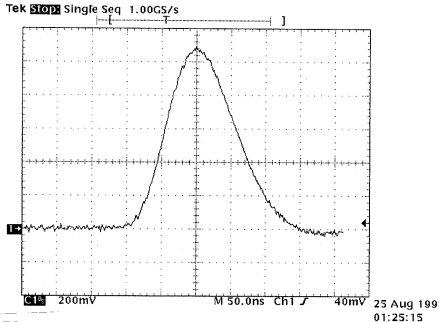


Fig.13. "KATOD-1" ASIC typical output signal in response to 225 GeV muons. (Beam tests of ME1/1 chamber P3 prototype at CERN (SPS).

Outputs of the KATOD-1 ASIC have been connected to the fast line driver to provide remote data handling. The KATOD-1 typical output signal for 225 GeV muons is shown in Fig.13. The peaking time of 100ns and pulse recovery time of 500ns were observed what fully agrees with simulation and bench tests results.

Table 1. Typical performance characteristics of the "KATOD-1" ASIC

V_{CC} supply voltage	+5V
V_{EE} supply voltage	-5V
Power consumption (per channel)	<17 mW
Time Constants:	
Peaking time (delta response, C_D=150 pF)	80ns
Peaking time (chamber signal response)	100ns
Recovery time (chamber signal response)	<600ns
Gain (*Controlled*)	(-4.2÷+5.0) mV/fC
Gain dispersion	<5%
Equivalent noise charge (C_D=0 pF), ENC	2400 *e*
noise slope (up to C_D=200 pF)	12 *e*/pF
Cross-talk (adjacent channels)	<1%
Non-linearity	<1% (0÷1.5V)

5. Conclusion

16-channels preamplifier-shaper ASIC for cathode readout of ME1/1 cathode strip chambers was designed and successfully tested. The aim of design was to meet the specific requirements of ME1/1 such as high spatial and timing resolution at the background rates >100 kHz per readout channel. Each readout channel includes pair charge sensitive preamplifiers with relatively small time constant of *RC* feedback, shaper with gain and tail cancellation control and output buffer. The noise performance is *ENC*=2400+12e/pF. Cross-talk level between adjacent channels is not exceeds 1% at C_D=150pF. Power consumption is less than 17mW per channel.

Simple and handy gain tuning as well as adjustment of the output signal shape provide the possibility of KATOD-1 ASIC application for different multi-channel detectors, especially if the fast enough shaping is needed.

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Голутвин И.А. и др. E13-2001-151
Интегральная схема «КАТОД-1» для считывания информации со стрипов катодной стриповой камеры

16-канальная интегральная схема (ИС) «КАТОД-1» была разработана для проведения тестов полномасштабных прототипов P3 и P4 камеры с катодным считыванием для передней мюонной станции ME1/1 эксперимента «компактный мюонный соленоид» (CMS). Канал регистрации ИС состоит из двух зарядочувствительных предусилителей, формирователя третьего порядка и выходного буфера. ИС имеет регулировку усиления в диапазоне (−4,2÷+5,0) мВ/фК и регулировку формы выходного импульса. Эквивалентный входной шум усилителя — 2400 эл. и наклон 12 эл./пФ в диапазоне емкостей детектора до 200 пФ. Время формирования выходного импульса ИС для сигнала от детектора — 100 нс. ИС изготовлена по технологии Bi-jFET.

Работа выполнена в Лаборатории физики частиц ОИЯИ.

Сообщение Объединенного института ядерных исследований. Дубна, 2001

Golutvin I.A. et al. E13-2001-151
The «KATOD-1» Strip Readout ASIC for Cathode Strip Chamber

The «KATOD-1», a 16-channels readout ASIC, has been designed to perform tests of P3 and P4 full-scale prototypes of the cathode strip chamber for the ME1/1 forward muon station of the Compact Muon Solenoid (CMS) experiment. The ASIC channel consists of two charge-sensitive preamplifiers, a three-stage shaper with tail cancellation, and an output driver. The ASIC is instrumented with control of gain, in the range of (−4.2÷+5.0) mV/fC, and control of output pulse-shape. The equivalent input noise is equal to 2400 e with the slope of 12 e/pF for detector capacity up to 200 pF. The peaking time is 100 ns for the chamber signal. The ASIC has been produced by a microwave Bi-jFET technology.

The investigation has been performed at the Laboratory of Particle Physics, JINR.

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