E10-2003-2

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READOUT LOGIC AND ITS HARDWARE IMPLEMENTATION IN THE **DIRAC** EXPERIMENT

Submitted to «Nuclear Instruments and Methods A»

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Логика считывания данных и ее аппаратная реализация
в эксперименте ДИРАК

Описываются логика считывания и архитектура аппаратуры съема данных эксперимента ДИРАК в ЦЕРН. Система сбора данных объединяет как специально разработанные, так и коммерчески доступные ветви считывания, работающие параллельно. Процесс считывания управляется триггерными процессорами, которые могут браковать событие во время его обработки. Малое мертвое время системы считывания обеспечивает достаточно высокую скорость приема данных.

Работа выполнена в Лаборатории ядерных проблем им. В. П. Джелепова ОИЯИ.

Препринт Объединенного института ядерных исследований. Дубна, 2003

Karpukhin V. V. et al. E10-2003-2
Readout Logic and Its Hardware Implementation
in the **DIRAC** Experiment

Readout logic and architecture of the readout hardware of the experiment DIRAC at CERN are described. The data collection system is configured from dedicated and commercial readout branches running in a parallel hardware-controlled mode. Readout process is controlled by trigger processors which may decide to reject an event during its acquisition. The system design provides a small dead time resulting in a sufficiently high rate capability.

The investigation has been performed at the Dzhelepov Laboratory of Nuclear Problems, JINR.

Preprint of the Joint Institute for Nuclear Research. Dubna, 2003

1 Introduction

In the experiment DIRAC [1] at CERN the lifetime of an atom $A_{2\pi}$ consisting of π^+ and π^- mesons has to be measured. This lifetime is directly connected with a difference of the pion scattering lengths $a_0 - a_2$ which is calculated within the framework of the chiral perturbation theory with a high precision but has not been measured experimentally with a sufficient accuracy.

The experiment is performed at the extracted 24 GeV proton beam of the PS accelerator. The beam hits the target followed by the magnetic spectrometer with detectors arranged in one upstream and two downstream arms, Fig.1. The upstream part contains the scintillating fiber detector (SFD), the microstrip gas chambers (MSGC) and the scintillation hodoscope (IH – ionization hodoscope) to measure ionization losses. The downstream arms include the drift chambers (DC), the scintillation

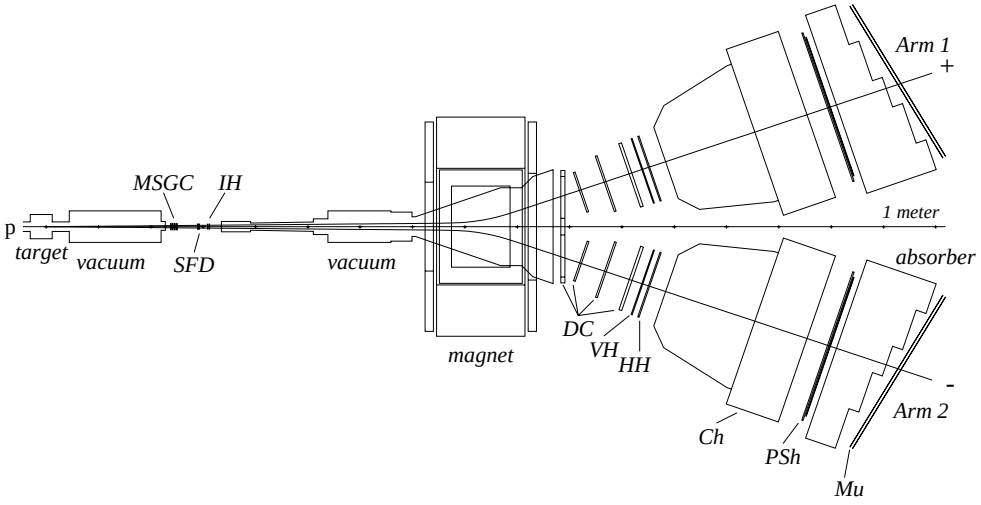

Fig.1. Schematic top view of the DIRAC spectrometer. Upstream of the magnet: microstrip gas chambers (MSGC), scintillating fiber detectors (SFD), ionization hodoscopes (IH). Downstream of the magnet, in each arm of the spectrometer: drift chambers (DC), vertical and horizontal scintillation hodoscopes (VH, HH), gas Cherenkov counter (CH), preshower detector (PSh) and, behind the iron absorber, muon detector (Mu).

hodoscopes (VH and HH) with vertically and horizontally oriented counters, the gas Cherenkov counters (Ch), the preshower detectors (PRs) and the muon counters (Mu) placed behind iron absorbers.

A pionic atom $A_{2\pi}$ disintegrates into a pair of positive and negative pions in the same target where it was produced and the resulting free pions with a very small relative momentum, $Q < 3\,MeV/c$, have to be detected in the experimental setup.

2 Trigger logic

The trigger logic [2] selects coincidences of low relative momentum pions in two downstream arms. Pion pairs are produced in the target mainly in a free state with rather high relative momenta. To decrease the trigger rate, a multilevel trigger is applied which selects pairs with low relative momenta.

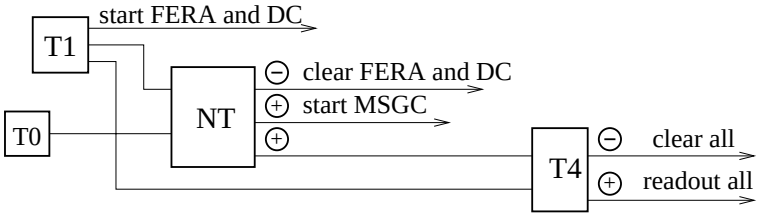

Fig.2. Scheme of the trigger. T1 is the first level trigger, T0 is the pretrigger. The encircled signs '+' and '–' denote positive or negative decisions of the trigger processors NT and T4, respectively.

The scheme of the trigger is shown in Fig.2. The first level trigger T1 [3] starts digitization in all data acquisition (DAQ) electronic modules (ADC, TDC, fast scalers and registers) except MSGC electronics. T1 also generates the Inhibit signal in order to prevent the DAQ system from further triggering until the end of the event processing. In parallel, the event data are analyzed in two hardware trigger processors, NT (Neural Trigger) and T4. NT is a neural network system[1] (described in [4]) which makes use of the hit patterns in the upstream IH and SFD detectors

[1]In this paper we use abbreviation NT for the neural trigger while in [2] and [4] it is named DNA (DIRAC Neural Atomic) and RNA (Revised Neural Atomic) trigger.

and downstream VH hodoscopes. For low relative momentum events, the hits in these detectors should be correlated and the corresponding dependences are implemented into the neural network algorithm. NT is started by a simple fast pretrigger T0 and takes decision in 250 ns. The rejection factor of NT is close to 2.

The processor T4 handles the data from the drift chambers. First it reconstructs straight tracks in the X-projection of the drift chambers and then compares the track parameters in the left and right arms to select events with low relative momenta. Decision time of T4 depends on the complexity of the event and is 3.5 μs on average. The rejection factor of T4 is 5–6 with respect to T1 or 2.5–3 with respect to NT.

In the case of a negative decision of NT or T4, the event is discarded and all registers are cleared to be ready for taking new data. If a positive decision of NT is followed by a positive decision of T4, the event is accepted and recorded.

3 Structure of the readout hardware

The beam is extracted to the channel in spills of duration 400–500 ms. In a 15–20 s supercycle of PS from one to several spills are delivered to the DIRAC setup, separated by not less than 1 s. During a spill the readout system of DIRAC should be able to collect up to 2000 events from the detectors of the setup, at a typical event size of 400–500 words. Thus an average interval between the events is 200–250 μs. However, a dead time of the readout system has to be much less to avoid large losses due to statistical distribution of events in a spill. The dead time of about 40 μs has been accepted as a reasonable value.

To meet this requirement, a parallel hardware-controlled configuration of the data collection system has been chosen. The data sources are grouped into branches in the way to achieve an approximately equal sub-event size in each branch. Each branch is connected to a separate VME buffer memory which accumulates the data from one spill. Readout of the buffer memories' content to the VME processor boards, event building and other relatively slow software operations are performed [5] in the intervals between the spills and between the supercycles.

The architecture of the readout hardware is shown in Fig.3. Data from different detectors are read out via 12 readout branches: 4 for

MSGC, 3 for DC and 5 for all other detectors. Readout of MSGC [6] and DC [7] is performed with dedicated electronics developed under responsibility of the University of Santiago de Compostela and JINR, Dubna, respectively. Other detector data are read out using the FERA system [8]. The FERA branches contain LeCroy modules ADC 4300B, TDC 3377 and universal logic modules 2366 configured as registers and scalers.

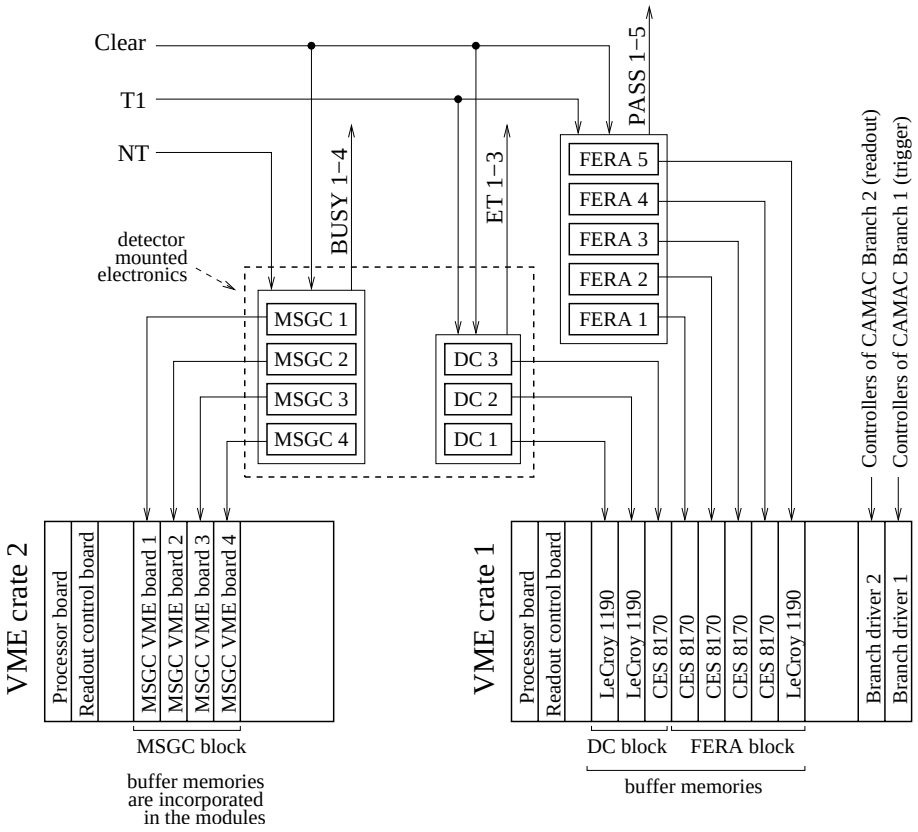

Fig.3. Readout hardware architecture.

Check of the data conformity in different branches and event building are fulfilled using event headers containing the trigger numbers. The dedicated electronics of DC and MSGC provides such event headers. In the FERA subsystem the modules 2366, implemented in each FERA branch, count the trigger numbers and the headers of 2366 serve as the event delimiters.

The VME buffer memories used are commercial CES 8170 and LeCroy

1190 units for FERA and DC branches. For MSGC data the buffer memories are incorporated into custom-made VME modules. Besides buffer memories and MSGC electronics, the VME crates contain the processor boards (8062 KA and RIO 8061), the readout control boards (RCB 8047) and two CAMAC branch drivers (CBD 8210). The first CAMAC branch of 7 crates controls the front-end, trigger and readout synchronization electronics, the second one of 5 crates is intended for controlling the data acquisition process in the FERA branches.

During a spill all the branches transmit the data in parallel at a rate of about 10 MHz under control of the readout synchronization system (RSS). The RSS produces the Readout Enable signal to start the event data transfer to VME buffer memories and then waits until the transfer in all the branches is completed. Upon receiving the individual end-of-readout signals (BUSY, PASS and ET in Fig.3) from all the branches, the RSS clears the data registers in the modules and then, with a guard pause, releases the Inhibit signal thus permitting to accept a new event.

4 Readout logic

Readout logic is controlled by synchronization signals from the accelerator and by signals of the trigger logic: the beginning and the end of a burst (BOB and EOB), the first level trigger (T1), positive or negative decisions of the trigger processors (NT and T4). In the interval between BOB and EOB only hardware readout operations are allowed for the DAQ system. The T1 signal starts digitization in the data acquisition modules. Negative or positive decisions of the neural trigger NT either clear an event or permit its further processing. The drift chamber processor T4 finally decides to clear or to accept an event.

High statistics is required in DIRAC to reach necessary precision of the pionic atom lifetime measurement and hence a lot of beamtime is consumed. To make the data taking more efficient, the readout logic is designed in the way to minimize deadtime losses coming from the operation time of the trigger processors and from the data transfer. Timing diagrams of the trigger and readout logic are presented in Figs.4–6 and commented below. Figure 4 is the diagram for accepted events, i.e. when both trigger processors decide positively. Figures 5 and 6 show the diagrams for events rejected by the trigger processors NT or T4, respectively.

The T1 signal starts acqusition of an event and immediately sends to the trigger system the Inhibit signal which is held until the end of the event processing, i.e. until the reset of the trigger after the event readout is completed or the Clear process is finished if the event is rejected by NT or T4. The Gate, Common Start and Common Stop signals to FERA modules and DC electronics are generated by the leading edge of T1. T1 also initiates a Measure Pause Interval (MPI) signal, whose duration defines the allowed interval to apply Fast Clear to FERA TDC 3377.

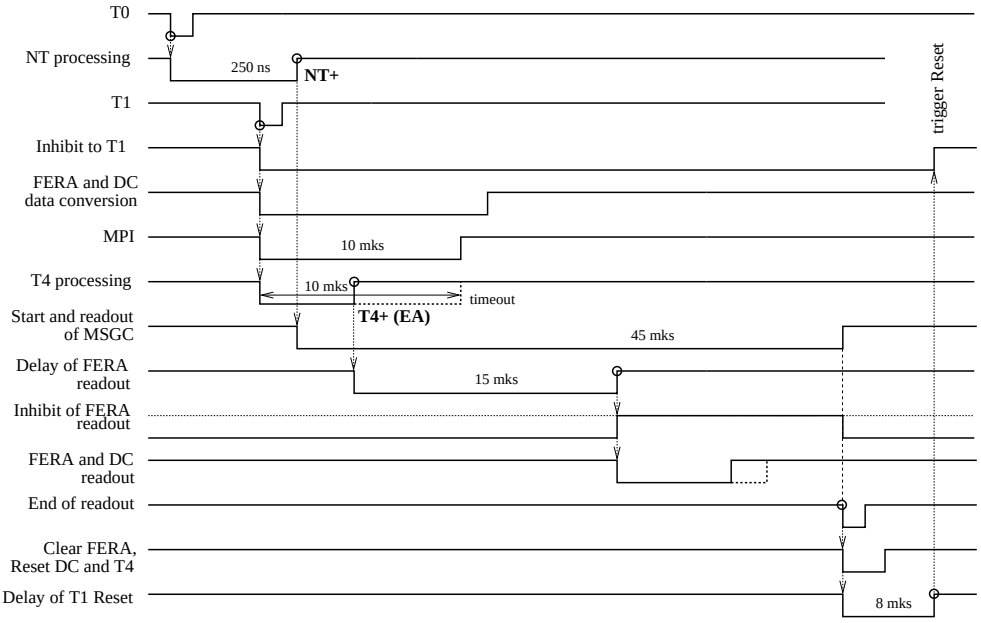

Fig.4. Time diagrams for accepted events. The pulse edge marked with a circle is the source of other transitions at this moment. (The same marks are used in Figs.5–6.)

The MSGC are started not by T1 but by a positive decision of the next level trigger NT. This is done in order to decrease the number of Clear signals applied to MSGC electronics (there is no Clear from NT negative decisions in this case) as its clearing takes more time. Hence, some dead time is saved.

A positive decision of NT is obligatory for processing the DC data at the next trigger level in the T4 processor. If the NT decision is negative,

a Fast Clear signal is sent to all branches except MSGC which was not started. The trigger Inhibit signal is released 8 μs later to allow finishing the Clear processes.

If the NT decision is positive, the T4 processor starts the data evaluation and takes decision to accept or to reject the event. For negative decisions, Fast Clear signals are generated and sent to all the branches. In this case release of Inhibit takes place with 13 μs delay with respect to the Clear signal.

The positive decision of T4 results in generation of the Event Accepted (EA) signal permitting the data transfer to buffer memories from the FERA and DC branches. Action of this signal is immediate for the DC system. The EA signal to the FERA system is delayed by 15 μs in order to come after the end of the conversion processes in the FERA modules, as on average EA is generated by T4 much earlier.

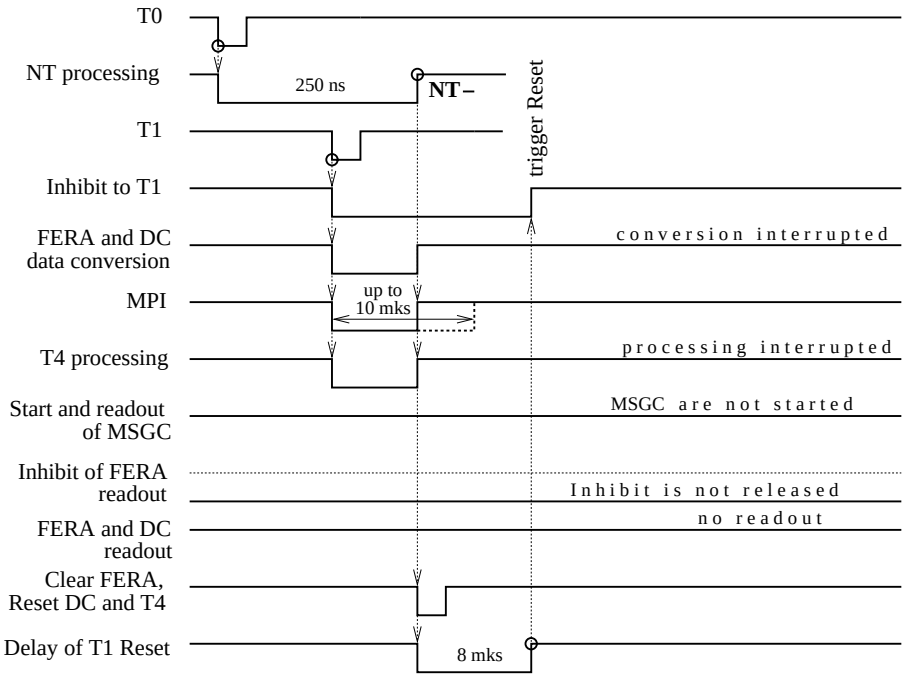

Fig.5. Time diagrams for events rejected by the neural trigger NT.

To increase noise immunity of the FERA system the Inhibit Readout level is almost permanently held at the corresponding FERA line. Inhibit Readout is released only for the period of the data transfer, i.e. from the delayed by 15 μs EA signal until the end of the event readout to buffer memories.

Different readout branches respond to Fast Clear in a different way. For the DC this signal may be applied at any time. For the MSGC system Fast Clear is only effective if it comes not later than 10 μs after T1. For this reason the 10 μs timeout limit is set in the T4 processor, so that if the decision is not taken yet within this interval, an event is accepted unconditionally and hence no Fast Clear may appear in later than 10 μs. The same value of 10 μs is given to a maximum duration of the MPI signal which is applied to the FERA system and defines the interval within which the FERA modules can be cleared. Really for rejected events the MPI signal is shorter because Fast Clear resets it.

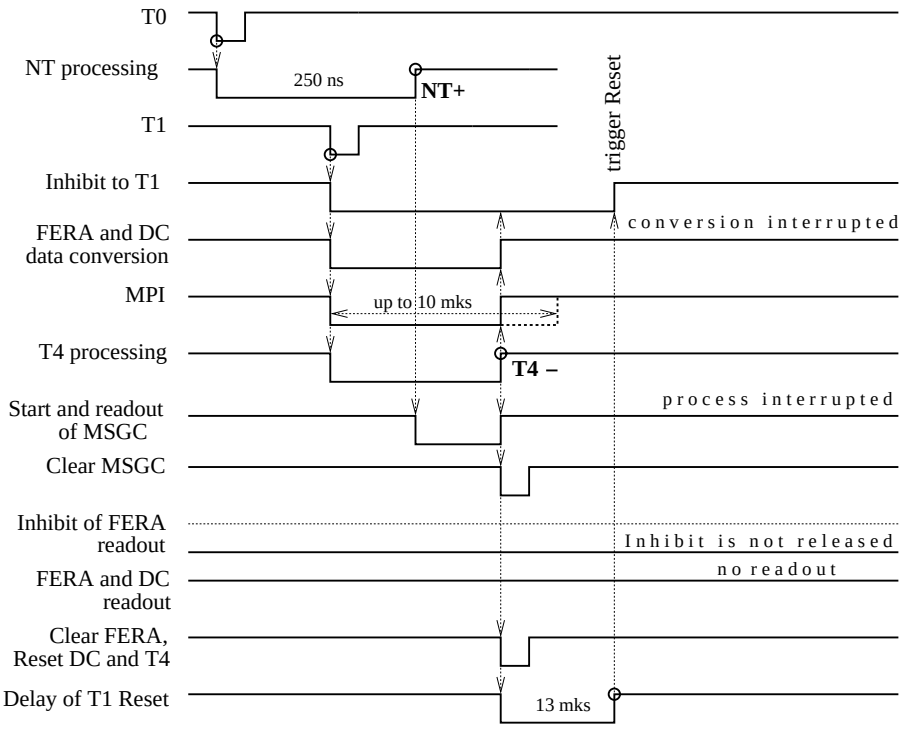

Fig.6. Time diagrams for events rejected by the drift chamber processor T4.

Operation of the DIRAC FERA system with multiple sources of Gates and Clear is described in more detail in [9].

A total processing time of an accepted event is defined by the branch with the longest data transfer time. At typical conditions of the data taking in DIRAC it is about 45 μs. This value is equal to a fixed readout time of MSGC which exceeds the conversion and data transfer time of other branches at standard conditions[2]. So, a dead time per accepted event is 45 μs. In case of disabling some of the branches, the processing time is defined by the rest of those enabled. If, for example, MSGC are disabled, a total acquisition time is decreased to about 30 μs.

A dead time coming from the NT negative decision is a sum of its fixed processing time (250 ns) and the time needed to clear FERA and DC modules and reset the trigger system, in total $\sim$ 8 μs per rejected event.

A dead time induced by the negative decision of T4 is equal to its non-fixed processing time (up to 10 μs, the average value is 3.5 μs) plus 13 μs for clearing all the branches (including MSGC) and resetting the trigger.

As mentioned above, at standard conditions of the data taking the rejection factors at different trigger levels are 2.0 for NT with respect to T1 and 2.5–3.0 for T4 with respect to NT. Then the rate of accepted events is 700–800 per 450 ms spill. At such conditions, the measured dead time introduced by all the readout processes and trigger processors is 13–14%.

The average volume of one event is $\sim$0.9 Kbyte, so about 0.7 Mbyte per spill is transferred to the buffer memories. This is well below the upper limit of the DAQ rate capability which is about 2 Mbyte (or $\sim$2000 events) per spill. This the rate capability is defined at present by the capacity of the buffer memories.

[2] At some types of calibration measurements the volume of data to be read out from the DC or FERA systems may greatly increase. In this case one of these subgroups defines the readout time.

5 Conclusions

Joint operation of the readout hardware consisting of different dedicated or commercial units is implemented in the described system. The readout process is controlled by the trigger processors which may decide to reject an event during its acquisition. Readout system design, developed in order to minimize the deadtime, provided a sufficiently high rate capability.

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