A High Precision Bandgap Reference Used in Power Management ICs

Gu Shurong*, Wu Xiaobo, Yan Xiaolang

***Abstract*—A 2.5V high precision BiCMOS bandgap reference with supply voltage range of 6V to 18V was proposed and realized. It could be applied to lots of Power Management ICs (Intergrated Circuits) due the high voltage. By introducing a preregulated current source, the PSRR (Power Supply Rejection Ratio) of 103dB at low frequency and the line regulation of 26.7μV/V was achieved under 15V supply voltage at ambient temperature of 27ºC. Moreover, if the proper resistance trimming is implemented, the temperature coefficient could be reduced to less than 16.4ppm/ºC. The start up time of the reference voltage could also be decreased with an additional bipolar and capacitor.**

***Index Terms*—bandgap reference, high precision , preregulate**

I. Introduction

In recent years, as the rapid development of modern communication and consumer products such like web servers, cellular phones and various PDA products, high quality power supplies that provides them suitable power are in great demand. As results, the research on power management ICs has become a new hot spot for IC designers. And voltage reference, as one of the key modules in power management ICs, is responsible for offering a precision reference voltage to other internal blocks such as regulator, comparators, error amplifiers, DAC (Digital Analog Converter), OSC (Oscillator) and etc. Sometimes, it also offers external reference voltage through an additional pin.

There is no doubt that at present low voltage and low power are two important design criteria in both analog and digital systems. It also brought new challenge to design of reference. Consequently, even sub 1V CMOS bandgap reference has been proposed [1] without introducing any special devices and technology. Some of them are constituted by use of parasitic vertical bipolar junction transistors (BJT) [1]. And others are based on the research of Filanovsky and Allam in 2001[2]. But due to the limit of technology and the fluctuations of the process, not all these theories became practice..

In this paper, a high precision 2.5V bandgap voltage reference with a new circuit topology is proposed, which is realized in BCD (Bipolar-CMOS-DMOS) technology. A preregulated circuit is introduced to supply a relatively stable voltage for the reference, which is also a PTAT current source. With a negative feedback loop the reference has a quick response once a fluctuation occurs in the output. The settling time is shortened with an additional bipolar and capacitor series. The supply voltage is between 6V and 18V, which is widely applied to power management ICs like PWM (Pulse Width Modulator) controller, APFC (Active Power Factor Correction IC) and etc. The key points of the layout design are also discussed.

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II. Proposed Reference Circuit

Different from the conventional bandgap voltage references, the proposed reference includes a preregulated circuit, which is self-biased by a cascode current mirror. The key bandgap structure requires only fewer transistors so that the chip area is reduced and the offset originated from device mismatches is also eliminated to a certain extent.

A. The Preregulated Circuit

A conventional bandgap reference is shown in Fig.1. An additional high gain, low offset amplifier was introduced to ensure the equality of voltage between node A and B. Besides, the sources of M1 and M3 connect directly to VDD, which brings transient noise to the circuit. The noise may be random or systematic in nature and its frequency components spread over broad spectrum range. The amplifier also increases the effective impedance looked from the sensitive nodes A and B to VDD and thus improves the PSRR of the circuit. At the same time, it increases the complex of the circuit.

In practice, one of effective approaches to achieve high PSRR is to preregulate the supply voltage VDD.. And by using buffer, noisy and fluctuations of power supply can be essentially isolated from the reference. Both of the measures are adopted in the proposed circuit.

A preregulated circuit is designed for the reference as shown in Fig.2. For this preregulator, the drain voltage of MP6 can be looked as a pseudo-supply whose fluctuations

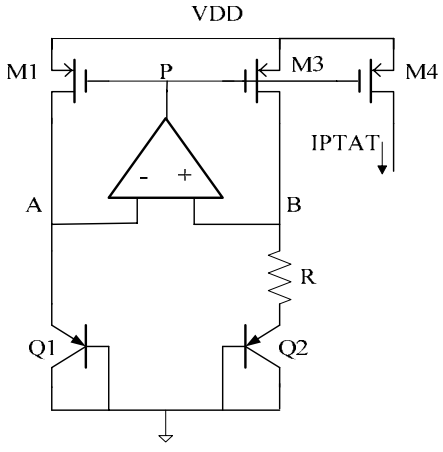

Fig.1 Conventional bandgap reference

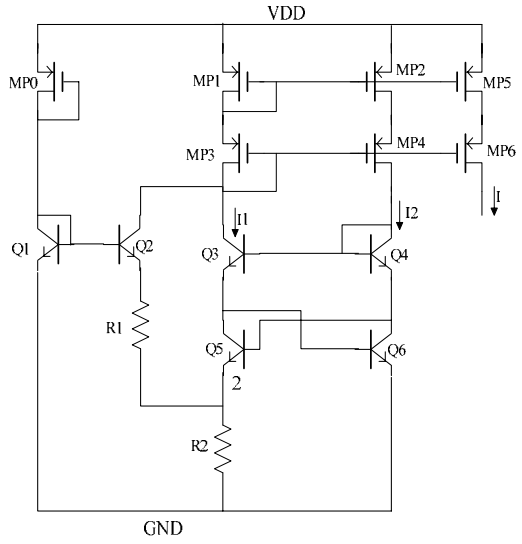

Fig.2 Preregulated circuit

are much smaller than VDD.

In Fig.2, MP0, Q1, Q2, and R_1 constitute a start-up circuit. Once the steady-state current is established in the current loop, the voltage drop across R_1 and R_2 is large enough to turn off Q2 and then disconnect the start-up circuit from the bias circuit. In practice, in order to turn off Q2 quickly, an aspect ratio of MP0 much less than unit was chosen and R_1 should be large enough.

After start up, a KVL equation around the base-emitter loop composed of Q3, Q4, Q5, Q6, and R_2 is given as

$$V_{BE3} + V_{BE6} = V_{BE4} + V_{BE5} + I_1 R_2 \tag{1}$$

Assuming that the transistors operate in the forward -active region, the base-emitter voltage V_{BE} is given as,

$$V_{BE} = V_T \ln(\frac{I_C}{I_S}) \tag{2}$$

where $V_T=kT/q$ is the thermal voltage and I_S is reverse saturation current, which is proportional to emitter area. Substituting (2) in (1) gives,

$$V_T \ln(\frac{I_{C3}}{I_S}) + V_T \ln(\frac{I_{C6}}{I_S}) = V_T \ln(\frac{I_{C4}}{I_S}) + V_T \ln(\frac{I_{C5}}{2I_S}) + I_1 R_2 \tag{3}$$

Assuming the MOS transistor MP1,2,3,4,5,6 have the same W/L ratio, neglecting the base current, and thus

$$I_{C3} = I_{C6} = I_{C4} = I_{C5} = I_1 = I_2 = I \tag{4}$$

$$I = \frac{V_T \ln 2}{R_2} \tag{5}$$

Here I is a PTAT current. In terms of the above equations, one can choose appropriate R to get the desired current and mirrored to different blocks of the chip.

A PTAT (Proportional to Absolute Temperature) current is intuitively a good choice for a diode current, which can partially compensate for the nonlinear logarithmic component of a diode voltage. It is obvious from the relation below. Notice that the logarithmic coefficient decreases as the order of I_D (χ) increases. The temperature dependence of a forward-biased diode is described by

$$V_D \approx V_{go} - \frac{T}{T_r}[V_{go} - V_D(T_r)] - (\eta - \chi) V_T \ln(\frac{T}{T_r}) \tag{6}$$

where V_{g0} is the forward voltage of the diode at 0K, T is Kelvin temperature, V_D (T_γ) is the voltage across the diode at reference temperature T_γ, η is a temperature-independent and process-dependent constant ranging from 3.6 to 4, and χ refers to the temperature dependence of the current forced through the diode ($I_D=DT^{\chi}$,, where D is a temperature independent constant and χ, equals 1 for a PTAT current).

For a bipolar transistor, the base-emitter voltage V_{BE} is a diode voltage, which is used in core bandgap circuit. So, the PTAT current flowing through MP6 into the bipolar transistor of bandgap and improves the temperature coefficient of the reference. Besides, other blocks of the overall control IC can also use it as a constant current source. but just the bandgap, which saves the chip area.

B. The Core of Bandgap Reference

The circuit above just provides the bias current and a pseudo-power supply. The key part of the bandgap reference is shown in Fig .3.

Here, Q11, Q12, R_3, and R_4 constitute the core bandgap. MOS transistors MP9 and MP10 whose sources and gates are connected respectively ensure that the current I_3 equals I_4 (Neglecting the channel length modulation). Thus from a KVL equation I_3 can be obtained as follows,

$$I_3 = \frac{V_{BE12} - V_{BE11}}{R_3} = \frac{V_T \ln n}{R_3} \tag{7}$$

where n is the emitter ratio of Q11 and Q12. Neglecting the temperature dependence of R_3, I_3 is a PTAT current since V_T

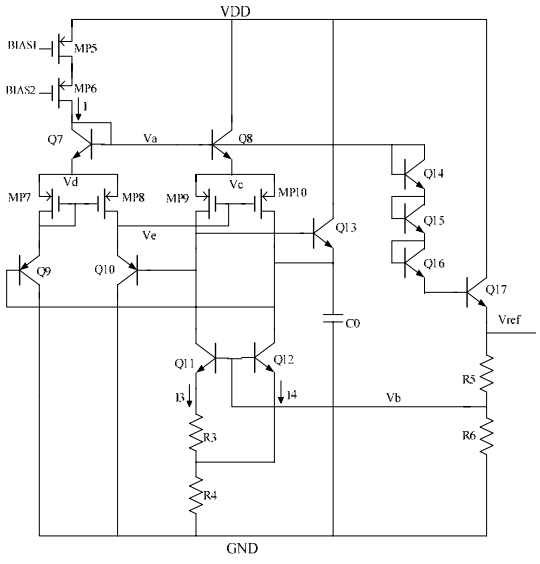

Fig.3 Proposed bandgap core circuit

has a positive TC (temperature coefficient) of +0.085mV/°C.

For I_3=I_4=I and R_4/R_3=m,

$$V_b = V_{BE12} + 2\mathrm{IR}_4 = V_{BE12} + 2\frac{\mathrm{V_T}\ln n}{R_3}R_4 = V_{BE12} + 2mV_T \ln n \quad (8)$$

where V_{BE12} has a negative TC of approximately -1.8mV/°C at 27°C (determined by the process). In theory, to get a temperature independent voltage V_{b}, it should be ensured

$$\frac{\partial V_b}{\partial T} = \frac{\partial V_{BE12}}{\partial T} + 2\frac{\partial V_T}{\partial T}\frac{R_4}{R_3}\ln n = -1.8 + 0.086 \times 2m \ln n = 0 \quad (9)$$

$$\Rightarrow m \ln n = 10.5 \quad (10)$$

In the circuit, n is set to 6, and m to approximately 5.8 (The exact value is due to the trimming results). In equation (9), $m\ln n$ is multiplied by 2, namely the positive item is twice as large as the conventional bandgap one, so that to get the zero temperature coefficient the required value of $\partial V_{\mathrm{b}}/\partial T$ is smaller. Moreover, trimming on the resistor R_4 can be done to achieve a best TC. The output V_{ref} can be expressed as,

$$V_{ref} = V_b \frac{R_5 + R_6}{R_6} = V_b\left(1 + \frac{R_5}{R_6}\right) \quad (11)$$

Therefore a scaled-up bandgap reference can be obtained by selecting an appropriate ratio of R_5 to R_6. To get a 2.5V reference voltage, it is good to set R_5=R_6.

C. *The Negative Feedback Loop*

In this circuit, Q17 is a power transistor, and a series of diode connected transistors are used to set up the internal stable voltage V_{a}, which is approximately four diode drops above V_{ref}. It constitutes a part of the feedback loop. Another part is constituted by two directly coupled pairs of Q11 and Q10, Q12 and Q9, respectively. The two parts well guarantee the stability of the reference output. Once changes of the load or the environment give rise to the rising of V_{ref}, V_{b} rises by the same amount for they have liner relationship. Since Q11 and Q12 work as common emitter reverse amplifiers, their collector will decrease, which results in the decrease of the gate voltage of MP7, 8, 9, 10 for Q9 and Q10 work as emitter followers. At the same time, the collector current of Q17 increases as V_{ref} goes up, so does the base current. For the bias current I from the cascade configuration is constant, the current flowing into the sources of MP7, 8, 9, 10 decreases. Thus the source voltages V_{d} and V_{c} are pulled down to decrease the $|V_{GS}|$. This will in turn pull down V_{ref} through the base-emitter voltages of Q8, 14, 15, 16, 17. As a whole, the output voltage will keep stable due to effects of the negative feedback loop.

In Fig.3 the transistor Q13 and capacitor C0 are used to speed up the settling time. Once the circuit is powered on, the emitter current of Q13 flows into the bandgap core to speed up the rising of the voltage V_{ref}. C0 is used to filter the input ripple.

III. LAYOUT DESIGN

The layout design is of key importance for the precision of the output reference voltage. There are some points should be paid attentions.

1) The ratio of R_3 to R_4 (but not their absolute values) determines the temperature performance of the reference directly. Thus, to get the best temperature compensation, resistor ratio trimming is needed. Here, R_4 with a 4-bit binary-weighted voltage trim scheme is chosen for the fuse trimming.
2) To improve resister matching, all matching resistors should be made up of the same material and have the same widths. Since some effects of process such like the lateral diffusion will introduce systematic mismatches to resistors having different widths. Furthermore, if accurate resistance rations are requested, it is best to constitute the resisters by groups of parallel or serial resisters with identical geometries, which will reduce the corner effects.
3) Common-centroid layout is applied to MP9 and MP10 to achieve best matching. It is beneficial to precision of the reference since the equality of the MOS pair determines the equality of the current I_3 and I_4, which is important to circuit precision.
4) As shown in equations (8) and (9), the emitter ratio of Q11 to Q12 is set to 6. To guarantee the precise ratio, Q11 is composed of six unity bipolar transistors and Q12 is composed of one. Their placement should also be taken care. Fig.4 is the whole layout of the reference shown in Fig.3.

IV. SIMULATION RESULTS

The proposed bandgap reference shown in Fig.3 has been simulated in Cadence Spectra with ABCD 150 library.

The temperature coefficient of the proposed reference at the supply voltage of 15V is about 16.4ppm/°C. Fig.5 shows that the output voltage varies 4.1mV at the most over the temperature ranges from -15°C to 85°C. When the supply voltage changes, the TC is just 38ppm/°C at the worst case.

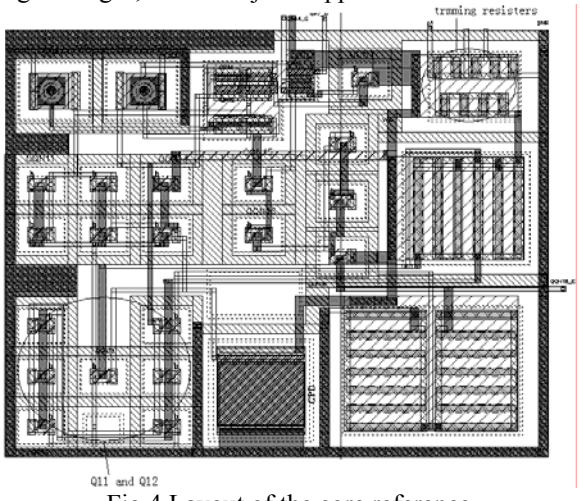

Fig.4 Layout of the core reference

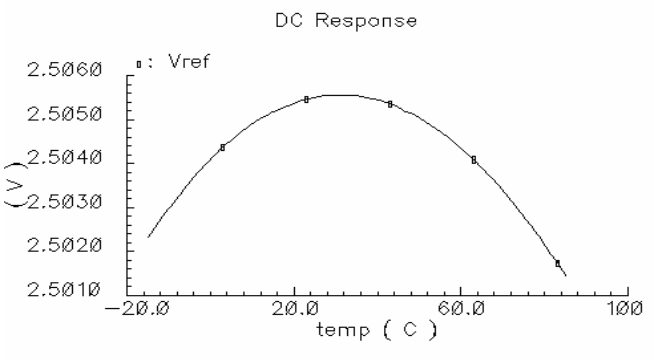

Fig.5 Reference voltage versus temperature

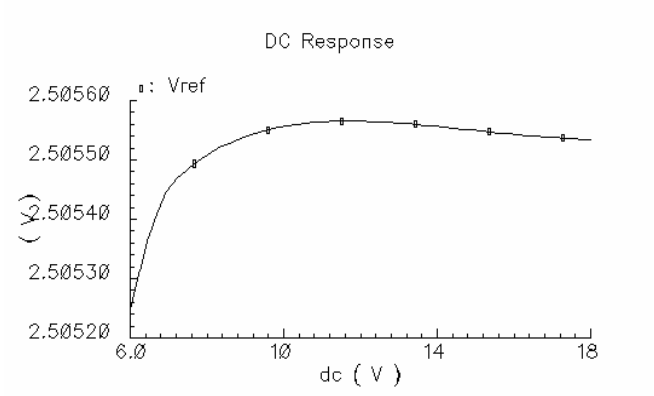

Fig.6 The line regulation of the reference

When the supply voltage changes from 6V to 18V, the variation of output voltage of 2.5V is within 320μV. That is to say, the line regulation is 26.7μV/V. The DC sweep results of the line regulation can be seen from Fig.5. It shows that the reference has a very high stability.

The power supply rejection ratio (PSRR) indicates the effects of the power supply ripple on the output. The PSRR of the proposed reference can be seen from Fig. 7, which is about 103dB at 100Hz.

V. CONCLUSION

A high precision bandgap reference was proposed in this paper. It can be applied to various power management ICs such as PWM controller, PFC and hot swap controller, etc. The inner preregulated circuit provides a relatively stable pseudo-power supply to the bandgap core as well as the PTAT bias current which can also be used in many other blocks of the ICs. The special design of the bandgap core made the PTAT voltage be twice as high as usual one, which reduces the ratio of the resisters and the bipolar transistors and results in saving chip area and increasing the ratio accuracy.

Other design issues involved in the feedback loops and layout were also discussed. Based on these ideas, a bandgap reference with TC of 16.4ppm/°C, PSRR of 103dB at 100Hz and line regulation of 26.7μV/V is developed and realized in 1.5μm BCD technology.

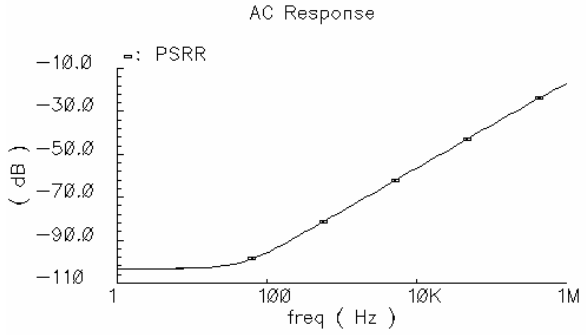

Fig.7 PSRR

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