Analysis of Hybrid Translinear Circuit and Its Application

Cheng Yuhua, Wu Xiaobo, Yan Xiaolang

***Abstract*—A hybrid translinear (TL) circuit constituted by two kinds of transistors, bipolar and CMOS transistors, was proposed to control its quiescent current. And a new method was introduced to analyze the hybrid TL circuit, which converted it into an uniform equivalent bipolar TL circuit. It simplified its analysis and design. This hybrid TL circuit is applied to the output stage of a class AB amplifier. The simulation results in 1.5μm BCD (Bipolar-CMOS-DMOS) technology were consistent with expectations well.**

***Index Terms*—translinear circuit, hybrid integrated circuit, differential pair, quiescent current control**

I. Introduction

The translinear principle proposed by Gilbert in 1975 is one of the important contributions to circuit theory in the electronics era [1]. Generalized translinear principle which applies to devices having transconductance linear with an electrical variable such as current or voltage has been proposed by [2]. In this paper the hybrid translinear circuit containing both bipolar and CMOS transistors was proposed and analyzed. And its application to the output structure of the class AB amplifier to control the quiescent current was given, which offered three types of output structure for comparison. All circuits were simulated in 1.5μm BCD (Bipolar-CMOS-DMOS) technology and the results are consistent with expectations well.

II. Hybrid Translinear Circuit

If the transconductance is linear with current, thus

$$g = dI / dV = aI \tag{1}$$

$$I = b\exp(aV). \tag{2}$$

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This is an exponential current-voltage characteristic of bipolar transistor or MOS transistor working in weak inversion.

If the transconductance is linear with voltage, it can be expressed as

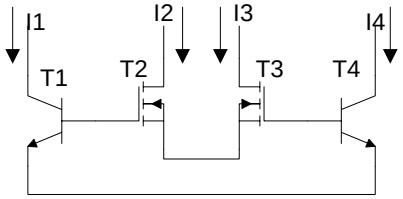
$$g = dI / dV = aV \tag{3}$$

$$I = AV^2 / 2 + B. \tag{4}$$

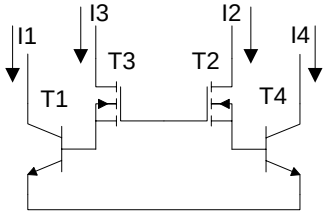
This is a square law current-voltage characteristic of MOS transistor working in strong inversion.

Although BTL (Bipolar TL) circuits are better in matching than MTL (MOS TL) ones due to their process, the advantage of MTL is that it can be easily adjusted by the aspect ratios of MOS transistors to achieve high accuracy, which is more convenient than BTL that is adjusted by the areas. Besides, the zero DC gate current of MOS transistor and low power dissipation are also its advantages. For MTL and BTL work in different manners, they have different appropriate applications. It was introduced in many papers.

It should be pointed out that in some situations it is difficult to satisfy the requirements by using onefold bipolar or CMOS transistor. So a hybrid TL circuit that consists of both CMOS and bipolar transistors is needed. Fig. 1 shows the basic structure of a hybrid translinear circuit which has two structures similar to MTL or BTL circuit respectively. One is up-down structure and the other is stacked structure. They fit the same equation according to kirchhoff's voltage law. That is

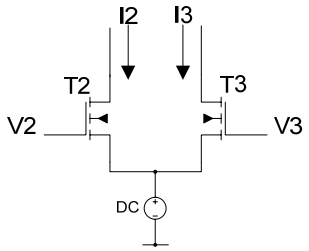


(a) Up-down structure

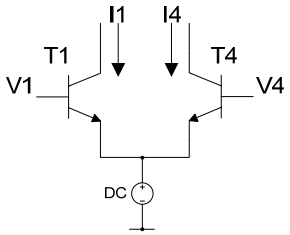


(b) Stacked structure

Fig. 1. Hybrid translinear circuit



(a)



(b)

Fig. 2. A model of HTL

$$V_{be1} + V_{gs3} = V_{be4} + V_{gs2} \tag{5}$$

$$V_{be1} - V_{be4} = V_{gs2} - V_{gs3}. \tag{6}$$

Changing from (5) to (6) will bring the benefit later. A model to analyze the HTL circuit will be proposed in section III.

III. A Model of TL Circuit

The TL loop shown in Fig. 1 can be divided into two differential pairs because the currents of I_1 plus I_4 and I_2 plus I_3 are always kept constant (i.e. the tail current is kept constant ideally). So the hybrid TL is divided into two differential pairs which are shown in Fig. 2. Similarly, the stacked structure can also be divided as shown in Fig. 2 since the input signals of the sources of T2 and T3 are equivalent to that of the gates of T2 and T3. Both they change the V_{gs} but in different ways.

From Fig. 2(a) it can be seen that

$$2I_{tail1} / \beta = (V_{gs2} - V_{TH})^2 + (V_{gs3} - V_{TH})^2. \tag{7}$$

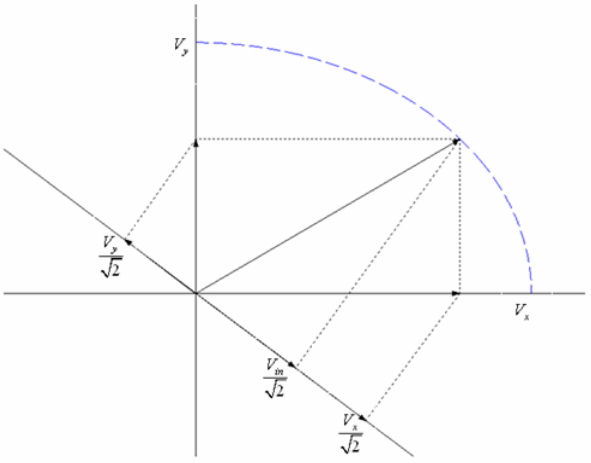
Bipolar differential pair working in weak inversion is similar to the MOS one. From Fig. 2(b) it can be derived:

$$2 = \exp(\frac{V_{be1} - V_0}{V_T}) + \exp(\frac{V_{be4} - V_0}{V_T}). \tag{8}$$

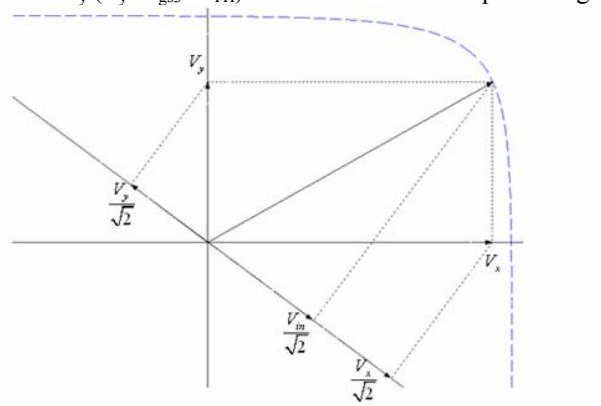
Here $V_0 = V_T ln(I_{tail2}/2)$.

The graphic models of a MOS differential pair in strong and weak inversion were proposed respectively [3]. That of the bipolar differential pair is similar to the weak inversion one. Fig. 3 shows the graph model of MOS differential pair in strong inversion and that of bipolar one respectively.

Although two curves are different due to their different laws,



(a) The effective gate-source voltage V_x (V_x=V_{gs2}–V_{TH}) versus V_y (V_y=V_{gs3}–V_{TH}) and the differential input voltage V_{in}



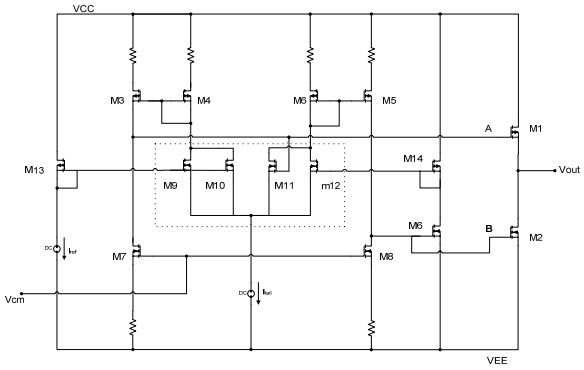
(b) The effective base-emitter voltage V_x (V_x=V_{be1}–V_0) versus V_y (V_y=V_{be4}–V_0) and the differential input voltage V_{in}.

Fig. 3. The graphic model of Fig. 2

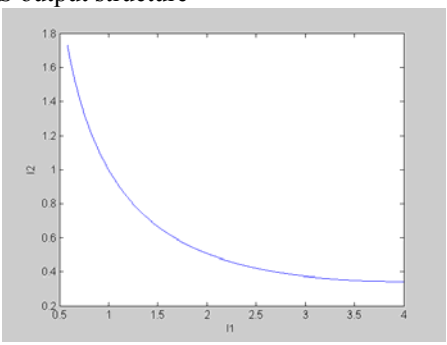
their trends are alike. If V_{in} is reflected in the new coordinate, the difference will be smaller. From (6) it is known that the equal V_{in} is the essential requirement and the two differential pairs can be replaced by each other while considering the voltage relationship. So MTL, BTL and HTL circuit could be uniform.

IV. Application In Class AB Output

An example is the translinear circuit used in the quiescent current control of the transistor in output stage. The CMOS output stage has been proposed in [4] and the schematic is redrawn in Fig. 4(a). The inferior performance of analog CMOS requires much more improvement measures to compensate for process inadequacies [5] which costs more and limits its application to other situations. The mismatch is the factor of the sensitivity of quiescent current [6]. Although the matching will be improved by using bipolar output transistors, the quiescent current will be larger that is unfortunate for power consumption. If it is used in BiCOMS process, HTL circuit can be chose. It maybe gets better performance. The output transistors use CMOS because the quiescent current can be

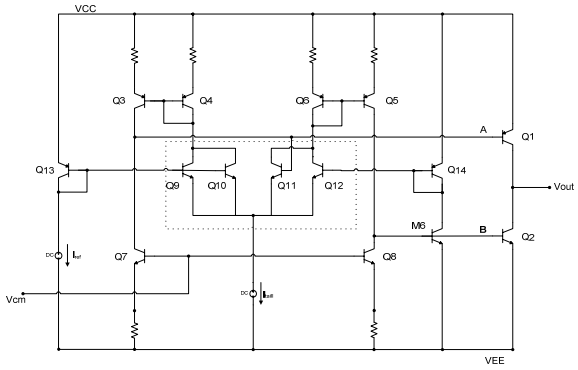


(a) CMOS output structure

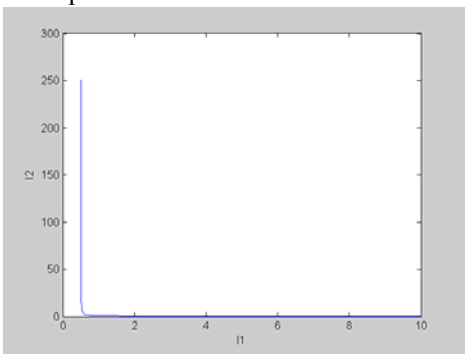


(b) *I*2 versus *I*1

Fig. 4. CMOS output stage



(a) Bipolar output structure



(b) *I*2 versus *I*1

Fig. 5. Bipolar output stage

controlled lower, more convenient and more accurate by adjusting the *W/L*. And the quiescent current control component uses bipolar to get better matching.

If $I_{ref}=I_9=I_{10}=1/4I_{tail}$, β_1-β_{13} are equal and $\beta_1=\beta_2$, with the MTL loops M1, M11, M14, M12 and M1, M11, M13, M9 in Fig. 4(a),

$$(\sqrt{\frac{I_{tail}}{\beta_{11}}}-\sqrt{\frac{I_1}{\beta_1}})^2+(\sqrt{\frac{I_{tail}}{\beta_{11}}}-\sqrt{\frac{I_2}{\beta_2}})^2=\frac{I_{tail}}{2\beta_{11}}. \tag{9}$$

The quiescent current is

$$I_q=\beta_1 I_{ref}/\beta_{13}=MI_{ref}. \tag{10}$$

And the residual output current while the other output transistor is heavily driven is found from (9):

$$I_{residual}=(\frac{1-\sqrt{2}}{2})^2 MI_{tial}. \tag{11}$$

M is the ratio of *W/L* of transistors M1 and M14, M2 and M6.

The output structure composed by fully bipolar transistors is shown in Fig. 5(a).

The BTL loops Q1, Q11, Q14, Q12 and Q1, Q11, Q13, Q9 are similar to the MTL loops in Fig. 5(a). It can be derived that

$$I_1 I_2/(I_1+I_2)=MI_{ref}/2. \tag{12}$$

It is a harmonic-mean value. The quiescent current and residual current are

$$I_q=MI_{ref} \tag{13}$$

$$I_{residual}=\frac{M}{2}I_{ref}. \tag{14}$$

The mixed output structure constituted by both bipolar and CMOS transistors is shown in Fig. 6(a).

With the HTL loops M1, Q11, M14, Q12 and M1, Q11, M13, Q9, it can be derived that

$$1/\exp(\frac{\sqrt{\frac{2I_1}{\beta_1}}}{V_T})+1/\exp(\frac{\sqrt{\frac{2I_2}{\beta_2}}}{V_T})=2/\exp(\frac{\sqrt{\frac{2I_{ref}}{\beta_{13}}}}{V_T}). \tag{15}$$

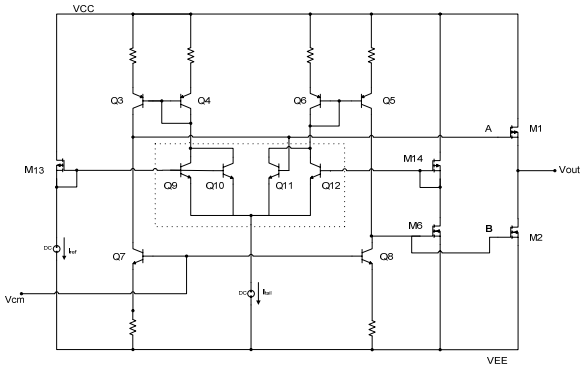
The quiescent current and residual current are

$$I_q=MI_{ref} \tag{16}$$

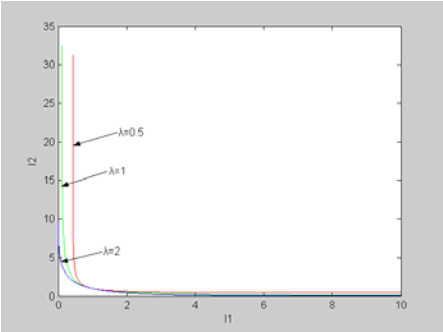
$$I_{residual}=\beta_1(\sqrt{2I_{ref}/\beta_{13}}-V_T\ln 2)^2/2 \tag{17}$$

It can be seen that the quiescent currents in three cases are all equal, and their residual currents are not too small to cut off the output transistor while other transistors are under heavy driving. They are determined by equation (9), (12), (15).

Normalizing the three equations and defining $I_q=MI_{ref}=1$, the equations (9), (12), (15) become (18), (19), (20) respectively.



(a) BiCMOS output structure



(b) $I2$ versus $I1$

Fig. 6. BiCMOS output stage

$$(2-\sqrt{I_1})^2+(2-\sqrt{I_2})^2=2 \tag{18}$$

$$1/I_1+1/I_2=2 \tag{19}$$

$$\exp(\frac{1-\sqrt{I_1}}{\lambda})+\exp(\frac{1-\sqrt{I_2}}{\lambda})=2. \tag{20}$$

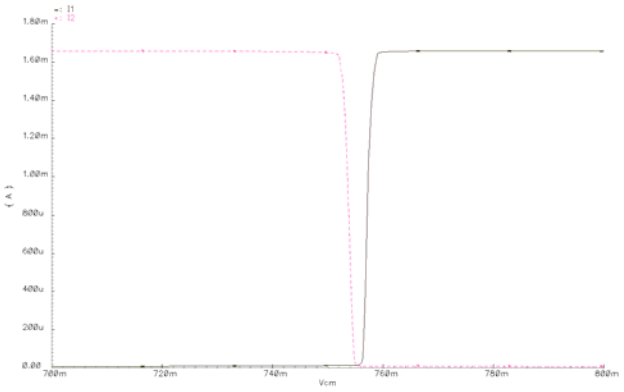
Here, $\lambda=\sqrt{2\beta_1}V_T$.

The minimum current of (18) is 0.34 times of quiescent current that accords to the depiction in [4].

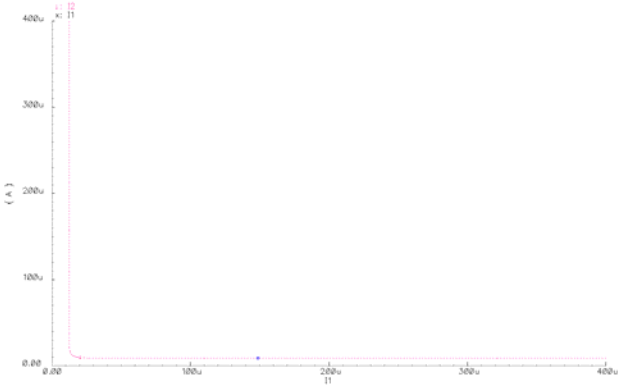
And the minimum current of (19) is $0.5I_q$. But the minimum current of (20) is not a certain value. It is about 0 - I_q.

The graphs of the three equations are depicted in Fig. 4(b), Fig. 5(b) and Fig. 6(b) respectively. All of them can reach quiescent current control. It approves the uniformity of MTL, BTL and HTL circuit. Moreover, it can be seen that the three curves have different ascending curvature and the exponential ones are steeper than the square law one. That means if BTL or HTL circuits with exponential curves are applied to current control, the more accurate quiescent current control is available. On the other hand, since MOS transistors have zero dc gate-source currents, the output circuits consisting of MOS devices have higher accuracy than bipolar ones. But bipolar circuits are better for matching and getting lower offset that is of importance to the fractional change in the quiescent current of the error amplifier [6].

As results, HTL circuit is the best choice for accurate and convenient quiescent current control.



(a) $I1$ and $I2$ versus V_{cm}



(b) $I2$ versus $I1$

Fig. 7 Simulation result of Fig. 6

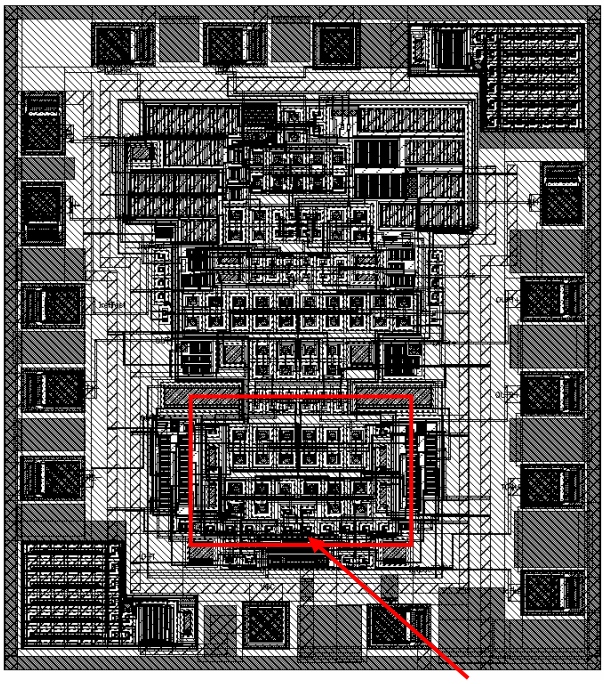


Fig. 8. Layout of the amplifier

V. Simulation Result

The output structure of Fig. 6(a) is simulated in 1.5μm BCD (Bipolar-CMOS-DMOS) technology. The simulation results

are shown in Fig. 7.

The minimum current is about 5μA ($0.5I_q$), and the maximum current is about 1.7mA. It is well consistent with the analysis results. The circuit was applied to a precision differential amplifier. The layout in 1.5μm BCD technology is shown in Fig. 8.

VI. Conclusion

In this paper, a hybrid TL circuit (HTL circuit) and a new method for TL circuit analyzing were proposed, which divides the HTL circuit into two differential pairs and converts them into an equivalent bipolar TL one to simplify its analysis and design. As example, three types of TL circuit were successfully uniformed. And an application of HTL circuit to the output stage of a class AB amplifier was developed. In comparison with onefold MTL or BTL circuit, it could get lower quiescent current variation and more accurate quiescent current control. The simulation results were given and it is proved that the results are consistent with the theoretical results accurately.

Acknowledgment

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