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## What is TWI? How to Configure the TWI for I2C Communication

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### Introduction

The Two-Wire Interface (TWI) is similar to the I<sup>2</sup>C interface with a few differences. The TWI peripheral provides an interface to components on a unique two-wire bus, consisting of one clock line and one data line. The TWI can be used with I<sup>2</sup>C compatible devices, such as a Real-Time Clock (RTC), memories, and sensors. Similar to I<sup>2</sup>C, the TWI supports standard speed (up to 100 kHz) and fast speed (up to 400 kHz) modes. Some SAM MCUs support high-speed for TWI, with speeds up to 3.4 MHz in slave high-speed mode, and in those products, the TWI peripheral is named TWIHS (TWI High Speed). The TWI is programmable as a master or slave.

The following table provides the features of the TWI compared to the standard I<sup>2</sup>C specification.

**Table 1. TWI Compatibility with I<sup>2</sup>C Standard**

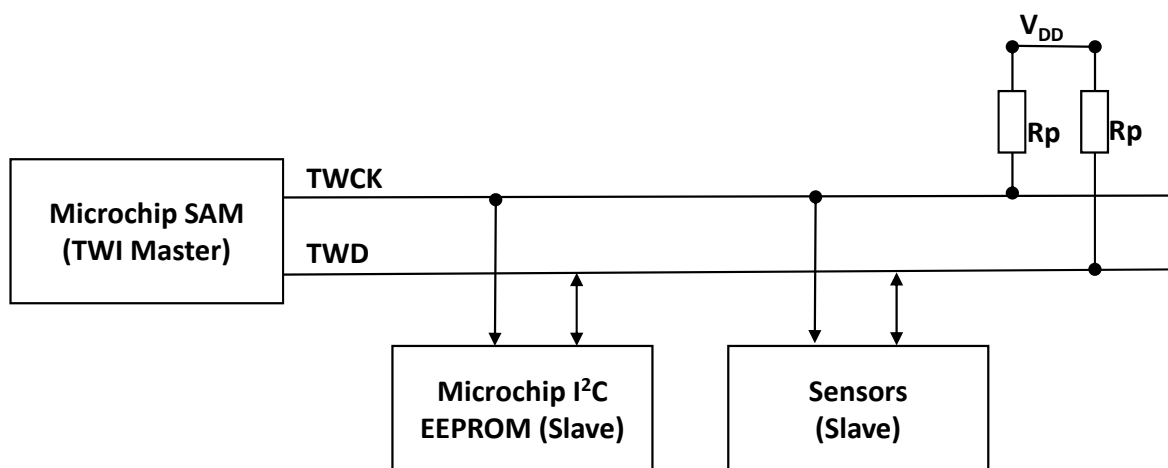
Standard I <sup>2</sup> C	TWI
7-bit or 10-bit Slave addressing, repeated Start (Sr) Condition, ACK and NACK management, multimaster capability, clock stretching	Supported
Input Filtering	Supported (Not supported for some SAM3/SAM4 devices)
START Byte (START + b000000001 + ACK + Sr), slope control	Not Supported

The TWI peripheral is available in the Microchip Cortex<sup>®</sup>-M3, Cortex-M4 and Cortex-M7 based MCUs. In some products, more than one instance of the TWI is available. For additional information, refer to the product data sheet.

## 1. TWI Pins, Data Formats, and Modes

The TWI pins, TWI Clock (TWCK) and TWI Data (TWD) are bidirectional lines, which are connected to a positive supply voltage using a current source or pull-up resistor. The value of the pull-up resistor is driven by the total capacitance of the bus, which includes the input capacitance of each slave, wire, connectors, PCB layout,  $V_{DD}$  of the bus, and the TWI bit rate. The number of slave devices that can be connected to the bus are limited only by the Maximum Bus Capacitive Loading ( $C_{bus}$ ). As per I<sup>2</sup>C standard, maximum  $C_{bus}$  value is 400pF. Since the low-to-high transition time (rise time or  $t_R$ ) is determined by the RC network formed by the pull-up resistor ( $R_p$ ) and bus capacitance, the  $R_p$  value has to be computed to match the rise time required by the I<sup>2</sup>C Standard. The  $R_p$  value can be computed using the speed and Rise time values given in the data sheet.

**Figure 1-1. SAM TWI Master and Slave Relationship Block Diagram**



**Note:** Due to the clock stretching capability of the TWI, the value of the pull-up resistors ( $R_p$ ) need to be computed correctly using the estimated bus capacitance. If the pull-ups are weak, the rise time will be higher, therefore resulting in a lower TWI speed.

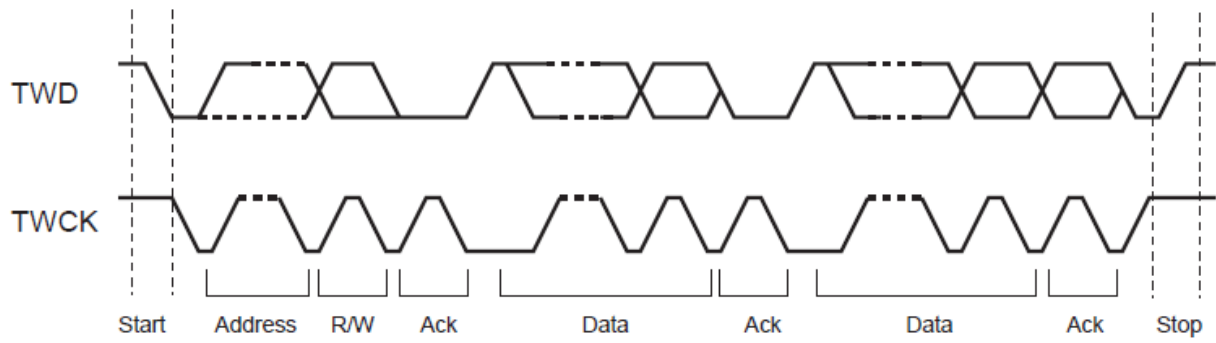
The SAM TWI devices (master or slave) have their input and output buffers powered at 3.3V. The interfaced I<sup>2</sup>C devices may operate at a different voltage. To know if you need to use level shifters, refer to the electrical specifications chapter in the data sheet to understand  $V_{IH}$ ,  $V_{IL}$  and  $V_{OL}$  parameters. The Cortex-M7 I/Os are not 5V tolerant. If a Cortex-M7 MCU is operating at 3.3V, and the TWI is interfaced with 5V TWI device, a level shifter is required.

Similar to I<sup>2</sup>C, the output stages of the devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function.

**Note:** There is no need to program the TWD and TWCK as open-drain. When TWI is enabled, the TWD and TWCK pins are configured as open-drain port mode by the hardware.

The TWI data transfer format is similar to the I<sup>2</sup>C data transfer format as shown in the following figure:

Figure 1-2. TWI Transfer Format



## 2. How to Configure the TWI

The TWI peripheral can be configured as shown in the following steps. The first three configurations are common for both master and slave modes.

**Note:** The Cortex-M7 MCU is used as an example. Some of the registers and bit names may be different for Cortex-M3 or Cortex-M4 MCUs. Refer to the data sheet for further information.

### TWI Common Configuration

The Configuration Steps are as follows:

1. Program the Parallel Input and Output Controller (PIO) to configure the TWD and TWCK as a peripheral pin.
2. Configure the Power Management Controller (PMC) to enable the TWIHS clock.
3. If the TWI is used in Interrupt Mode, program the Interrupt Controller before configuring the TWIHS. If not, this configuration is not needed.

### TWI Master Mode Configuration

The master write and read operation flow charts for various application examples may be found in the data sheet.

When the master reads the bytes from the slave, the master needs to Not Acknowledge (NACK) the last byte to generate the stop condition. To handle this scenario with the correct timing, it is recommended to set the STOP bit before reading the Receive Holding Register (TWIHS\_RHR) value for the second to last byte. If the master is reading only one byte, it is recommended to set the STOP bit when the re-start bit is set. If the stop condition is not set correctly, the slave will send an additional byte, or the bus will not be released for the next transaction.

In some devices (i.e., SAM4E), the repeated Start mode is handled automatically by the device, and there is no bit to control the repeated start. As soon as the internal address is set, the repeated start condition is automatically enabled.

**Trick:** There could be scenarios where the I<sup>2</sup>C/TWI communication hangs (bus error or wrong stop condition generation or detection), and the I<sup>2</sup>C bus remains in a busy state. In this condition, perform these actions:

1. Disable the TWI.
2. Reconfigure the TWCK pin in PIO output mode.
3. Generate nine clock pulses by the software to unlock the I<sup>2</sup>C bus.
4. Once the bus is free, enable the TWI.
5. Configure the TWCK pin as the TWI clock pin.

### TWI Slave Mode Configuration

The slave write and read operation flow charts for various applications are given in the data sheet.

After a Start or Repeated Start condition is detected from the master side, if the address sent by the master matches the slave address programmed in the Slave Address (SADR) field, the Slave Access (SVACC) flag is set and the Slave Read (SVREAD) indicates the direction of the transfer. After the SADR is received for TWI, the acknowledge management and data transmission is same as in I<sup>2</sup>C protocol. Refer to the reference section at the end of this document.

### TWI Clock Stretching

The clock is always controlled by the Master, but can be held low any time by any device on the bus. In this way, a Slave device can hold back a transaction if it needs more time to process the data. Due to the bus topology, the master cannot continue clocking if the SCL is held low. A slave pulling the SCL line low after the Master has released, it is said to perform *clock stretching*.

Some of the I<sup>2</sup>C masters and slaves support clock stretching, and others do not. In both situations, meeting the I<sup>2</sup>C bus timing is challenging. In these scenarios, the TWI interrupt priority should be configured high. If they are not configured high, there is a possibility that the MCU is processing other tasks and it might miss the I<sup>2</sup>C bus timings to process the next activity. Also the Interrupt service routine (ISR) needs to be written in such a way that the CPU is able to write or read the bytes quickly without taking much time.

Inside the ISR follow these steps:

1. Check for error status bits. If there is an error, handle it in a callback function.
2. Check if the TWI/ I<sup>2</sup>C is in transmitter or receiver mode.
3. If the TWI/ I<sup>2</sup>C is in transmitter mode:
  - 3.1. Send the data from the buffer.
  - 3.2. Increment the pointer.
4. If the TWI/ I<sup>2</sup>C is in receiver mode:
  - 4.1. Read the data and store it in the buffer.
  - 4.2. Increment the pointer.

The processing of the data can be done after the stop condition.

An example of clock stretching is shown in the following code sample. The code is for Slave mode in the SAMG55. In the SAMG55, the flexible communication unit (FLEXCOM) is available. The FLEXCOM can be configured as TWI, USART or SPI. The ISR routines are written to manage the various events.

### Clock Stretching Code Example

```
void FLEXCOM0_Handler(void)
{
    uint32_t status;
    status = TWI0->TWI_SR;
    /** ERROR Interrupt Management **/
    if (status & TWI_SR_OVRE)
        TWI_error_callback();
    if (status & TWI_SR_ARBLST)
        TWI_error_callback();
    /** TWI Read Access detected **/
    if ((status & TWI_SR_RXRDY)&&(status & TWI_SR_SVACC)) {
        TWI_read_callback();
    }
    /** TWI Read Access detected **/
    if (status & TWI_SR_EOSACC) {
        TWI_EOSACC_callback();
    }
    /** TWI Read Access detected **/
    if ((status & TWI_SR_SVACC)&&(status & TWI_SR_SVREAD)&&(status & TWI_SR_TXRDY)) {
        TWI_write_callback();
    }
}

/* TWI call-back to be modified according to Application need */
void TWI_EOSACC_callback(void)
{
    first_data = 1;
}

void TWI_write_callback(void)
{
    FLEXCOM0->FLEXCOM_THR = databuff[++intAddr];
}
```

```
}  
  
void TWI_read_callback(void)  
{  
    if (first_data) {  
        first_data = 0;  
        intAddr = FLEXCOM0->FLEXCOM_RHR;  
        FLEXCOM0->FLEXCOM_THR = databuff[intAddr];  
    } else {  
        databuff[intAddr++] = FLEXCOM0->FLEXCOM_RHR;  
    }  
}
```

Another method to manage clock stretching is to use the DMA. The DMA configuration steps are given in the data sheet.

### 3. Relevant Resources

- SAM E70 Datasheet: [http://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-11296-32-bit-Cortex-M7-Microcontroller-SAM-E70Q-SAM-E70N-SAM-E70J\\_Datasheet.pdf](http://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-11296-32-bit-Cortex-M7-Microcontroller-SAM-E70Q-SAM-E70N-SAM-E70J_Datasheet.pdf)
- AT91-AN01: Using the Two-wire interface (TWI) in Master Mode on AT91SAM Microcontrollers: <http://www.microchip.com/wwwappnotes/appnotes.aspx?appnote=en590839>
- In ASF 3.X, the TWI master implementation example uses the EEPROM as a slave. The TWI slave implementation example is available for the various Cortex-M3, Cortex-M4 and Cortex-M7 devices.
  - TWIHS MASTER Example for Cortex-M7: [http://asf.atmel.com/docs/3.34.1/sam.drivers.twihs.twihs\\_master\\_example.samv71\\_xplained\\_ultra/html/index.html](http://asf.atmel.com/docs/3.34.1/sam.drivers.twihs.twihs_master_example.samv71_xplained_ultra/html/index.html)
  - TWIHS Slave Example for High Speed Slave mode: [http://asf.atmel.com/docs/3.34.1/sam.drivers.twihs.twihs\\_slave\\_example.samv71\\_xplained\\_ultra/html/index.html](http://asf.atmel.com/docs/3.34.1/sam.drivers.twihs.twihs_slave_example.samv71_xplained_ultra/html/index.html)
  - TWI SLAVE Example in ASF 3.x: [http://asf.atmel.com/docs/latest/sam.drivers.twi.twi\\_slave\\_example.sam3u\\_ek/html/index.html](http://asf.atmel.com/docs/latest/sam.drivers.twi.twi_slave_example.sam3u_ek/html/index.html)
  - TWI EEPROM Example in ASF 3.x: [http://asf.atmel.com/docs/3.34.1/sam.drivers.twi.twi\\_eeprom\\_example.sam3x\\_ek/html/index.html](http://asf.atmel.com/docs/3.34.1/sam.drivers.twi.twi_eeprom_example.sam3x_ek/html/index.html)
  - Two-Wire Interface (TWI) in ASF 3.x: [http://asf.atmel.com/docs/latest/samg/html/group\\_sam\\_drivers\\_twi\\_group.html](http://asf.atmel.com/docs/latest/samg/html/group_sam_drivers_twi_group.html)

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