Intel® Itanium™ Processor Reference Manual for Software Development

Revision 2.0

December 2001

Document Number: 245320-003

Contents

Figures

Tables

About this Manual 1

The *Intel® Itanium™ Processor Reference Manual for Software Development* describes model-specific architectural features incorporated into the Intel® Itanium™ processor, the first processor based on the Itanium architecture. This document (Document number 245320) has been re-titled. In previous revisions, it was titled the *Intel® Itanium™ Architecture Software Developer's Manual, Volume 4: Itanium™ Processor Programmer's Guide.*

1.1 Overview of the *Intel® Itanium™ Processor Reference Manual for Software Development*

Chapter 1, "About this Manual" provides an overview of four volumes in the *Intel® Itanium Architecture Software Developer's Manual*.

Chapter 2, "Register Stack Engine Support" summarizes Register Stack Engine (RSE) support provided by the Itanium processor.

Chapter 3, "Virtual Memory Management Support" details size of physical and virtual address, region register ID, and protection key register implemented on the Itanium processor.

Chapter 4, "Processor Specific Write Coalescing (WC) Behavior" describes the behavior of write coalesce (also known as Write Combine) on the Itanium processor.

Chapter 5, "Model Specific Instruction Implementation" describes model specific behavior of Itanium instructions on the Itanium processor.

Chapter 6, "Processor Performance Monitoring" defines the performance monitoring features which are specific to the Itanium processor. This chapter outlines the targeted performance monitor usage models and describes the Itanium processor specific performance monitoring state.

Chapter 7, "Performance Monitor Events" summarizes the Itanium processor events and describes how to compute commonly used performance metrics for Itanium processor events.

Chapter 8, "Model Specific Behavior for IA-32 Instruction Execution" describes some of the key differences between an Itanium processor executing IA-32 instructions and the Intel® Pentium® III processor.

1.2 Terminology

The following definitions are for terms related to the Itanium architecture and will be used throughout this document:

Instruction Set Architecture (ISA) – Defines application and system level resources. These resources include instructions and registers.

Itanium Architecture – The new ISA with 64-bit instruction capabilities, new performance-enhancing features, and support for the IA-32 instruction set.

IA-32 Architecture – The 32-bit and 16-bit Intel Architecture as described in the *Intel Architecture Software Developer's Manual*.

Itanium System Environment – The operating system environment that supports the execution of both IA-32 and Itanium-based code.

IA-32 System Environment – The operating system privileged environment and resources as defined by the *Intel Architecture Software Developer's Manual*. Resources include virtual paging, control registers, debugging, performance monitoring, machine checks, and the set of privileged instructions.

Itanium-based Firmware – The Processor Abstraction Layer (PAL) and System Abstraction Layer (SAL).

Processor Abstraction Layer (PAL) – The firmware layer which abstracts processor features that are implementation dependent.

System Abstraction Layer (SAL) – The firmware layer which abstracts system features that are implementation dependent.

1.3 Related Documents

The following documents can be downloaded at the Intel's Developer Site at http://developer.intel.com:

- ***Intel® Itanium™ Processor Reference Manual for Software Development*** – This document (Document number 245320) describes model-specific architectural features incorporated into the Intel® Itanium™ processor, the first processor based on the Itanium architecture. This document has been re-titled and replaces the *Intel® Itanium™ Architecture Software Developer's Manual, Volume 4: Itanium™ Processor Programmer's Guide.*
- ***Intel® Architecture Software Developer's Manual*** – This set of manuals describes the Intel 32-bit architecture. They are readily available from the Intel Literature Department by calling 1-800-548-4725 and requesting Document Numbers 243190, 243191and 243192.
- ***Itanium™ Software Conventions and Runtime Architecture Guide –*** This document (Document number 245358) defines general information necessary to compile, link, and execute a program on an Itanium-based operating system.
- ***Itanium™ Processor Family System Abstraction Layer Specification*** – This document (Document number 245359) specifies requirements to develop platform firmware for Itanium-based systems.
- ***Extensible Firmware Interface Specification*** – This document defines a new model for the interface between operating systems and platform firmware.

1.4 Revision History

Date of Revision	Revision Number	Description
December 2001	2.0	Initial release of re-titled document. This document (Document number 245320) replaces the former *Intel® Itanium™ Architecture Software Developer's Manual, Volume 4: Itanium™ Processor Programmer's Guide*. Performance monitoring changes (Section 7.8). Revised Chapter 7 Performance Monitoring Events (new Section 7.6.5, Frontside Bus; added bus monitors to Section 7.8, Event List; misc. changes and fixes). Revised IBR and DBR addressing (Section 6.2.4). IA-32 related changes (Section 8). Miscellaneous performance monitoring events changes (Chapter 7).
July 2000	1.1	Reformatted the Performance Monitor Events chapter for readability and ease of use (no changes to any of the events except for renaming of some); events are listed in alphabetical order (Chapter 7).
January 2000	1.0	Initial release of document.

Register Stack Engine Support 2

2.1 RSE Modes

The Itanium processor implements the enforced lazy RSE mode. Refer to Chapter 6, “Register Stack Engine” in Volume 2 of the *Intel® Itanium™ Architecture Software Developer’s Manual* for a description of the RSE modes.

2.2 RSE and Clean Register Stack Partitions

On the Itanium processor, the internal RSE pointer RSE.BSPLoad is always equal to AR.BSPStore, meaning that the size of the clean register stack partition is always zero. This implies that, on the Itanium processor, a `flushrs` instruction will create a dirty region of size zero and an invalid region of size equal to 96 - CFM.sof. On other implementations that maintain a clean partition, `flushrs` behavior may differ by creating a clean register stack partition in addition to an invalid partition and a zero-sized dirty partition. As a result, the Itanium processor’s RSE may perform more mandatory fills upon a branch-return (`br.ret`) or `rfi` following a `flushrs` instruction than an implementation that maintains a clean partition.

Virtual Memory Management Support 3

3.1 Page Size Supported

The following page sizes are supported on the Itanium processor: 4K, 8K, 16K, 64K, 256K, 1M, 4M, 16M and 256M bytes.

3.2 Physical and Virtual Addresses

The Itanium architecture requires that a processor implement at least 54 virtual address bits and 32 physical address bits. The Itanium processor implements 54 virtual address bits (51 address bits plus 3 region index bits) and 44 physical address bits.

3.3 Region Register ID

The Itanium processor implements the minimum region register IDs allowed by the Itanium architecture. The region register ID contains 18 bits.

3.4 Protection Key Register

The Itanium architecture requires a minimum of 16 protection key registers, each at least as wide as the region register IDs. The Itanium processor implements 16 protection key registers, each 21 bits wide.

Processor Specific Write Coalescing (WC) Behavior 4

4.1 Write Coalescing

For increased performance of uncacheable references to frame buffers, previous Intel IA-32 processors defined the Write Coalescing (WC) memory type. WC coalesces streams of data writes into a single larger bus write transaction. Refer to the *Intel® Architecture Software Developer's Manual* for additional information.

On the Itanium processor, WC loads are performed directly from memory and not from coalescing buffers. It has a separate 2-entry, 64-byte Write Coalesce Buffer (WCB) which is used exclusively for WC accesses. Each byte in the line has a valid bit. If all the valid bits are true, then the line is full and will be evicted (or flushed) by the processor.

Note: WC behavior of the Itanium processor in the IA-32 System Environment is similar to the Pentium III processor. Refer to the *Intel® Architecture Software Developer's Manual* for more information.

4.2 WC Buffer Eviction Conditions

To ensure consistency with memory, the WCB is flushed on the following conditions (both entries are flushed). These conditions are followed when the processor is operating in the Itanium System Environment:

Table 4-1. Intel® Itanium™ Processor WCB Eviction Conditions

Eviction Condition	Intel® Itanium™ Instructions
Memory Fence (mf)	mf
Architectural Conditions for WCB Flush	
Memory Release ordering (op.rel)	st.rel, cmpxchg.rel, fetchadd.rel, ptc.g
Flush Cache (fc) hit on WCB	yes
Flush Write Buffers (fwb)	yes
Any UC load	no [a]
Any UC store	no [a]
UC load or ifetch hits WCB	no [a]
UC store hits WCB	no [a]
WC load/ifetch hits WCB	
WC store hits WCB	

a. Itanium architecture doesn't require the WC buffers to be coherent w.r.t to UC load/store operations.

4.3 WC Buffer Flushing Behavior

As mentioned previously, the Itanium processor WCB contains two entries. The WC entries are flushed in the same order as they are allocated. That is, the entries are flushed in written order. This flushing order applies only to a “well-behaved” stream. A “well-behaved” stream writes one WC entry at a time and does not write the second WC entry until the first one is full.

In the absence of platform retry or deferral, the flushing rule implies that the WCB entries are always flushed in a program written order for a “well-behaved” stream, even in the presence of interrupts. For example, consider the following scenario: if software issues a “well-behaved” stream, but is interrupted in the middle; one of the WC entries could be partially filled. The WCB (including the partially filled entry) could be flushed by the OS kernel code or by other processes. When the interrupted context resumes, it sends out the remaining line and then moves on to fill the other entry. Note that the resumed context could be interrupted again in the middle of filling up the other entry, causing both entries to be partially filled when the interrupt occurs.

For streams that do not conform to the above “well-behaved” rule, the order in which the WC buffer is flushed is random.

WCB eviction is performed for full lines by a single 64-byte bus transaction in a stream of 8-byte packages. For partially full lines, the WCB is evicted using up to eight 8-byte transactions with the proper byte enables. When flushing, WC transactions are given the highest priority of all external bus operations.

Model Specific Instruction Implementation 5

This section describes how Itanium instructions with processor implementation-specific features, behave on the Intel Itanium processor.

5.1 ld.bias

If the instruction hits L1D[1] or L2 cache and the state of the line is exclusive (E) or modified (M), the line is returned and remains in cache; no external bus traffic is generated. If the line is shared (S) or invalid (I) or the instruction misses the L2, it is treated as a store miss by the L3/bus. The line is returned and stored in E state by the processor in the L2 and L3 cache.

Please refer to page 3:135 in Volume 3 of the *Intel® Itanium™ Architecture Software Developer's Manual* for a detailed description of the `ld` instruction.

5.2 lfetch Exclusive Hint

The exclusive hint in the `lfetch` instruction allows the cache line to be fetched in an exclusive (E) state. On the Itanium processor, an `lfetch` transaction that has a snoop hit will be cached in an shared (S) state; otherwise, it is cached in an exclusive state.

Please refer to page 3:146 in Volume 3 of the *Intel® Itanium™ Architecture Software Developer's Manual* for a detailed description of the `lfetch` instruction.

5.3 fwb

The Itanium processor implements the flush write-back buffer (`fwb`) instruction. This instruction carries a weak memory attribute and causes the coalescing buffer to be flushed. The L1D and L2 store buffers are not flushed.

Please refer to page 3:126 in Volume 3 of the *Intel® Itanium™ Architecture Software Developer's Manual* for a detailed description of the `fwb` instruction.

1. The Itanium processor cache hierarchy consists of the following levels: on-chip L1I, L1D, L2 caches, and off-chip L3 cache.

5.4 thash

The Itanium architecture defines a `thash` instruction for generating the hash address for long format VHPT. `thash` is implementation specific. On the Itanium processor, since the hashing function is performed in the HPW, the HPW will generate the VHPT Entry which corresponds to the virtual address supplied. The hashing function is given in the following pseudo-code:

```
If (GR[r3].nat = ’1 or unimplemented virtual address bits) then {
GR[r1] = ’0 ;                          // treated as a speculative access.
GR[r1].nat = ’1;
}
else {
Mask = (2^PTA.size) - 1;
HPN = VA{50:0} >> RR[VA{63:61}].ps;   // Hash Page Number unsigned right shift.
                                      // mov 2 RR checks for supported ps
if (PTA.vf=32) {                      // 32B PTE (Long format)
    Hash_Index = HPN ^ (zero{63:18} || rid{17:0})
    VHPT_Offset = Hash_Index << 5 ;
}
if (PTA.vf=8) {                       // 8B PTE
    Hash_Index = HPN ;
    VHPT_Offset = Hash_Index << 3;
}
GR[r1] =  (PTA.base{63:61} << 61)
           || ([(PTA.base{60:15} & ~Mask{60:15}) ||
                  (VHPT_Offset{60:15} & Mask{60:15})] << 15)
           || VHPT_Offset{14:0} ;
}
}
```

Please refer to page 3:234 in Volume 3 of the *Intel® Itanium™ Architecture Software Developer’s Manual* for a detailed description of the `thash` instruction.

5.5 ttag

The Itanium architecture defines the `ttag` instruction for generating the tag for a long format VHPT entry. `ttag` is implementation specific. The HPW will generate the tag for the long format VHPT entry which corresponds to the virtual address supplied. The function is:

```
If (GR[r3].nat = ’1 or unimplemented virtual address bits) then {
GR[r1] = ’0 ;
GR[r1].nat = ’1;
}
else {
GR[r1] =(VA{50:0}>> RR[VA{63:61}].PS) ^
           ((zero{5:0} || RR[VA{63:61}].RID{17:0}) << 39);
}
}
```

Please refer to page 3:238 in Volume 3 of the *Intel® Itanium™ Architecture Software Developer’s Manual* for a detailed description of the `ttag` instruction.

5.6 ptc.e

On the Itanium processor, a single `ptc.e` purges all translation cache (TC) entries in both the instruction and data TLBs. The caches are not flushed.

Please refer to page 3:202 in Volume 3 of the *Intel® Itanium™ Architecture Software Developer's Manual* for a detailed description of the `ptc` instruction.

5.7 mf.a

In the Itanium architecture, the `mf.a` instruction is a memory acceptance fence for UC transactions only. On the Itanium processor, `mf.a` is implemented as an acceptance fence for both cacheable and UC data transactions (but not I fetches). The processor stalls until all data buffers in the L2 and bus are empty. This does not include buffers for instruction and L3 WB buffer in the bus request queue.

Please refer to page 3:149 in Volume 3 of the *Intel® Itanium™ Architecture Software Developer's Manual* for a detailed description of the `mf` instruction.

5.8 Prefetch Behavior

The Itanium processor does not initiate prefetches with post-increment loads.

5.9 Temporal and Non-temporal Hints Support

Itanium architecture provides memory locality hints for data accesses that can be used for allocation control in the processor cache hierarchy. For more details on this topic, please refer to Volume 1 of the *Intel® Itanium™ Architecture Software Developer's Manual*, Section 4.4.6. Implementation of locality hints is left as an implementation-specific feature on processors based on the Itanium architecture.

On the Itanium processor, four types of memory locality hints are implemented: t1, nt1, nt2 and nta. The Itanium processor does not support a non-temporal buffer; instead, non-temporal accesses are allocated in L2 cache with biased replacement.

Processor Performance Monitoring 6

This chapter defines the performance monitoring features on the Itanium processor. The Itanium processor provides four 32-bit performance counters, more than 50 monitorable events, and several advanced monitoring capabilities. This chapter outlines the targeted performance monitor usage models, defines the software interface and programming model, and lists the set of monitored events.

Itanium architecture incorporates architected mechanisms that allow software to actively and directly manage performance critical processor resources such as branch prediction structures, processor data and instruction caches, virtual memory translation structures, and more. To achieve the highest performance levels, dynamic processor behavior can be monitored and fed back into the code generation process to improve observed run-time behavior or to expose higher levels of instruction level parallelism. One can quantify and measure behavior of real-world Itanium-based applications, tools and operating systems. These measurements will be critical for compiler optimizations and the efficient use of several architectural features such as speculation, predication, and more.

The remainder of this chapter is split into the following two subsections:

- Section 6.1, "Performance Monitor Programming Models" discusses how performance monitors are used and presents various Itanium processor performance monitoring programming models.
- Section 6.2, "Performance Monitor State" defines the Itanium processor specific PMC/PMD performance monitoring registers.

6.1 Performance Monitor Programming Models

This section introduces the Itanium processor performance monitoring features from a programming model point-of-view and describes how the different event monitoring mechanisms can be used effectively. The Itanium processor performance monitor architecture focuses on the following two usage models:

- **Workload Characterization**: the first step in any performance analysis is to understand the performance characteristics of the workload under study. Section 6.1.1, "Workload Characterization" discusses the Itanium processor support for workload characterization.
- **Profiling**: profiling is used by application developers and profile-guided compilers. Application developers are interested in identifying performance bottlenecks and relating them back to their code. Their primary objective is to understand which program location caused performance degradation at the module, function, and basic block level. For optimization of data placement and the analysis of critical loops, instruction level granularity is desirable. Profile-guided compilers that use advanced Itanium architectural features such as predication and speculation benefit from run-time profile information to optimize instruction schedules. The Itanium processor supports instruction granular statistical profiling of branch mispredicts and cache misses. Details of the Itanium processor's profiling support are described in Section 6.1.2, "Profiling".

Whenever monitoring overhead is irrelevant, but accuracy is the primary objective, system and processor designers may resort to tracing processor activity at the system or the processor bus interface. However, trace based performance analysis and hardware tracing of the Itanium processor are beyond the scope of this documentation.

6.1.1 Workload Characterization

The first step in any performance analysis is to understand the performance characteristics of the workload under study. There are two fundamental measures of interest: event rates and program cycle break down.

- **Event Rate Monitoring**: Event rates of interest include average retired instructions-per-clock (IPC), data and instruction cache miss rates, or branch mispredict rates measured across the entire application. Characterization of operating systems or large commercial workloads (e.g. OLTP analysis) requires a system-level view of performance relevant events such as TLB miss rates, VHPT walks/second, interrupts/second or bus utilization rates. Section 6.1.1.1, "Event Rate Monitoring" discusses event rate monitoring.
- **Cycle Accounting**: The cycle break-down of a workload attributes a reason to every cycle spent by a program. Apart from a program's inherent execution latency, extra cycles are usually due to pipeline stalls and flushes. Section 6.1.1.4, "Cycle Accounting" discusses cycle accounting.

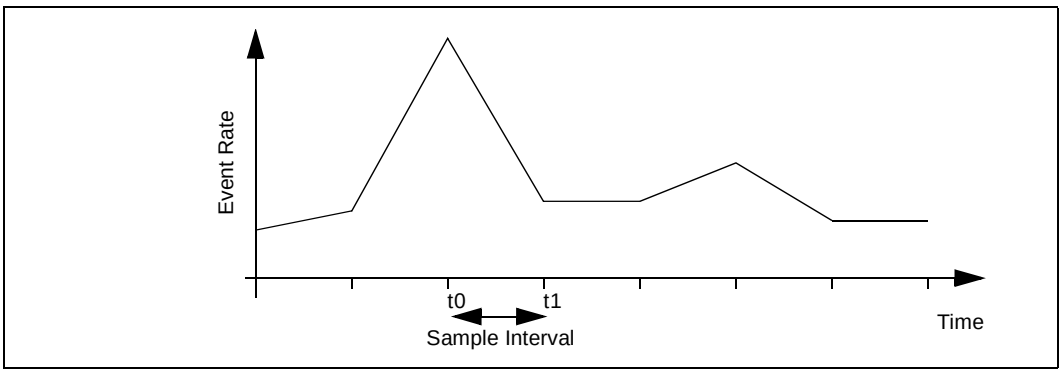
6.1.1.1 Event Rate Monitoring

Event rate monitoring determines event rates by reading processor event occurrence counters before and after the workload is run and then computing the desired rates. For instance, two basic Itanium processor events that count the number of retired Itanium instructions (IA64_INST_RETIRED) and the number of elapsed clock cycles (CPU_CYCLES) allow a workload's instructions per cycle (IPC) to be computed as follows:

$$IPC = (IA64\_INST\_RETIRED_{t1} - IA64\_INST\_RETIRED_{t0}) / (CPU\_CYCLES_{t1} - CPU\_CYCLES_{t0})$$

Time-based sampling is the basis for many performance debugging tools [VTune™, gprof, Windows NT*]. As shown in Figure 6-1, time-based sampling can be used to plot the event rates over time, and can provide insights into the different phases the workload moves through.

Figure 6-1. Time-based Sampling



On the Itanium processor, many event types (e.g. TLB misses or branch mispredicts) are limited to a rate of one per clock cycle. These are referred to as “single occurrence” events. However, in the Itanium processor multiple events of the same type may occur in the same clock. We refer to such events as “multi-occurrence” events. An example of a multi-occurrence events on the Itanium processor is data cache misses (up to two per clock). Multi-occurrence events, such as the number of entries in the memory request queue, can be used to the derive average number and average latency of memory accesses. The next two sections describe the basic Itanium processor mechanisms for monitoring single and multi-occurrence events.

6.1.1.2 Single Occurrence Events and Duration Counts

A single occurrence event can be monitored by any of the Itanium processor performance counters. For all single occurrence events a counter is incremented by up to one per clock cycle. Duration counters that count the number of clock cycles during which a condition persists are considered “single occurrence” events. Examples of single occurrence events on the Itanium processor are TLB misses, branch mispredictions, or cycle-based metrics.

6.1.1.3 Multi-occurrence Events, Thresholding and Averaging

Events that, due to hardware parallelism, may occur at rates greater than one per clock cycle are termed “multi-occurrence” events. Examples of such events on the Itanium processor are retired instructions or the number of live entries in the memory request queue. The Itanium processor’s four performance counters are asymmetrical. While all counters handle single-occurrence and multi-occurrence events with event rates up to three per cycle, only two counters can handle multi-occurrence events with event rates up to seven per cycle. For details, see Section 6.2.2, "Performance Counter Registers".

Thresholding capabilities are available in the Itanium processor’s multi-occurrence counters and can be used to plot an event distribution histogram. When a non-zero threshold is specified, the monitor is incremented by one in every cycle in which the observed event count exceeds that programmed threshold. This allows questions such as “for how many cycles did the memory request queue contain more than two entries?” or “during how many cycles did the machine retire more than three instructions?” to be answered. This capability allows micro-architectural buffer sizing experiments to be supported by real measurements. By running a benchmark with different threshold values, a histogram can be drawn up that may help to identify the performance “knee” at a certain buffer size.

For overlapping concurrent events, such as pending memory operations, the average number of concurrently outstanding requests and the average number of cycles that requests were pending is of interest. To calculate the average number or latency of multiple outstanding requests in the memory queue, we need to know the total number of requests (n_{total}) and, in each cycle, the number of live requests per cycle (n_{live}/cycle). By summing up the live requests (n_{live}/cycle) using a multi-occurrence counter Σnlive is directly measured by hardware. We can now calculate the average number of requests and the average latency as follows:

- Average outstanding requests/cycle = $\Sigma n_{live} / \Delta t$
- Average latency per request = $\Sigma n_{live} / n_{total}$

An example of this calculation is given in Table 6-1, in which the average outstanding requests/cycle = 15/8 = 1.825, and the average latency per request = 15/5 = 3 cycles.

Table 6-1. Average Latency per Request and Requests per Cycle Calculation Example

Time [Cycles]	1	2	3	4	5	6	7	8
# Requests In	1	1	1	1	1	0	0	0
# Requests Out	0	0	0	1	1	1	1	1
n_{live}	1	2	3	3	3	2	1	0
Σn_{live}	1	3	6	9	12	14	15	15
n_{total}	1	2	3	4	5	5	5	5

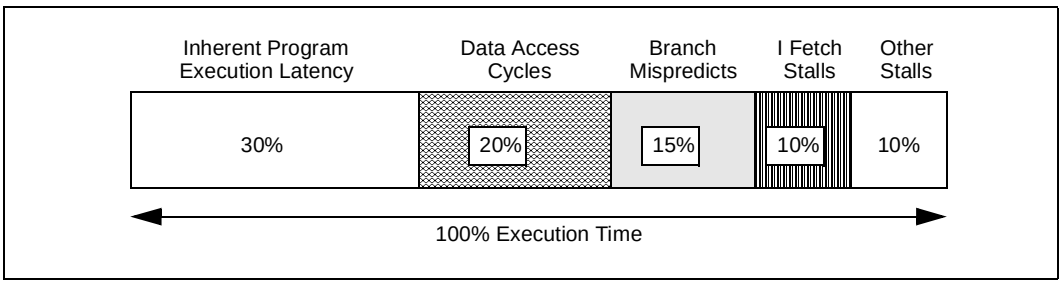
The Itanium processor provides the following capabilities to support event rate monitoring:

- Clock cycle counter
- Retired instruction counter
- Event occurrence and duration counters
- Multi-occurrence counters with thresholding capability

6.1.1.4 Cycle Accounting

While event rate monitoring counts the number of events, it does not tell us whether the observed events are contributing to a performance problem. A commonly used strategy is to plot multiple event rates and correlate them with the measured instructions per cycle (IPC) rate. If a low IPC occurs concurrently with a peak of cache miss activity, chances are that cache misses are causing a performance problem. To eliminate such guess work, the Itanium processor provides a set of cycle accounting monitors based on the Itanium architecture, that break-down the number of cycles that are lost due to various kinds of micro-architectural events. As shown in Figure 6-2, this lets us account for every cycle spent by a program and therefore provides insight into an application's micro-architectural behavior. Note that cycle accounting is different from simple stall or flush duration counting. Cycle accounting is based on the machine's actual stall and flush conditions and accounts for overlapped pipeline delays, while simple stall or flush duration counters do not. Cycle accounting determines a program's cycle break-down by stall and flush reasons, while simple duration counters are useful in determining cumulative stall or flush latencies.

Figure 6-2. Cycle Accounting in the Intel® Itanium™ Architecture



The Itanium processor cycle accounting monitors account for all major single and multi-cycle stall and flush conditions. Overlapping stall and flush conditions are prioritized in reverse pipeline order (i.e. delays that occur later in the pipe and that overlap with earlier stage delays are reported as being caused later in the pipeline). The eight stall and flush reasons are prioritized in the following order:

1. Back-end Flush Cycles: cycles lost due to branch mispredictions, ALAT flushes, serialization flushes, failed control speculation flushes, MMU-IEU bypasses and other exceptions.

2. Data Access Cycles: cycles lost when instructions stall waiting for their source operands from the memory subsystem, and when memory flushes arise (L1D way mispredictions, DTC flushes).
3. Scoreboard Dependency Cycles: cycles lost when instructions stall waiting for their source operands from non-load instructions; this includes FP-related flushes.
4. RSE Active Cycles: stalls due to register stack spills to and fills from the backing store in memory.
5. Issue Limit Cycles: dispersal breaks due to stops, port over-subscription or asymmetries.
6. Instruction Access Cycles: instruction fetch stalls due to L1I or ITLB misses.
7. Taken Branch Cycles: bubbles incurred on correct taken branch predictions.

Four of the eight categories (1, 2, 3, 6) are directly measurable as Itanium processor events. The other four categories (4, 5, 7, 8) are not measured directly. Instead, four combined categories are available as the Itanium processor events: pipeline flush cycles (1+7), memory cycles (2+4), dependency cycles (3+5), and unstalled back-end cycles (6+8). For details refer to Section 7.4, “Cycle Accounting Events” on page 50.

6.1.2 Profiling

Profiling is used by application developers and profile-guided compilers, optimizing linkers and run-time systems. Application developers are interested in identifying performance bottlenecks and relating them back to their source code. Based on profile feedback developers can make changes to the high-level algorithms and data structures of the program. Compilers can use profile feedback to optimize instruction schedules by employing advanced Itanium architectural features such as predication and speculation.

To support profiling, performance monitor counts have to be associated with program locations. The following mechanisms are supported directly by the Itanium processor’s performance monitors:

- Program Counter Sampling
- Miss Event Address Sampling: Itanium processor Event Address Registers (EARs) provide sub-pipeline length event resolution for performance critical events (instruction and data caches, branch mispredicts, instruction and data TLBs).
- Event Qualification: constrains event monitoring to a specific instruction address range, to certain opcodes or privilege levels.

These profiling features are presented in the next three subsections.

6.1.2.1 Program Counter Sampling

Application tuning tools like [VTune, gprof] use time-based or event-based sampling of the program counter and other event counters to identify performance critical functions and basic blocks. As shown in Figure 6-3, the sampled points can be histogrammed by instruction addresses. For application tuning, statistical sampling techniques have been very successful, because the programmer can rapidly identify code hot-spots in which the program spends a significant fraction of its time or where certain event counts are high.

Figure 6-3. Event Histogram by Program Counter

Program counter sampling points the performance analysts at code hot-spots, but does not indicate what caused the performance problem. Inspection and manual analysis of the hot-spot region along with a fair amount of guess work are required to identify the root cause of the performance problem. On the Itanium processor, the cycle accounting mechanism (described in Section 6.1.1.4, "Cycle Accounting") can be used to directly measure an application's micro-architectural behavior.

The Itanium architectural interval timer facilities (ITC and ITM registers) can be used for time-based program counter sampling. Event-based program counter sampling is supported by a dedicated performance monitor overflow interrupt mechanism described in detail in Volume 2, Section 7.2.2, "Performance Monitor Overflow Status Registers (PMC[0]..PMC[3])".

To support program counter sampling, the Itanium processor provides the following mechanisms:

- Timer interrupt for time-based program counter sampling.
- Event count overflow interrupt for event-based program counter sampling.
- Hardware supported cycle accounting.

6.1.2.2 Miss Event Address Sampling

Program counter sampling and cycle accounting provide an accurate picture of cumulative micro-architectural behavior, but they do not provide the application developer with pointers to specific program elements (code locations and data structures) that repeatedly cause micro-architectural "miss events". In a cache study of the SPEC92 benchmarks, [Lebeck] used (trace based) cache miss profiling to gain performance improvements of 1.02 to 3.46 on various benchmarks by making simple changes to the source code. This type of analysis requires identification of instruction and data addresses related to micro-architectural "miss events" such as cache misses, branch mispredicts, or TLB misses. Using symbol tables or compiler annotations these addresses can be mapped back to critical source code elements. Like Lebeck, most performance analysts in the past have had to capture hardware traces and resort to trace driven simulation.

Due to the super-scalar issue, deep pipelining, and out-of-order instruction completion of today's microarchitectures, the sampled program counter value may not be related to the instruction address that caused a miss event. On a Pentium processor pipeline, the sampled program counter may be off by 2 dynamic instructions from the instruction that caused the miss event. On a Pentium Pro processor, this distance increases to approximately 32 dynamic instructions. On the Itanium processor it is approximately 48 dynamic instructions. If program counter sampling is used for miss event address identification on the Itanium processor, a miss event might be associated with an

instruction almost five dynamic basic blocks away from where it actually occurred (assuming that 10% of all instructions are branches). Therefore, it is essential for hardware to precisely identify an event's address.

The Itanium processor provides a set of *event address registers* (EARs) that record the instruction and data addresses of data cache misses for loads, the instruction and data addresses of data TLB misses, the instruction addresses of instruction TLB and cache misses. A four deep *branch trace buffer* captures sequences of branch instructions. Table 6-2 summarizes the capabilities offered by the EARs and branch trace buffer. Exposing miss event addresses to software allows them to be monitored either by sampling or by code instrumentation. This eliminates the need for trace generation to identify and solve performance problems and enables performance analysis by a much larger audience on unmodified hardware.

Table 6-2. Intel® Itanium™ Processor EARs and Branch Trace Buffer

Event Address Register	Triggers on	What is Recorded
Instruction Cache	Instruction fetches that miss the L1 instruction cache (demand fetches only)	Instruction Address Number of cycles fetch was in flight.
Instruction TLB (ITLB)	Instruction fetch missed ITLB (demand fetches only)	Instruction Address Who serviced TLB miss: VHPT or software.
Data Cache	Load instructions that miss L1 data cache	Instruction Address Data Address Number of cycles load was in flight.
Data TLB (DTLB)	Data references that miss L1 DTLB	Instruction Address Data Address Who serviced TLB miss: L2 DTLB, VHPT or software.
Branch Trace Buffer	Branch Outcomes	Branch Instruction Address Branch Target Instruction Address Mispredict status and reason

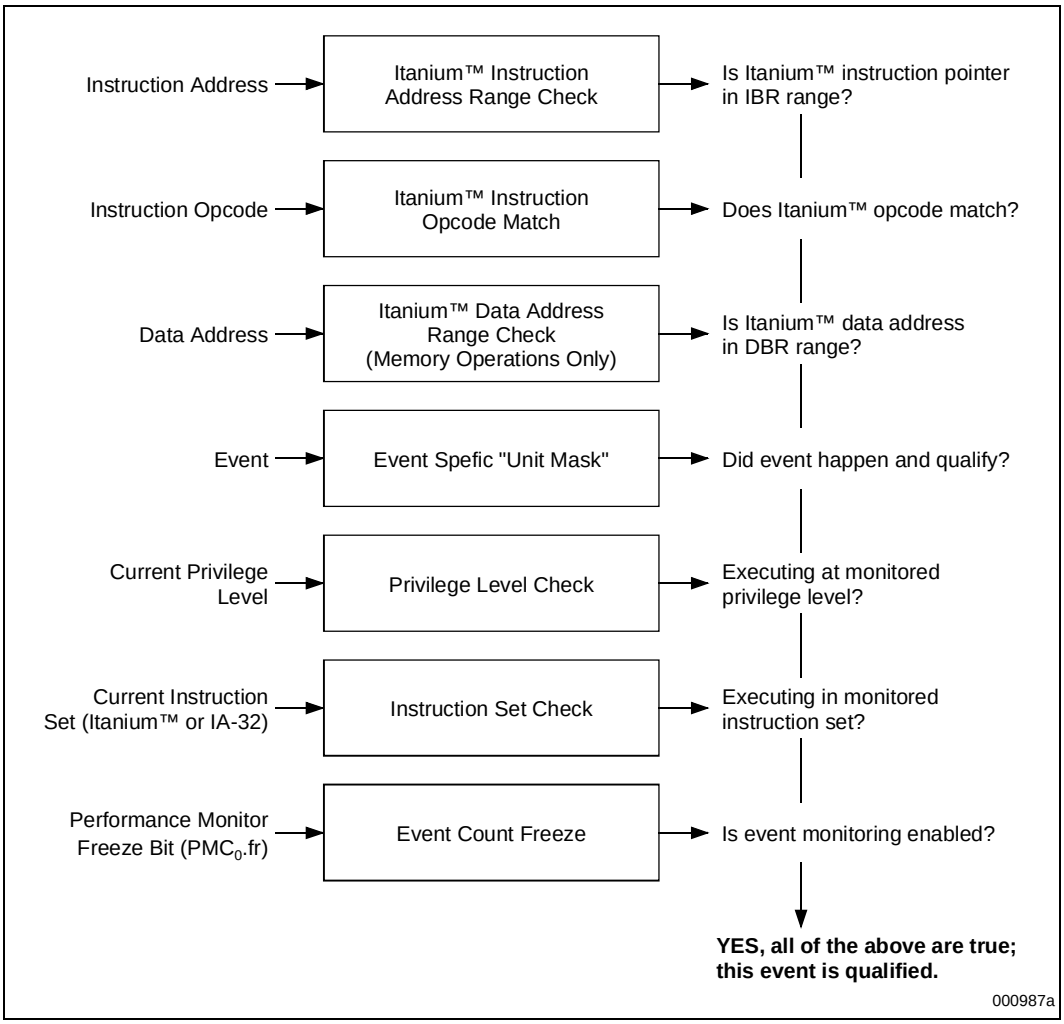
The Itanium processor EARs enable statistical sampling by configuring a performance counter to count, for instance, the number of data cache misses or retired instructions. The performance counter value is set up to interrupt the processor after a pre-determined number of events have been observed. The data cache event address register repeatedly captures the instruction and data addresses of actual data cache load misses. Whenever the counter overflows, miss event address collection is suspended until the event address register is read by software (this prevents software from capturing a miss event that might be caused by the monitoring software itself). When the counter overflows an interrupt is delivered to software, the observed event addresses are collected, and a new observation interval can be setup by rewriting the performance counter register. For time-based (rather than event-based) sampling methods, the event address registers indicate to software whether or not a qualified event was captured. Statistical sampling can achieve arbitrary event resolution by varying the number of events within an observation interval, and by increasing the number of observation intervals.

6.1.3 Event Qualification

On the Itanium processor, performance monitoring can be confined to a subset of all events. As shown in Figure 6-4, events can be qualified for monitoring based on an instruction address range, a particular instruction opcode, a data address range, an event specific “unit-mask”, the privilege level and instruction set the event was caused by, and the status of the performance monitoring freeze bit (PMC[0].fr).

- Itanium Instruction Address Range Check: The Itanium processor allows event monitoring to be constrained to a programmable instruction address range. This enables monitoring of dynamically linked libraries (DLL), functions, or loops of interest in the context of a large Itanium-based application. The Itanium instruction address range check is applied at the instruction fetch stage of the pipeline and the resulting qualification is carried by the instruction throughout the pipeline. This enables conditional event counting at a level of granularity smaller than dynamic instruction length of the pipeline (approximately 48 instructions). The Itanium processor’s instruction address range check operates only during Itanium-based code execution (i.e. when PSR.is is zero). For details, see Section 6.2.4, "Intel® Itanium™ Instruction Address Range Check Register (PMC[13])".
- Itanium Instruction Opcode Match: The Itanium processor provides two independent Itanium opcode match registers each of which match the currently issued instruction encodings with a programmable opcode match and mask function. The resulting match events can be selected as an event type for counting by the performance counters. This allows histogramming of instruction types, usage of destination and predicate registers as well as basic block profiling (through insertion of tagged nops). The opcode matcher operates only during Itanium-based code execution (i.e. when PSR.is is zero). Details are described in Section 6.2.5, "Intel® Itanium™ Opcode Match Registers (PMC[8,9])".
- Itanium Data Address Range Check: The Itanium processor allows event collection for memory operations to be constrained to a programmable data address range. This enables selective monitoring of data cache miss behavior of specific data structures. For details, see Section 6.2.6, "Intel® Itanium™ Data Address Range Check (PMC[11])".
- Event Specific Unit Masks: Some events allow the specification of “unit masks” to filter out interesting events directly at the monitored unit. For details, refer to the event pages in Chapter 7, "Performance Monitor Events".
- Privilege Level: Two bits in the processor status register are provided to enable selective process-based event monitoring. The Itanium processor supports conditional event counting based on the current privilege level; this allows performance monitoring software to break-down event counts into user and operating system contributions. For details on how to constrain monitoring by privilege level refer to Section 6.2.1, "Performance Monitor Control and Accessibility".
- Instruction Set: The Itanium processor supports conditional event counting based on the currently executing instruction set (Itanium architecture or IA-32) by providing two instruction set mask bits for each event monitor. This allows performance monitoring software to break-down event counts into Itanium-based and IA-32 contributions. For details, refer to Section 6.2.1, "Performance Monitor Control and Accessibility".
- Performance Monitor Freeze: Event counter overflows or software can freeze event monitoring. When frozen, no event monitoring takes place until software clears the monitoring freeze bit (PMC[0].fr). This ensures that the performance monitoring routines themselves, e.g. counter overflow interrupt handlers or performance monitoring context switch routines, do not “pollute” the event counts of the system under observation.

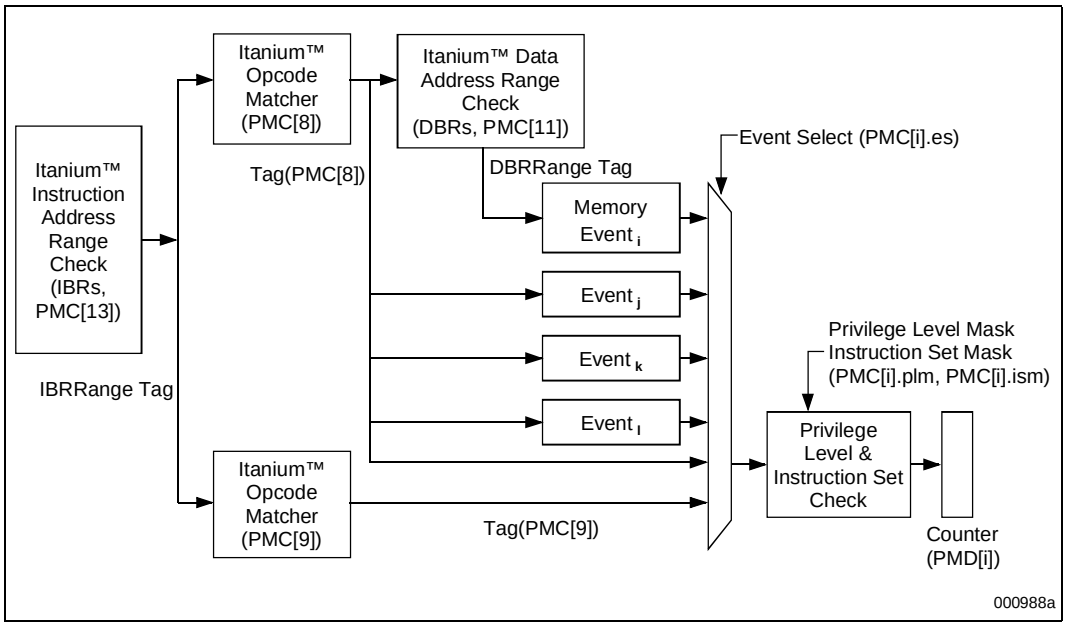
Figure 6-4. Intel® Itanium™ Processor Event Qualification



6.1.3.1 Combining Opcode Matching, Instruction, and Data Address Range Check

The Itanium processor allows various event qualification mechanisms to be combined by providing the instruction tagging mechanism shown in Figure 6-5. Instruction address range check and opcode matching are available only for Itanium-based code; they are disabled when IA-32 code is executing.

Figure 6-5. Instruction Tagging Mechanism in the Intel® Itanium™ Processor



During Itanium instruction execution (PSR.is is zero), the instruction address range check is applied first. The resulting address range check tag (IBRRangeTag) is passed to two opcode matchers that combine the instruction address range check with the opcode match. Each of the two combined tags (Tag(PMC[8]) and Tag(PMC[9])) can be counted as a retired instruction count event (for details refer to event description IA64_TAGGED_INST_RETIRED in Table 7-3 “Instruction Issue and Retirement Events” on page 48).

One of the combined Itanium address range and opcode match tags, Tag(PMC[8]), qualifies all down-stream pipeline events. Events in the memory hierarchy (L1 and L2 data cache and data TLB events) can further be qualified using a data address DBRRangeTag).

As summarized in Table 6-3, data address range checking can be combined with opcode matching and instruction range checking on the Itanium processor. Additional event qualifications based on the current privilege level and the current instruction set can be applied to all events and are discussed in Section 6.1.3.2, "Privilege Level Constraints" and Section 6.1.3.3, "Instruction Set Constraints".

Table 6-3. Intel® Itanium™ Processor Event Qualification Modes

Event Qualification Modes	Instr. Address Range Check PMC[13].ta	Opcode Matching PMC[8]	Data Address Range Check PMC[11].pt
Unconstrained Monitoring (all events)	1	0xffff_ffff_ffff_ffff	1
Instruction Address Range Check only	0	0xffff_ffff_ffff_ffff	1
Opcode Matching only	1	Desired Opcodes	1
Data Address Range Check only	1	0xffff_ffff_ffff_ffff	0
Instruction Address Range Check and Opcode Matching	0	Desired Opcodes	1

Table 6-3. Intel® Itanium™ Processor Event Qualification Modes (Continued)

Event Qualification Modes	Instr. Address Range Check PMC[13].ta	Opcode Matching PMC[8]	Data Address Range Check PMC[11].pt
Instruction and Data Address Range Check	0	0xffff_ffff_ffff_ffff	0
Opcode Matching and Data Address Range Check	1	Desired Opcodes	0

6.1.3.2 Privilege Level Constraints

Performance monitoring software cannot always count on context switch support from the operating system. In general, this has made performance analysis of a single process in a multi-processing system or a multi-process workload very difficult. To provide hardware support for this kind of analysis, the Itanium architecture specifies three global bits (PSR.up, PSR.pp, DCR.pp) and a per-monitor “privilege monitor” bit (PMC[i].pm). To break down the performance contributions of operating system and user-level application components, each monitor specifies a 4-bit privilege level mask (PMC[i].plm). The mask is compared to the current privilege level in the processor status register (PSR.cpl), and event counting is enabled if PMC[i].plm[PSR.cpl] is one. The Itanium processor performance monitors control is discussed in Section 6.2.1, "Performance Monitor Control and Accessibility".

PMC registers can be configured as user-level monitors (PMC[i].pm is zero) or system-level monitors (PMC[i].pm is one). A user-level monitor is enabled whenever PSR.up is one. PSR.up can be controlled by an application using the `sum`/`rum` instructions. This allows applications to enable/disable performance monitoring for specific code sections. A system-level monitor is enabled whenever PSR.pp is one. PSR.pp can be controlled at privilege level 0 only, which allows monitor control without interference from user-level processes. The pp field in the default control register (DCR.pp) is copied into PSR.pp whenever an interruption is delivered. This allows events generated during interruptions to be broken down separately: if DCR.pp is zero, events during interruptions are not counted, if DCR.pp is one, they are included in the kernel counts.

As shown in Figure 6-6, Figure 6-7 and Figure 6-8, single process, multi-process, and system level performance monitoring are possible by specifying the appropriate combination of PSR and DCR bits. These bits allow performance monitoring to be controlled entirely from a kernel level device driver, without explicit operating system support. Once the desired monitoring configuration has been setup in a process’ processor status register (PSR), “regular” unmodified operating context switch code automatically enables/disables performance monitoring.

With support from the operating system, individual per-process break-down of event counts can be generated as outlined in Section 7.2, "Performance Monitoring" of Volume 2 of the *Intel® Itanium™ Architecture Software Developer’s Manual*.

6.1.3.3 Instruction Set Constraints

On the Itanium processor, monitoring can additionally be constrained based on the currently executing instruction set as defined by PSR.is. This capability is supported by the four generic performance counters as well as the instruction and data event address registers. However, the Itanium instruction address range checking, Itanium opcode matching and the Itanium branch trace buffer, only support Itanium-based code execution. When these Itanium architecture only features

are used, the corresponding PMC register instruction set mask (PMC[i].ism) should be set to Itanium architecture only (01) to ensure that events generated by IA-32 code do not corrupt the Itanium-based event counts.

Figure 6-6. Single Process Monitor

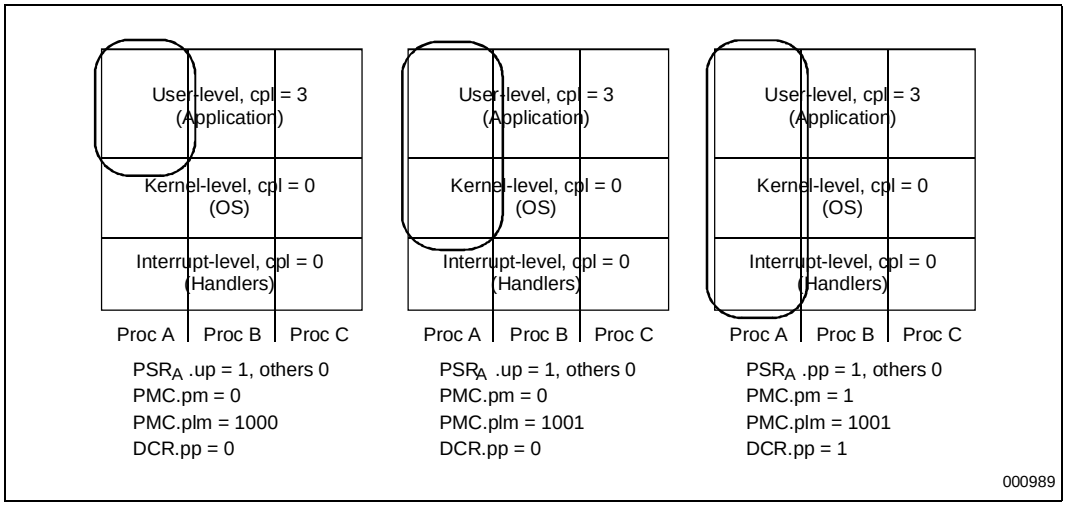


Figure 6-7. Multiple Process Monitor

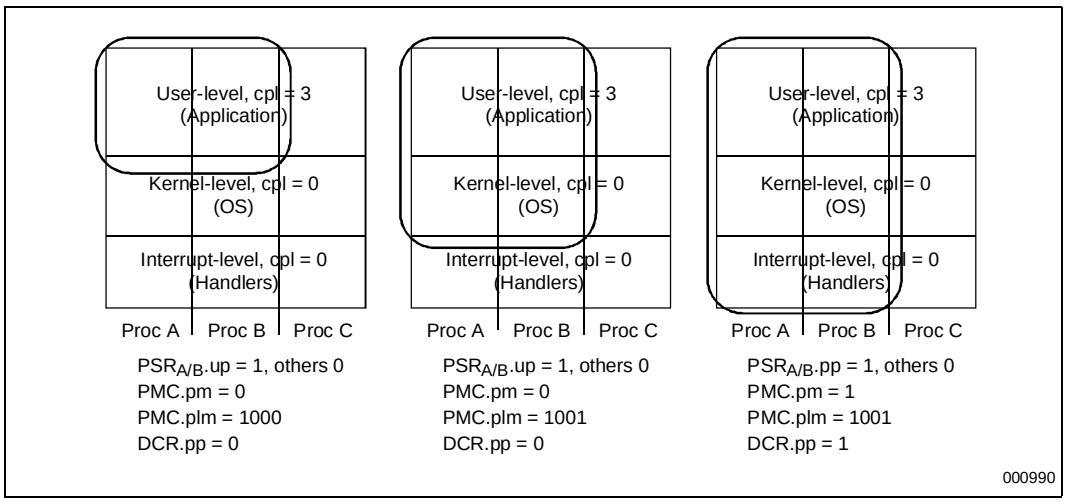
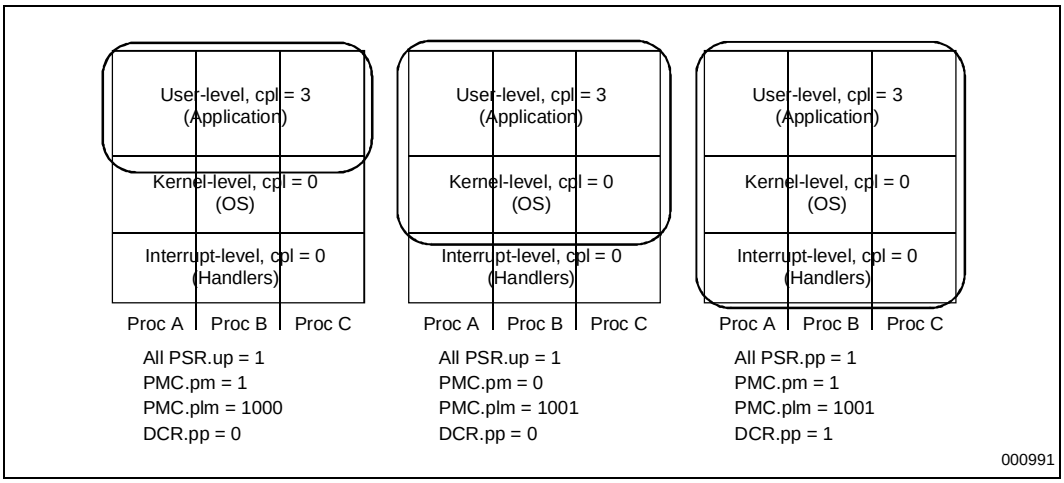


Figure 6-8. System Wide Monitor



6.2 Performance Monitor State

Two sets of performance monitor registers are defined. Performance Monitor Configuration (PMC) registers are used to configure the monitors. Performance Monitor Data (PMD) registers provide data values from the monitors. This section describes the Itanium processor performance monitoring registers which expands on the Itanium architectural definition. As shown in Figure 6-9, the Itanium processor provides four 32-bit performance counters (PMC/PMD[4,5,6,7] pairs), and the following model-specific monitoring registers: instruction and data event address registers (EARs) for monitoring cache and TLB misses, a branch trace buffer, two opcode match registers and an instruction address range check register.

Table 6-4 defines the PMC/PMD register assignments for each monitoring feature. The interrupt status registers are mapped to PMC[0,1,2,3]. The four generic performance counter pairs are assigned to PMC/PMD[4,5,6,7]. The event address registers and the branch trace buffer are controlled by three configuration registers (PMC[10,11,12]). Captured event addresses and cache miss latencies are accessible to software through five event address data registers (PMD[0,1,2,3,17]) and a branch trace buffer (PMD[8-16]). On the Itanium processor, monitoring of some events can additionally be constrained to a programmable instruction address range by appropriate setting of the instruction breakpoint registers (IBR) and the instruction address range check register (PMC[13]). Two opcode match registers (PMC[8,9]) allow monitoring of some events to be qualified with a programmable opcode. For memory operations, events can be qualified by a programmable data address range by appropriate setting of the data breakpoint registers (DBR) and the data address range check bits in PMC[11].

6.2.1 Performance Monitor Control and Accessibility

Event collection is controlled by the Performance Monitor Configuration (PMC) registers and the processor status register (PSR). Four PSR fields (PSR.up, PSR.pp, PSR.cpl and PSR.sp) and the performance monitor freeze bit (PMC[0].fr) affect the behavior of all performance monitor registers.

Finer, per monitor, control is provided by three PMC register fields (PMC[i].plm, PMC[i].ism, and PMC[i].pm). Instruction set masking based on PMC[i].ism is an Itanium processor model-specific feature. Event collection for a monitor is enabled under the following constraints on the Itanium processor:

```
Monitor Enable_i =(not PMC[0].fr) and PMC[i].plm[PSR.cpl] and ((not
PMC[i].ism[PSR.is]) or (PMC[i]=12)) and (not (PMC[i].pm) and PSR.up) or
(PMC[i].pm and PSR.pp))
```

Figure 3-2, “Processor Status Register (PSR)” on page 2:18 in Volume 2 of the *Intel® Itanium™ Architecture Software Developer’s Manual* defines the PSR control fields that affect performance monitoring. For a detailed definition of how the PSR bits affect event monitoring and control accessibility of PMD registers, please refer to Section 3.3.2, "Processor Status Register (PSR)" and Section 7.2.1, "Generic Performance Counter Registers" in Volume 2 of the *Intel® Itanium™ Architecture Software Developer’s Manual*.

Figure 6-9. Intel® Itanium™ Processor Performance Monitor Register Model

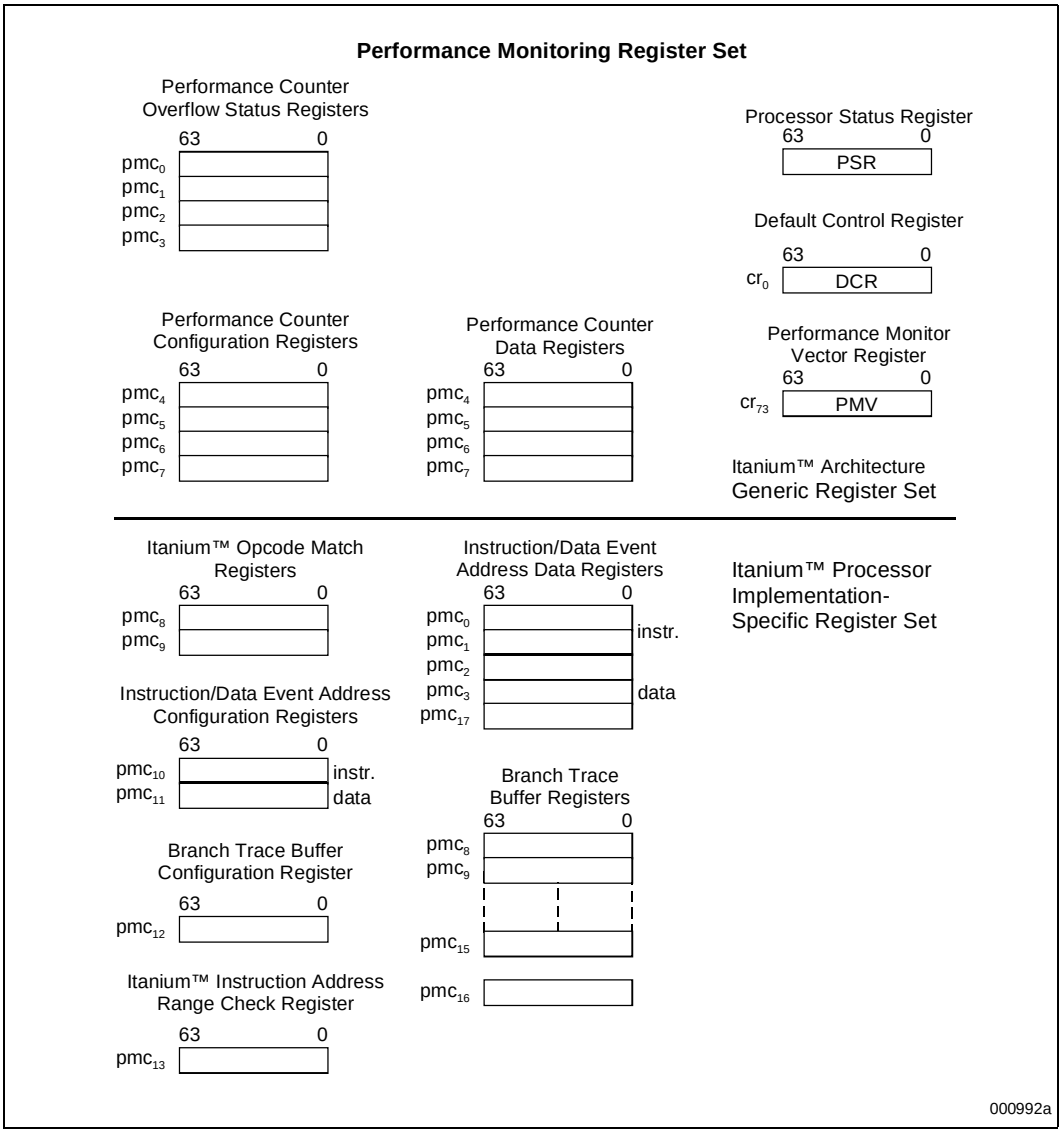


Table 6-4. Intel® Itanium™ Processor Performance Monitor Register Set

Monitoring Feature	Configu-ration Registers (PMC)	Data Registers (PMD)	Description
Interrupt Status	PMC[0,1,2,3]	none	See Section 6.2.3, "Performance Monitor Overflow Status Registers (PMC[0,1,2,3])"
Event Counters	PMC[4,5,6,7]	PMD[4,5,6,7]	See Section 6.2.2, "Performance Counter Registers"
Opcode Matching	PMC[8,9]	none	See Section 6.2.5, "Intel® Itanium™ Opcode Match Registers (PMC[8,9])"
Instruction EAR	PMC[10]	PMD[0,1]	See Section 6.2.7.1, "Instruction EAR (PMC[10], PMD[0,1])"
Data EAR	PMC[11]	PMD[2,3,17]	See Section 6.2.7.4, "Data EAR (PMC[11], PMD[2,3,17])"
Instruction Address Range Check	PMC[13]	none	See Section 6.2.4, "Intel® Itanium™ Instruction Address Range Check Register (PMC[13])"
Data Address Range Check	PMC[11]	none	See Section 6.2.6, "Intel® Itanium™ Data Address Range Check (PMC[11])"

As defined in Table 6-4, each of these PMC registers controls the behavior of its associated performance monitor data registers (PMD). Table 6-11 defines per monitor controls that apply to PMC[4,5,6,7,10,11,12]. The Itanium processor model-specific PMD registers associated with instruction/data EARs and the branch trace buffer (PMD[0,1,2,3,8-17]) can be read reliably only when event monitoring is frozen (PMC[0].fr is one).

Figure 6-10. Processor Status Register (PSR) Fields for Performance Monitoring

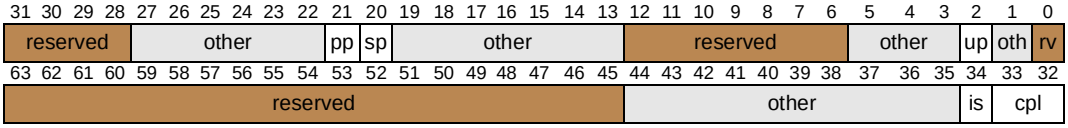


Figure 6-11. Performance Monitor PMC Register Control Fields (PMC[4,5,6,7,10,11,12])

Field	Bits	Description
plm	3:0	Privilege Level Mask - controls performance monitor operation for a specific privilege level. Each bit corresponds to one of the 4 privilege levels, with bit 0 corresponding to privilege level 0, bit 1 with privilege level 1, etc. A bit value of 1 indicates that the monitor is enabled at that privilege level. Writing zeros to all plm bits effectively disables the monitor. In this state, the Intel® Itanium™ processor will not preserve the value of the corresponding PMD register(s).
pm	6	Privileged monitor - When 0, the performance monitor is configured as a user monitor, and enabled by PSR.up. When PMC.pm is 1, the performance monitor is configured as a privileged monitor, enabled by PSR.pp, and PMD can only be read by privileged software.
ism	25:24	Instruction Set Mask - controls performance monitor operation based on the current instruction set. The instruction set mask applies to PMC[4,5,6,7,10,11] but not to PMC[12]. 00: monitoring enabled during Intel® Itanium™ instruction execution and IA-32 instruction execution (regardless of PSR.is) 10: bit 24 low enables monitoring during Intel® Itanium™ instruction execution (when PSR.is is zero) 01: bit 25 low enables monitoring during IA-32 instruction execution (when PSR.is is one) 11: disables monitoring

6.2.2 Performance Counter Registers

The Itanium processor provides four generic performance counters (PMC/PMD[4,5,6,7] pairs). The implemented counter width on the Itanium processor is 32 bits. The Itanium processor counters are not symmetrical (i.e. not all event types can be monitored by all counters). Counters PMC/PMD[4,5] can track events whose maximum per-cycle event increment is 7. Counters PMC/PMD[6,7] can track events whose maximum per-cycle event increment is 3.

The Itanium processor extends the generic Itanium counter configuration register (PMC) layout by adding two fields for specifying a unit mask (umask) and a threshold field. These model-specific fields are described in Table 6-5. A counter overflow occurs when the counter wraps (i.e. a carry out from bit 31 is detected). Software can force an external interruption or external notification after N events, by preloading the monitor with a count value of 2^{32} - N. When accessible, software can continuously read the performance counter registers PMD[4,5,6,7] without disabling event collection. The processor guarantees that software will see monotonically increasing counter values.

Figure 6-12 and Table 6-5 define the layout of the Itanium processor Performance Counter Data Registers (PMD[4,5,6,7]). Figure 6-13, Figure 6-14 and Table 6-5 define the layout of the Itanium processor Performance Counter Configuration Registers (PMC[4,5,6,7]).

Figure 6-12. Intel® Itanium™ Processor Generic PMD Registers (PMD[4,5,6,7])

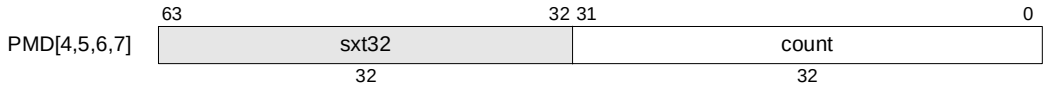


Table 6-5. Intel® Itanium™ Processor Generic PMD Register Fields

Field	Bits	Description
sxt32	63:32	Writes are ignored, Reads return the value of bit 31, so count values appear as sign extended.
count	31:0	Event Count. The counter is defined to overflow when the count field wraps (carry out from bit 31).

Figure 6-13. Intel® Itanium™ Processor Generic PMC Registers (PMC[4,5])

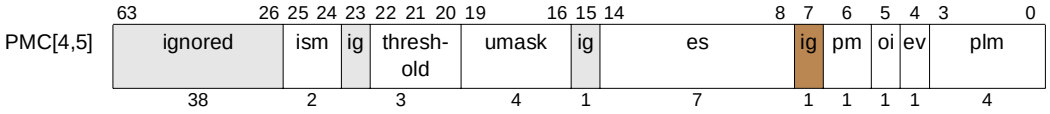


Figure 6-14. Intel® Itanium™ Processor Generic PMC Registers (PMC[6,7])

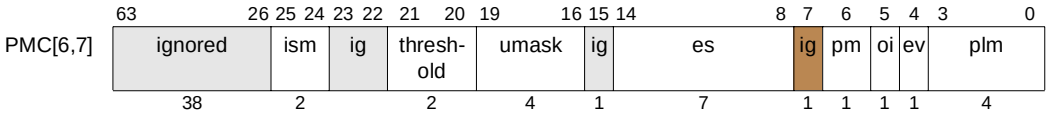


Table 6-6. Intel® Itanium™ Processor Generic PMC Register Fields (PMC[4,5,6,7])

Field	Bits	Description
plm	3:0	Privilege Level Mask. See Table 6-11, “Performance Monitor PMC Register Control Fields (PMC[4,5,6,7,10,11,12])”.
ev	4	External visibility - When 1, an external notification (BPM pin strobe) is provided whenever the counter wraps, i.e a carry out from bit 31 is detected. External notification occurs regardless of the setting of the oi bit. On the Intel® Itanium™ processor, PMC[4] external notification strobes the BPM0 pin, PMC[5] external notification strobes the BPM1 pin, PMC[6] external notification strobes the BPM2 pin, and PMC[7] external notification strobes the BPM3 pin.
oi	5	Overflow interrupt - When 1, a Performance Monitor Interrupt is raised and the performance monitor freeze bit (PMC[0].fr) is set when the monitor overflows. When 0, no interrupt is raised and the performance monitor freeze bit (PMC[0].fr) remains unchanged. Overflow occurs when the counter wraps, i.e. a carry out from bit 31 is detected. Counter overflows generate only one interrupt.
pm	6	Privilege Monitor. See Table 6-11, “Performance Monitor PMC Register Control Fields (PMC[4,5,6,7,10,11,12])”.
ig	7	ignored
es	14:8	Event select - selects the performance event to be monitored. Intel® Itanium™ processor event encodings are defined in Chapter 7, "Performance Monitor Events".
ig	15	ignored
umask	19:16	Unit Mask - event specific mask bits (see event definition for details)
threshold	22:20 21:20	Threshold -enables thresholding for “multi-occurrence” events. PMC[4,5] define 3 threshold bits 22:20, while PMC[6,7] define 2 threshold bits 21:20. When threshold is zero, the counter sums up all observed event values. When the threshold is non-zero, the counter increments by one in every cycle in which the observed event value exceeds the threshold.
ism	25:24	Instruction Set Mask. See Table 6-11, “Performance Monitor PMC Register Control Fields (PMC[4,5,6,7,10,11,12])”.
ignored	63:24	Read zero, Writes ignored.

6.2.3 Performance Monitor Overflow Status Registers (PMC[0,1,2,3])

The Itanium processor supports four counters. As shown in Figure 6-15 and Table 6-7 only PMC[0]{7:4} bits are populated. All other overflow bits are ignored, i.e. they read as zero and ignore writes.

Figure 6-15. Intel® Itanium™ Processor Performance Monitor Overflow Status Registers (PMC[0,1,2,3])

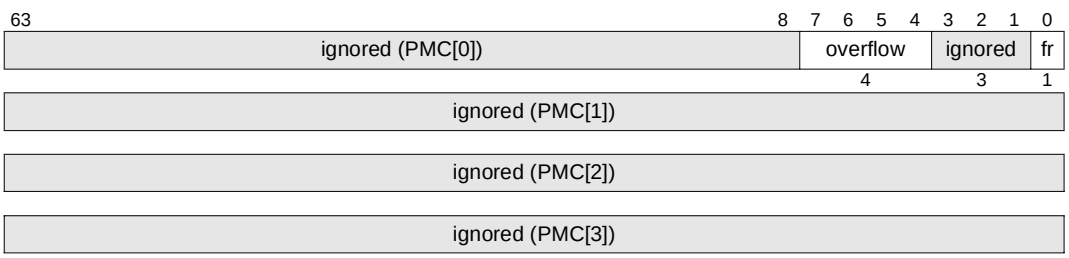


Table 6-7. Intel® Itanium™ Processor Performance Monitor Overflow Register Fields (PMC[0,1,2,3])

Register	Field	Bits	Description
PMC[0]	fr	0	Performance Monitor “freeze” bit - when 1, event monitoring is disabled. When 0, event monitoring is enabled. This bit is set by hardware whenever a performance monitor overflow occurs and its corresponding overflow interrupt bit (PMC.oi) is set to one. SW is responsible for clearing it. When the PMC.oi bit is not set, then counter overflows do not set this bit.
PMC[0]	ignored	3:1	Read zero, Writes ignored.
PMC[0]	overflow	7:4	Event Counter Overflow - When bit n is one, indicate that the PMD_n overflowed. This is a bit vector indicating which performance monitor overflowed. These overflow bits are set on their corresponding counters overflow regardless of the state of the PMC.oi bit. These bits are sticky and multiple bits may be set.
PMC[0]	ignored	63:8	Read zero, Writes ignored.
PMC [1,2,3]	ignored	63:0	Read zero, Writes ignored.

6.2.4 Intel® Itanium™ Instruction Address Range Check Register (PMC[13])

The Itanium processor allows event monitoring to be constrained to a range of instruction addresses. All four architectural breakpoint registers (IBRs) are used to specify the desired address range. The Itanium processor instruction address range check register PMC[13] specifies how the resulting address match is applied to the performance monitors.

Figure 6-16. Intel® Itanium™ Processor Instruction Address Range Check Register (PMC[13])

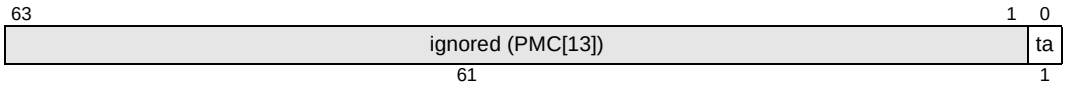


Table 6-8. Intel® Itanium™ Processor Instruction Address Range Check Register Fields (PMC[13])

Field	Bits	Description
ta	0	Tag All - when 1, all events are counted independent of instruction address and instruction set. The default value of this PMC[13].ta should be set to one upon reset.

Instruction address range checking is controlled by the “tag all” bit (PMC[13].ta). When PMC[13].ta is one, all instructions are tagged regardless of IBR settings. In this mode, events from both IA-32 and Itanium-based code execution contribute to the event count. When PMC[13].ta is zero, the instruction address range check based on the IBR settings is applied to all Itanium-based code fetches. In this mode, IA-32 instructions are never tagged, and, as a result, events generated by IA-32 code execution are ignored. Table 6-9 defines the behavior of the instruction address range checker for different combinations of PSR.is and PMC[13].ta.

Table 6-9. Intel® Itanium™ Processor Instruction Address Range Check by Instruction Set

	PSR.is	
PMC_{13}.ta	0 (Intel® Itanium™ Architecture)	1 (IA-32)
0	Tag only Intel® Itanium™ instructions if they match IBR range	DO NOT tag any IA-32 operations.
1	Tag all Intel® Itanium™ instructions and IA-32 instructions.Ignore IBR range.	

The processor compares every Itanium-based instruction fetch address IP{63:0} with each of the four architectural instruction breakpoint registers. Regardless of the value of the instruction break-point fault enable (IBR x-bit), the following expression is evaluated for each of the Itanium processor's four IBRs:

$IBRmatch_i$ = match(IP,$IBR_{[2*i]}$.addr,$IBR_{[2*i]+1}$.mask,$IBR_{[2*i]+1}$.plm

On the Itanium processor, in which only 54 virtual and 44 physical address bits are implemented, this IBR match is defined as follows:

$IBRmatch_i$ = ($IBR_{[2*i]+1}$.plm[PSR.cpl])

and ($AND_{b=50..0}$(($IBR_{[2*i]}$.addr{b} and $IBR_{[2*i]+1}$.mask{b}) = (IP{b} and $IBR_{[2*i]+1}$.mask{b})))

and ($AND_{b=55..51}$(($IBR_{[2*i]}$.addr{b} and $IBR_{[2*i]+1}$.mask{b}) = (IP{50} and $IBR_{[2*i]+1}$.mask{b})))

and ($AND_{b=60..56}$($IBR_{[2*i]}$.addr{b} = IP{50}))

and ($AND_{b=63..61}$($IBR_{[2*i]}$.addr{b} = IP{b}))

The resulting four matches are combined with the PSR.is bit, two instruction address range check register bits, the IBR x-bits, and PSR.db:

IBRRangeTag = (PMC[13].ta)
or ((not PSR.is)
and (($IBRmatch_0$ or $IBRmatch_1$ or $IBRmatch_2$ or $IBRmatch_3$)
and (not (PSR.db or IBR_1.x or IBR_3.x or IBR_5.x or IBR_7.x))))

The instruction range check tag (IBRRangeTag) considers the IBR address ranges only if PMC[13].ta is zero, PSR.is is zero, and if none of the IBR x-bits or PSR.db are set. Since the architectural break-point registers (IBRs) are used to specify the desired performance monitor address range, it is not possible to constrain monitoring when the IBRs are used in their architectural break-point capacity, i.e. when PSR.db or an IBR x-bit is set. In other words, it is not possible to use performance monitor address range checking when a debugger is running, unless the debugger and the performance monitor software carefully synchronize their use of the IBRs.

The instruction range check tag is computed early in the processor pipeline and therefore includes speculative, wrong-path as well as predicated off instructions. Furthermore, range check tags are not accurate in the instruction fetch and out-of-order parts of the pipeline (cache and bus units). Therefore, software must accept a level of range check inaccuracy for events generated by these units, especially for non-looping code sequences that are shorter than the Itanium processor pipeline. As described in Section 6.1.3.1, "Combining Opcode Matching, Instruction, and Data Address Range Check", the instruction range check result may be combined with the results of the Itanium opcode match registers described in the next section.

6.2.5 Intel® Itanium™ Opcode Match Registers (PMC[8,9])

The Itanium processor allows event monitoring to be constrained based on the Itanium-based encoding (opcode) of an instruction. Registers PMC[8,9] allow two independent opcodes matches to be specified. The Itanium opcode matcher operates only during Itanium-based code execution (i.e. when PSR.is is zero).

Figure 6-17. Opcode Match Registers (PMC[8,9])

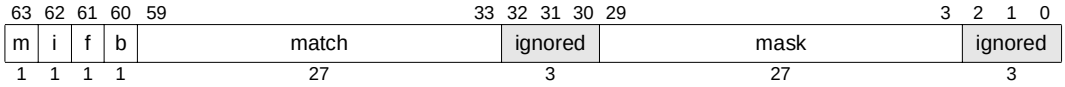


Table 6-10. Opcode Match Register Fields (PMC[8,9])

Field	Bits	Width	Description
mask	29:3	27	Bits that mask Intel® Itanium™ instruction encoding bits {40:27} and {12:0}
match	59:33	27	Opcode bits to match Intel® Itanium™ instruction encoding bits {40:27} and {12:0}
b	60	1	If 1: match if opcode is an B-syllable
f	61	1	If 1: match if opcode is an F-syllable
i	62	1	If 1: match if opcode is an I-syllable
m	63	1	If 1: match if opcode is an M-syllable

For opcode matching purposes, an Itanium instruction is defined by two items: the instruction type “itype” (one of M, I, F or B) and the 40-bit encoding “enco{40:0}” defined in Volume 3 of the *Intel® Itanium™ Architecture Software Developer’s Manual*. Each instruction is evaluated against each opcode match register (PMC[8,9]) as follows:

Match(PMC[i]) = (imatch (itype,PMC[i].mifb) and
ematch(enco,PMC[i].match,PMC[i]PMC[i].mask))

Where:

imatch(itype,PMC[i].mifb) = itype=M and PMC[i].m) or (itype=I and PMC[i].i) or (itype=F and PMC[i].f) or (itype=B and PMC[i].b)

ematch(enco,match,mask) = AND $_{b=40..27}$ ((enco{b}=match{b-14}) or mask{b-14}) and AND $_{b=12..0}$ ((enco{b}=match{b}) or mask{b})

This function matches encoding bits{40:27} (major opcode) and encoding bits{12:0} (destination and qualifying predicate) only. Bits{26:13} of the instruction encoding are ignored by the opcode matcher.

This produces two opcode match events that are combined with the PSR.is bit, and the instruction range check tag (IBRRangeTag, see Section 6.2.4, "Intel® Itanium™ Instruction Address Range Check Register (PMC[13])") as follows:

Tag(PMC[8]) = Match(PMC[8]) and IBRRangeTag and (not PSR.is)

Tag(PMC[9]) = Match(PMC[9]) and IBRRangeTag and (not PSR.is)

As shown in Figure 6-5, the two tags, Tag(PMC[8]) and Tag(PMC[9]), are staged down the processor pipeline until instruction retirement, and can be selected as a retired instruction count event. In this way, a performance counters (PMC/PMD[4,5,6,7]) can be used to count the number of retired instructions within the programmed range that match the specified opcodes. All combinations of the mifb bits are supported. To match A-syllable instructions both m and i bits should be set to one. To match all instruction types, all mifb and all mask bits should be set to one. This will count the number of retired instructions within the programmed address range. One of the combined Itanium address range and opcode match tags, Tag(PMC[8]), qualifies most down-stream pipeline events. To ensure that all events are counted independent of the Itanium opcode matcher, all mifb and all mask bits of PMC[8] should be set to one (all opcodes match). Tag(PMC[9]) is not used to qualify downstream events.

6.2.6 Intel® Itanium™ Data Address Range Check (PMC[11])

For instructions that reference memory, the Itanium processor allows event counting to be constrained by data address ranges using the architectural data breakpoint registers (DBRs). Data address range checking capability is controlled enabled by the “pass tags” bit in the Data Event Address Register (PMC[11].pt). For details on PMC[11], refer to Section 6.2.7.4, "Data EAR (PMC[11], PMD[2,3,17])".

When enabled (PMC[11].pt is zero), data address range checking is applied to loads (all types), stores, semaphore operations, and the `lfetch` instruction whose upstream opcode match Tag(PMC[8]) was set. When PMC[11].pt is one, RSE operations and VHPT walks are tagged only if the opcode match Tag(PMC[8]) was set for the operation that caused the RSE or VHPT activity. When PMC[11].pt is zero, all RSE operations and VHPT walks that hit the programmed data address range are tagged (regardless of the opcode match Tag(PMC[8])). To capture all VHPT walks when PMC[11].pt is zero, the minimum DBR mask granularity must be set to the size of a single VHPT entry.

On the Itanium processor, in which only 54 virtual address bits are implemented, the performance monitoring DBR match function is defined as follows:

$DBRRangeMatch_i$=

($AND_{b=50..0}$((DBR$_{[2*i]}$.addr{b} and DBR$_{[2*i]+1}$.mask{b}) = (addr{b} and DBR$_{[2*i]+1}$.mask{b})))

and ($AND_{b=55..51}$((DBR$_{[2*i]}$.addr{b} and DBR$_{[2*i]+1}$.mask{b}) = (addr{50} and

DBR$_{[2*i]+1}$.mask{b})))

and ($AND_{b=60..56}$(DBR$_{[2*i]}$.addr{b} = addr{50}))

and ($AND_{b=63..61}$(DBR$_{[2*i]}$.addr{b} = addr{b}))

The resulting four matches are combined with PSR.db to form a single DBR match:

DBRRangeMatch = (($DBRRangeMatch_0$ or $DBRRangeMatch_1$ or $DBRRangeMatch_2$ or $DBRRangeMatch_3$)
and (not PSR.db))

Note: DBR matching for performance monitoring ignores the setting of the DBR r, w and plm fields. Finally, the DBRRangeMatch is combined with PMC[11].pt and the upstream opcode match tag Tag(PMC[8]) as follows:

DBRRangeTag = Tag(PMC[8]) and ((PMC[11].pt) or DBRRangeMatch)

DBR based data address range checking combined with opcode matching and instruction range checking allows the following combinations of event monitoring on the Itanium processor.

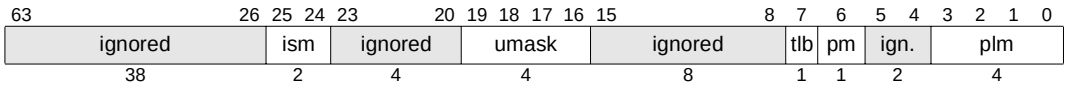
6.2.7 Event Address Registers (PMC[10,11]/PMD[0,1,2,3,17])

This section defines the register layout for the Itanium processor instruction and data event address registers (EARs). Sampling of four events is supported on the Itanium processor: instruction cache and instruction TLB misses, data cache load misses, and data TLB misses. The EARs are configured through two PMC registers (PMC[10,11]). EAR specific unit masks allow software to specify event collection parameters to hardware. Instruction and data addresses, operation latencies and other captured event parameters are provided in five PMD registers (PMD[0,1,2,3,17]). The instruction and data cache EARs report the latency of captured cache events and allow latency thresholding to qualify event capture. Event address data registers (PMD[0,1,2,3,17]) contain valid data only when event collection is frozen (PMC[0].fr is one). Reads of PMD[0,1,2,3,17] while event collection is enabled return undefined values.

6.2.7.1 Instruction EAR (PMC[10], PMD[0,1])

The instruction event address configuration register (PMC[10]) can be programmed to monitor either L1 instruction cache or instruction TLB miss events. Figure 6-18 and Table 6-11 detail the register layout of PMC[10]. Figure 6-19 describes the associated event address data registers PMD[0,1].

Figure 6-18. Instruction Event Address Configuration Register (PMC[10])

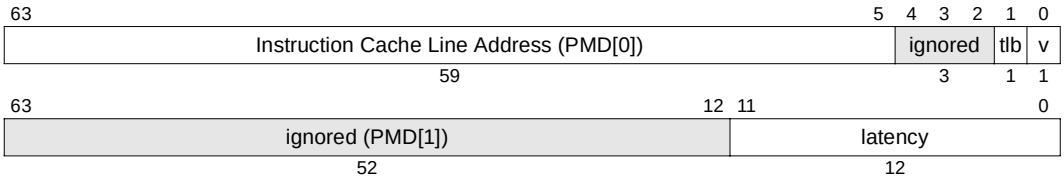


When the tlb-bit (PMC[10].tlb) is set to zero instruction cache misses are monitored, when it is set to one instruction TLB misses are monitored. The interpretation of the umask field and performance monitor data registers PMD[0,1] depend on the setting of the tlb bit, and are described in Section 6.2.7.2, "Instruction EAR Cache Mode (PMC[10].tlb=0)" for instruction cache monitoring and in Section 6.2.7.3, "Instruction EAR TLB Mode (PMC[10].tlb=1)" for instruction TLB monitoring.

Table 6-11. Instruction Event Address Configuration Register Fields (PMC[10])

Field	Bits	Description	
plm	3:0	See Table 6-11.	
pm	6	See Table 6-11.	
tlb	7	Instruction EAR selector: instruction cache/TLB	
		if tlb=0:	monitor L1 instruction cache misses PMD[0,1] register interpretation see Table 6-13.
		if tlb=1:	monitor instruction TLB misses PMD[0,1] register interpretation see Table 6-15.
umask	19:16	Instruction EAR unit mask	
		if tlb=0:	instruction cache unit mask (definition see Table 6-12)
		if tlb=1:	instruction TLB unit mask (definition see Table 6-14)
ism	25:24	See Table 6-11.	

Figure 6-19. Instruction Event Address Register Format (PMD[0,1]



6.2.7.2 Instruction EAR Cache Mode (PMC[10].tlb=0)

When PMC[10].tlb is zero, the instruction event address register captures instruction addresses and access latencies for L1 instruction cache misses. Only misses whose latency exceeds a programmable threshold are captured. The threshold is specified as a four bit umask field in the configuration register PMC[10]. Possible threshold values are defined in Table 6-12.

As defined in Table 6-13, the address of the instruction cache line missed the L1 instruction cache is provided in PMD[0]. If no qualified event was captured, the valid bit in PMD[0] is zero. The latency of the captured instruction cache miss in processor clock cycles is provided in the latency field of PMD[1]. In cache mode, the TLB miss bit of PMD[0] is undefined.

Table 6-12. Instruction EAR (PMC[10]) umask Field in Cache Mode (PMC[10].tlb=0)

umask Bits 3:0	Latency Threshold [CPU cycles]	umask Bits 3:0	Latency Threshold [CPU cycles]
0000	>= 4	0110	>= 256
0001	>= 8	0111	>= 512
0010	>= 16	1000	>= 1024
0011	>= 32	1001	>= 2048
0100	>= 64	1010	>= 4096
0101	>= 128	1011.. 1111	No events are captured.

Table 6-13. Instruction EAR (PMD[0,1]) in Cache Mode (PMC[10].tlb=0)

Register	Field	Bits	Description
PMD[0]	v	0	Valid Bit 0: invalid address (EAR did not capture qualified event) 1: EAR contains valid event data
	tlb	1	TLB Miss Bit (undefined in cache mode)
	Instruction Cache Line Address	63:5	Address of instruction cache line that caused cache miss[a]
PMD[1]	latency	11:0	Latency in processor clocks

a. The Itanium processor does not implement virtual address bits va{60:51} and physical address bits pa{62:44}. The instruction and data address bits {60:51} of PMD[0] read as a sign-extension of bit {50}. Writes to bits {60:51} of PMD[0] are ignored by the processor.

6.2.7.3 Instruction EAR TLB Mode (PMC[10].tlb=1)

When PMC[10].tlb is one, the instruction event address register captures addresses of instruction TLB misses. The unit mask allows event address collection to capture specific subsets of instruction TLB misses. Table 6-14 summarizes the instruction TLB umask settings. All combinations of the mask bits are supported.

As defined in Table 6-15, the address of the instruction cache line fetch that missed the L1 TLB is provided in PMD[0]. The tlb bit indicates whether the captured TLB miss hit in the VHPT or required servicing by software. If no qualified event was captured, the valid bit in PMD[0] reads zero. In TLB mode, the latency field of PMD[1] is undefined.

Table 6-14. Instruction EAR (PMC[10]) umask Field in TLB Mode (PMC[10].tlb=1)

umask Bit	Instruction TLB EAR Unit Mask (Instruction TLB misses)
0	ignored
1	ignored
2	if one, capture Instruction TLB misses that hit VHPT
3	if one, capture Instruction TLB misses handled by software

Table 6-15. Instruction EAR (PMD[0,1]) in TLB Mode (PMC[10].tlb=1)

Register	Field	Bits	Description
PMD[0]	v	0	Valid Bit 0: invalid address (EAR did not capture qualified event 1: EAR contains valid event data
	tlb	1	TLB Miss Bit: 0: VHPT Hit 1: Instruction TLB Miss handled by software
	Instruction Cache Line Address	63:5	Address of instruction cache line that caused TLB miss[a]
PMD[1]	latency	11:2	undefined in TLB mode

a. The Itanium processor does not implement virtual address bits va{60:51}. The instruction address bits {60:51} of PMD[0] read as a sign-extension of bit {50}. Writes to bits {60:51} of PMD[0] are ignored by the processor.

6.2.7.4 Data EAR (PMC[11], PMD[2,3,17])

The data event address configuration register (PMC[11]) can be programmed to monitor either L1 data cache load misses or L1 data TLB misses. Figure 6-20 and Table 6-16 detail the register layout of PMC[11]. Figure 6-21 describes the associated event address data registers PMD[2,3,17]. The tlb bit in configuration register PMC[11] selects data cache or data TLB monitoring. The interpretation of the umask field and registers PMD[2,3,17] depends on the setting of the tlb bit, and is described in Section 6.2.7.5, "Data Cache Load Miss Monitoring (PMC[11].tlb=0)" for data cache load miss monitoring and in Section 6.2.7.6, "Data TLB Miss Monitoring (PMC[11].tlb=1)" for data TLB monitoring. The PMC[11].pt bit controls data address range checking which is described in Section 6.2.6, "Intel® Itanium™ Data Address Range Check (PMC[11])".

Figure 6-20. Data Event Address Configuration Register (PMC[11])

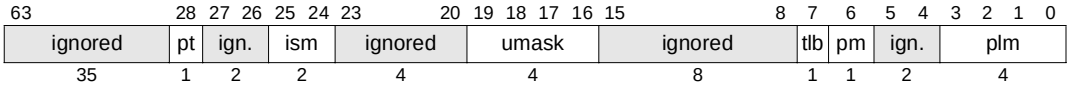
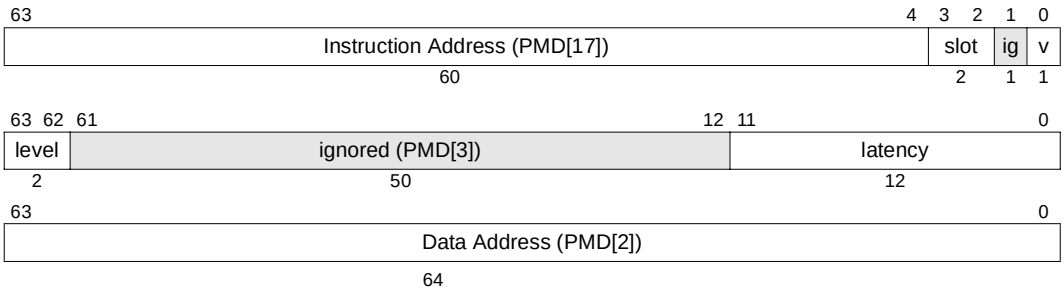


Table 6-16. Data Event Address Configuration Register Fields (PMC[11])

Field	Bits	Description
plm	3:0	See Table 6-11.
pm	6	See Table 6-11.
tlb	7	Data EAR selector: data cache/TLB
		if tlb=0:monitor L1 data cache load misses PMD[2,3,17] register interpretation see Table 6-18.
		if tlb=1: monitor L1 data TLB misses PMD[2,3,17] register interpretation see Table 6-20.
umask	19:16	Data EAR unit mask if tlb=0: data cache unit mask (definition see Table 6-17) if tlb=1: data TLB unit mask (definition see Table 6-19)
ism	25:24	See Table 6-11.
pt	28	Pass Tags. This bit enables/disables data address range checking. See Section 6.2.6, "Intel® Itanium™ Data Address Range Check (PMC[11])" for details. if pt=1: then the Tag(PMC[8]) is passed down the pipeline unmodified. if pt=0: data address range checking is enabled for memory operations.

Figure 6-21. Data Event Address Register Format (PMD[2,3,17])



6.2.7.5 Data Cache Load Miss Monitoring (PMC[11].tlb=0)

If the Data EAR is configured to monitor data cache load misses (PMC[11].tlb=0), the umask is used as a load latency threshold defined by Table 6-17.

As defined in Table 6-18, the instruction and data addresses as well as the load latency of a captured data cache load miss is presented to software in three registers PMD[2,3,17]. If no qualified event was captured, the valid bit in PMD[3] is zero. In data cache load miss mode, the level field of PMD[3] is undefined.

Table 6-17. PMC[11] Mask Fields in Data Cache Load Miss Mode (PMC[11].tlb=0)

umask Bits 3:0	Latency Threshold [CPU cycles]	umask Bits 3:0	Latency Threshold [CPU cycles]
0000	>= 4	0110	>= 256
0001	>= 8	0111	>= 512
0010	>= 16	1000	>= 1024
0011	>= 32	1001	>= 2048
0100	>= 64	1010	>= 4096
0101	>= 128	1011.. 1111	No events are captured.

Table 6-18. PMD[2,3,17] Fields in Data Cache Load Miss Mode (PMC[11].tlb=0)

Register	Fields	Bit Range	Description
PMD[2]	Data Address	63:0	64-bit address of data item that caused miss[a]
PMD[3]	latency	11:0	Latency in CPU clocks
	level	63:62	Undefined in data cache load miss mode
PMD[17]	valid	0	Valid bit 0: invalid address (EAR did not capture qualified event) 1: EAR contains valid event data
	slot	3:2	Instruction bundle slot of memory instruction. For IA-32 ISA mode, this field is undefined.
	Instruction Address	63:4	Address of bundle that contains memory instruction.[a]

a. The Itanium processor does not implement virtual address bits va{60:51} and physical address bits pa{62:44}. The data/instruction address bits {60:51} of PMD[2,17] read as a sign-extension of bit {50}. Writes to bits {60:51} of PMD[2,17] are ignored by the processor.

The detection of data cache load misses requires a load instruction to be tracked during multiple clock cycles from instruction issue to cache miss occurrence. Since multiple loads may be outstanding at any point in time and the Itanium processor data cache miss event address register can only track a single load at a time, not all data cache load misses may be captured. When the processor hardware captures the address of a load (called the monitored load), it ignores all other overlapped concurrent loads until it is determined whether the monitored load turns out to be an L1 data cache miss or not. If the monitored load turns out to be a cache miss, its parameters are latched into PMD[2,3,17]. The processor randomizes the choice of which load instructions are tracked to prevent the same data cache load miss from always being captured (in a regular sequence of overlapped data cache load misses). While this mechanism will not always capture all data cache load misses in a particular sequence of overlapped loads, its accuracy is sufficient to be used by statistical sampling or code instrumentation.

6.2.7.6 Data TLB Miss Monitoring (PMC[11].tlb=1)

If the Data EAR is configured to monitor data TLB misses (PMC[11].tlb=1), the umask defined by Table 6-19 determine which data TLB misses are captured by the Data EAR. For TLB monitoring, all combinations of the mask bits are supported.

Table 6-19. PMC[11] Unmask Field in TLB Miss Mode (PMC[11].tlb=1)

umask Bit	Data EAR Unit Mask (L1 data TLB misses)
0	reserved
1	if one, capture L1 TLB misses that hit L2 Data TLB
2	if one, capture L1 TLB misses that hit VHPT
3	if one, capture L1 TLB misses that was handled by software

As defined in Table 6-20, the instruction and data addresses of captured data TLB misses are presented to software in PMD[2,17]. The level of the TLB hierarchy from which the L1 data TLB miss was satisfied is recorded in the level field of PMD[3]. If no qualified event was captured, the valid bit in PMD[17] and the level field in PMD[3] read zero. When programmed for data TLB monitoring, the contents of the latency field of PMD[3] are undefined.

Table 6-20. PMD[2,3,17] Fields in TLB Miss Mode (PMC[11].tlb=1)

Register	Field	Bit Range	Description
PMD[2]	Data Address	63:0	64-bit address of data item that caused miss[a]
PMD[3]	latency	11:0	Undefined in TLB Miss mode
	level	63:62	Data TLB Miss Level 0: invalid address (EAR did not capture qualified event) 1: L2 Data TLB hit 2: VHPT hit 3: Data TLB miss handled by software
PMD[17]	valid	0	Valid Bit: 0: invalid address (EAR did not capture qualified event) 1: EAR contains valid event data
	slot	3:2	Instruction Bundle Slot of memory instruction. In IA-32 ISA mode, this field is undefined.
	Instruction Address	63:4	Address of bundle that contains memory instruction[a]

a. The Itanium processor does not implement virtual address bits va{60:51} and physical address bits pa{62:44}. The data/instruction address bits {60:51} of PMD[2,17] read as a sign-extension of bit {50}. Writes to bits {60:51} of PMD[2,17] are ignored by the processor.

6.2.8 Intel® Itanium™ Branch Trace Buffer

The branch trace buffer provides information about the outcome of the most recent Itanium branch instructions and their predictions and outcomes. The Itanium branch trace buffer configuration register (PMC[12]) defines the conditions under which branch instructions are captured and allows the trace buffer to capture specific subsets of branch events. The Itanium branch trace buffer operates only during Itanium-based code execution (i.e. when PSR.is is zero).

In every cycle in which a qualified Itanium branch retires, its source bundle address and slot number are written to the branch trace buffer. The branches' target address is written to the next buffer location. If the target instruction bundle itself contains a qualified Itanium branch, the branch

trace buffer either records a single trace buffer entry (with the b-bit set) or makes two trace buffer entries: one that records the target instruction as a branch target (b-bit cleared), and another that records the target instruction as a branch source (b-bit set). As a result, the branch trace buffer may contain a mixed sequence of the branches and targets.

6.2.8.1 Intel® Itanium™ Trace Buffer Collection Constraining

The Itanium branch trace buffer configuration register (PMC[12]) defines the conditions under which branch instructions are captured. These conditions are given in Figure 6-22 and Table 6-21, and refer to conditions associated with the branch prediction and resolution hardware. These conditions are:

- Which branch prediction hardware structure made the prediction,
- The path of the branch (not taken/taken),
- Whether or not the branch path was mispredicted, and
- Whether or not the target of the branch was mispredicted.

Figure 6-22. Intel® Itanium™ Branch Trace Buffer Configuration Register (PMC[12])

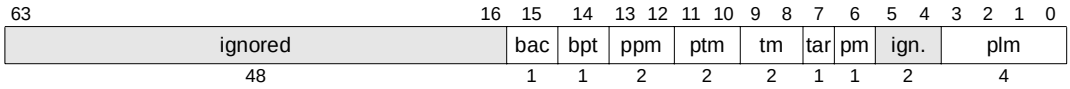


Table 6-21. Intel® Itanium™ Branch Trace Buffer Configuration Register Fields (PMC[12])

Field	Bits	Description
plm	3:0	See Table 6-11.
pm	6	See Table 6-11.
tar	7	Target Address Register: 1: capture TAR predictions 0: No TAR predictions are captured
tm	9:8	Taken Mask: 11: all Intel® Itanium™ branches 10: Taken Intel® Itanium™ branches only 01: Not Taken Intel® Itanium™ branches only 00: No branch is captured
ptm	11:10	Predicted Target Address Mask: 11: capture branch regardless of target prediction outcome 10: branch predicted target address correctly 01: branch mispredicted target address 00: No branch is captured
ppm	13:12	Predicted Predicate Mask: 11: capture branch regardless of predicate prediction outcome 10: branch predicted branch path (taken/not taken) correctly 01: branch mispredicted branch path (taken/not taken) 00: No branch is captured
bpt	14	Branch Prediction Table: 10: No TAC predictions are captured
bac	15	Branch Address Calculator: 1: capture BAC predictions 0: No BAC predictions are captured

The Itanium processor uses the following micro-architectural structures for branch prediction: the Target Address Registers (TAR), and Target Address Cache (TAC). Using the tar and bac fields of the branch trace buffer configuration register (PMC[12]), collection in the branch trace buffer can be restricted to only branches predicted by a subset of these prediction structures.

The Target Address Registers (TAR) are a small and fast fully associative buffer that is exclusively written to by branch predict instructions with the '.imp' extension. A hit in the TAR will cause a taken prediction and yield the target address of the branch. If the tar field in the branch trace buffer configuration register (PMC[12]) is set to one, branches predicted by TAR will be included in the trace buffer.

The Target Address Cache (TAC) is a larger structure that is also written to by branch predict instructions, or the prediction hardware. The primary function of the TAC is to provide the target address of a branch.

If the bpt field in the branch trace buffer configuration register (PMC[12]) is set to one, branches predicted by the TAC will be included in the trace buffer.

If neither the TAR nor TAC generated a hit, the branch has to be predicted using the static hints encoded in the branches and the target address has to be calculated. This is done by the branch address corrector (BAC). If the bac field in the branch trace buffer configuration register (PMC[12]) is set to one, branches predicted by the branch address corrector will be included in the trace buffer.

Furthermore, using the ptm, ppm and tm fields in the branch trace buffer configuration register (PMC[12]) collection in the branch trace buffer can be restricted based on the correctness of target and predicate prediction in addition to whether the branch was actually taken or not.

To summarize, an Itanium branch and its target are captured by the trace buffer if the following equation is true:

```
(not PSR.is)
and (       (tm[1] and branch taken)
        or (tm[0] and branch not taken)
    )
and (       (ptm[1] and hardware predicted target address correctly
                    and hardware predicted the branch path correctly
                    and branch is taken)
        or  (ptm[0] and hardware mispredicted target address
                    and hardware predicted the branch path correctly
                    and branch is taken)
        or (ptm[0] and ptm[1])
    )
and (       (ppm[1] and hardware predicted the branch path correctly)
        or  (ppm[0] and hardware mispredicted the branch path)
    )
and (       (bpt and branch was predicted by TAC)
        or  (bac and branch was predicted by BAC)
        or  (tar and branch was predicted by TAR)
    )
```

To capture all mispredicted Itanium branches, the branch trace buffer configuration settings in PMC[12] should be: Tm=11, ptm=01, ppm=01, bpt=1, bac=1, and tar=1.

6.2.8.2 Intel® Itanium™ Branch Trace Buffer Reading

The eight branch trace buffer registers PMD[8-15] provide information about the outcome of a captured branch sequence. The branch trace buffer registers (PMD[8-15]) contain valid data only when event collection is frozen (PMC[0].fr is one). While event collection is enabled, reads of PMD[8-15] return undefined values. The registers follow the layout defined in Figure 6-23, and contain the address of either a captured branch instruction (b-bit=1) or branch target (b-bit=0). For branch instructions, the mp-bit indicates a branch misprediction. A branch trace register with a zero b-bit and a zero mp-bit indicates an invalid branch trace buffer entry. The slot field captures the slot number of the first taken Itanium branch instruction in the captured instruction bundle. A slot number of 3 indicates a not-taken branch. The target address bundle of a branch to IA-32 (`br.ia`) is recorded. An IA-32 JMPE branch instruction and its Itanium-based target are not recorded.

Figure 6-23. Branch Trace Buffer Register Format (PMD[8-15])

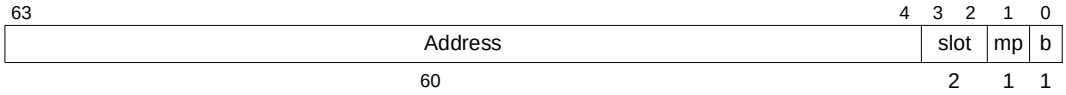


Table 6-22. Intel® Itanium™ Branch Trace Buffer Register Fields (PMD[8-15])

Field	Bit Range	Description
b	0	Branch Bit 1: contents of register is a branch instruction 0: contents of register is a branch target
mp	1	Mispredict Bit if b=1 and mp=1: mispredicted branch (due to target or predicate misprediction) if b=1 and mp=0: correctly predicted branch if b=0 and mp=0: **invalid branch trace buffer register** if b=0 and mp=1: valid target address
slot	3:2	if b=0: 00 if b=1: Slot index of first taken branch instruction in bundle 00: Itanium™-based Slot 0 branch/target 01: Itanium™-based Slot 1 branch/target 10: Itanium™-based Slot 2 branch/target 11: this was a not taken branch
Address	63:4	if b=1: 60-bit bundle address of Intel® Itanium™ branch instruction[a] if b=0: 60-bit target bundle address of Intel® Itanium™ branch instruction[a]

a. The Itanium processor does not implement virtual address bits va{60:51} and physical address bits pa{62:44}. When the processor captures an instruction address, bits {60:51} of PMD[8-15] are written by the processor with a sign-extension of bit {50} of the captured address. When PMD[8-15] are written by software bits {60:51} of PMD[8-15] can be written with any value (not necessarily a sign-extension of bit {50}).

In every cycle in which a qualified Itanium branch retires[1], its source bundle address and slot number are written to the branch trace buffer. The branches' target address is written to the next buffer location. If the target instruction bundle itself contains a qualified Itanium branch, the branch trace buffer either records a single trace buffer entry (with the b-bit set) or makes two trace buffer

1. In some cases, the Itanium processor branch trace buffer will capture the source (but not the target) address of an excepting branch instruction. This occurs on trapping branch instructions as well as faulting `br.ia`, `break.b` and multiway branches.

entries: one that records the target instruction as a branch target (b-bit cleared), and another that records the target instruction as a branch source (b-bit set). As a result, the branch trace buffer may contain a mixed sequence of the branches and targets.

The Itanium branch trace buffer is a circular buffer containing the last four to eight qualified Itanium branches. The Branch Trace Buffer Index Register (PMD[16]) defined in Figure 6-24 identifies the most recently recorded branch or target. In every cycle in which a qualified branch (branch or target) is recorded, the branch buffer index (bbi) is post-incremented. After 8 entries have been recorded, the branch index wraps around, and the next qualified branch will overwrite the first trace buffer entry. The wrap condition itself is recorded in the full bit of PMD[16]. The bbi field of PMD[16] defines the next branch buffer index that is about to be written.The following formula computes the last written branch trace buffer PMD index from the contents of PMD[16]:

last-written-PMD-index = 8+ ([(8*PMD[16].full) + (PMC[16].bbi - 1)] % 8)

If both the full bit and the bbi field of PMD[16] are zero, no qualified branch has been captured by the branch trace buffer. The full bit gets set the every time the branch trace buffer wraps from PMD[15] to PMD[8]. Once set, the full bit remains set until explicitly cleared by software, i.e. it is a sticky bit. Software can reset the bbi index and the full bit by writing to PMD[16].

Figure 6-24. Intel® Itanium™ Branch Trace Buffer Index Register Format (PMD[16])

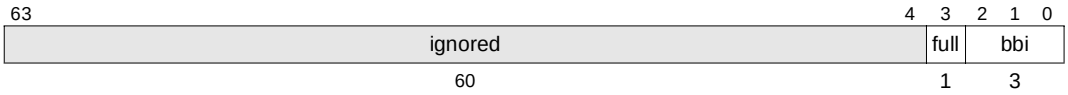


Table 6-23. Intel® Itanium™ Branch Trace Buffer Index Register Fields (PMD[16])

Field	Bit Range	Description
bbi	2:0	Branch Buffer Index [Range 0..7 - Index 0 indicates PMD[8]] Pointer to the next branch trace buffer entry to be written. if full=1: points to the oldest recorded branch/target if full=0: points to the next location to be written
full	3	Full Bit (sticky) if full=1: branch trace buffer has wrapped if full=0: branch trace buffer has not wrapped

6.2.9 Processor Reset, PAL Calls, and Low Power State

Processor Reset: On processor hardware reset bits oi, ev of all PMC registers are zero, and PMV.m is set to one. This ensures that no interrupts are generated, and events are not externally visible. On reset, PAL firmware ensures that the instruction address range check, the opcode matcher and the data address range check are initialized as follows:

- PMC[13].ta=1,
- PMC[8,9].mifb=1111, PMC[8,9].mask{29:3}= “all 1s”, PMC[8,9].match{59:33}= “all 0s”, and
- PMC[11].pt is 1.

All other performance monitoring related state is undefined.

PAL Call: As defined in Chapter 11, “Processor Abstraction Layer”in Volume 2 of the *Intel® Itanium™ Architecture Software Developer’s Manual*, the PAL call PAL_PERF_MON_INFO provides software with information about the implemented performance monitors. The Itanium processor specific values are summarized in Table 6-24.

Low Power State: To ensure that monitor counts are preserved when the processor enters low power state, PAL_LIGHT_HALT freezes event monitoring prior to powering down the processor. PAL_LIGHT_HALT preserves the original value of the PMC[0] register.

Table 6-24. Information Returned by PAL_PERF_MON_INFO for the Intel® Itanium™ Processor

PAL_PERF_MON_INFO Return Value	Description	Intel® Itanium™ Processor-specific Value
PAL_RETIRED	8-bit unsigned event type for counting the number of untagged retired Intel® Itanium™ instructions.	0x08
PAL_CYCLES	8-bit unsigned event type for counting the number of running CPU cycles.	0x12
PAL_WIDTH	8-bit unsigned number of implemented counter bits.	32
PAL_GENERIC_PM_PAIRS	8-bit unsigned number of generic PMC/PMD pairs.	4
PAL_PMCmask	256-bit mask defining which PMC registers are populated.	0x3FFF
PAL_PMDmask	256-bit mask defining which PMD registers are populated.	0x3FFFF
PAL_CYCLES_MASK	256-bit mask defining which PMC/PMD counters can count running CPU cycles (event defined by PAL_CYCLES)	0xF0
PAL_RETIRED_MASK	256-bit mask defining which PMC/PMD counters can count untagged retired Intel® Itanium™ instructions (event defined by PAL_RETIRED)	0x10

6.2.10 References

- [gprof] S.L. Graham S.L., P.B. Kessler and M.K. McKusick, “gprof: A Call Graph Execution Profiler”, Proceedings SIGPLAN’82 Symposium on Compiler Construction; SIGPLAN Notices; Vol. 17, No. 6, pp. 120-126, June 1982.
- [Lebeck] Alvin R. Lebeck and David A. Wood, “Cache Profiling and the SPEC benchmarks: A Case Study”, Tech Report 1164, Computer Science Dept., University of Wisconsin - Madison, July 1993.
- [VTune] Mark Atkins and Ramesh Subramaniam, “PC Software Performance Tuning”, IEEE Computer, Vol. 29, No. 8, pp. 47-54, August 1996.
- [WinNT] Russ Blake, “Optimizing Windows NT™”, Volume 4 of the Microsoft “Windows NT Resource Kit for Windows NT Version 3.51”, Microsoft Press, 1995.

Performance Monitor Events 7

This chapter describes the architectural and microarchitectural events on the Itanium processor whose occurrences are countable through the performance monitoring mechanisms described earlier in Chapter 6. The earlier sections of this chapter aim to provide a high-level view of the event list, grouping logically related events together. Computation (either directly by a counter in hardware, or indirectly as a “derived” event) of common performance metrics is also discussed. Each directly measurable event is then described in greater detail in the alphabetized list of all processor events in Section 7.8, “Performance Monitor Event List”.

7.1 Categorization of Events

Performance related events are grouped into the following categories:

- Basic Events: clock cycles, retired instructions (Section 7.2)
- Instruction Execution: instruction decode, issue and execution, data and control speculation, and memory operations (Section 7.3)
- Cycle Accounting Events: stall and execution cycle breakdowns (Section 7.4)
- Branch Events: branch prediction (Section 7.5)
- Memory Hierarchy: instruction and data caches (Section 7.6)
- System Events: operating system monitors, instruction and data TLBs (Section 7.7)

Each section listed above includes a table of all events (both directly measured and derived) in that category. Directly measurable events often use the PMC.umask field (See Table 6-7 in Chapter 6) to measure a certain variant of the event in question. Symbolic event names for such events (e.g. ALAT_REPLACEMENT.ALL) include a period to indicate use of the umask, specified by 4 bits in the detailed event description (x’s are for don’t-cares). Derived events are computable from directly measured events and include a “.d” suffix in their symbolic event names. Formulas to compute relevant derived events also appear in each section. Derived events are not, however, discussed in the systematic event listing in Section 7.8.

The tables in the subsequent sections define events by specifying three attributes: symbolic event name, a brief event title and a reference to the detailed event description page. Derived events are not listed in the detailed event description pages and hence lack the appropriate reference.

7.2 Basic Events

Table 7-1 summarizes four basic execution monitors. The CPU_CYCLES event can be used to break out separate or combined Itanium or IA-32 cycle counts (by constraining the PMC/PMD based on the currently executing instruction set). The Itanium retired instruction count (IA64_INST_RETIRED) includes predicated true and false instructions, and nops, but excludes RSE operations.

Table 7-1. Intel® Itanium™ and IA-32 Instruction Set Execution and Retirement Monitors

Execution Monitors	Title
CPU_CYCLES	CPU Cycles on page 88.
IA64_INST_RETIRED	Retired Itanium Instructions on page 92.
IA32_INST_RETIRED	Retired IA-32 Instructions on page 92.
ISA_TRANSITIONS	Itanium ISA to IA-32 ISA Transitions on page 94.

Table 7-2 defines IPC and average instructions/cycles per ISA transition metrics.

Table 7-2. Intel® Itanium™ and IA-32 Instruction Set Execution and Retirement Performance Metrics

Performance Metric	Performance Monitor Equation
Intel® Itanium™ Instruction per Cycle	IA64_INST_RETIRED / CPU_CYCLES [Intel® Itanium™ only]
IA-32 Instruction per Cycle	IA32_INST_RETIRED / CPU_CYCLES [IA-32 only]
Average Intel® Itanium™ Instructions/Transition	IA64_INST_RETIRED/ (ISA_TRANSITIONS*2)
Average IA-32 Instructions/Transition	IA32_INST_RETIRED/ (ISA_TRANSITIONS*2)
Average Intel® Itanium™ Cycles/Transition	CPU_CYCLES[IA64]/ (ISA_TRANSITIONS*2)
Average IA-32 Cycles/Transition	CPU_CYCLES[IA32]/ (ISA_TRANSITIONS*2)

7.3 Instruction Execution

This section describes events related to instruction issue and retirement (Table 7-3, Table 7-4) multi-media and FP (Table 7-5), data and control speculation (Table 7-7), as well as memory monitors (Table 7-9).

Table 7-3. Instruction Issue and Retirement Events

Decode, Issue, Retirement Monitors	Description
INST_DISPERSED	Instructions Dispersed on page 93.
EXPL_STOPS_DISPERSED	Explicit Stops Dispersed on page 91.
ALL_STOPS_DISPERSED	Implicit and Explicit Stops Dispersed on page 67.
IA64_TAGGED_INST_RETIRED	Retired Tagged Itanium Instructions on page 92.
NOPS_RETIRED	Retired Nop Instructions on page 105.
PREDICATE_SQUASHED_RETIRED	Instructions Squashed Due to Predicate Off on page 106.
RSE_REFERENCES_RETIRED	RSE Accesses on page 107.
RSE_LOADS_RETIRED	RSE Load Accesses on page 106.

Table 7-4. Instruction Issue and Retirement Events (Derived)

Decode, Issue, Retirement Monitors	Description	Performance Monitor Equation
RSE_STORES_RETIRED.d	RSE Store Accesses	RSE_REFERENCES_RETIRED - RSE_LOADS_RETIRED

Instruction cache lines are delivered to the execution core and are dispersed to the Itanium processor functional units. The number of dispersed instructions (INST_DISPERSED) on every cycle depends on the stops in the instruction stream (EXPL_STOPS_DISPERSED) as well as

functional unit availability. Resource limitations and branch bundles (regardless of prediction) force a break in the instruction dispersal. Therefore, they are known as implicit stops, and can be computed as ALL_STOPS_DISPERSED - EXPL_STOPS_DISPERSED.

Retired instruction counts (IA64_TAGGED_INST_RETIRED, NOPS_RETIRED) are based on tag information specified by the address range check and opcode match facilities. The tagged retired instruction counts include predicated off instructions. A separate event (PREDICATE_SQUASHED_RETIRED) is provided to count predicated off instructions. RSE_REFERENCES_RETIRED counts the number of retired RSE operations.

There are two ways to count the total number of retired Itanium instructions. Either the untagged IA64_INST_RETIRED event can be used or the IA64_TAGGED_INST_RETIRED event can be used by setting up the PMC_8 opcode match register to its don't care setting.

The FP monitors listed in Table 7-5 (FP_SIR_FLUSH, FP_FLUSH_TO_ZERO) capture dynamic information about pipeline flushes and flush-to-zero occurrences due to floating-point operations. FP_OPS_RETIRED.d is a derived event that counts the number of retired FP operations.

Table 7-5. Floating-point Execution Monitors

Floating-point Monitors	Description
FP_FLUSH_TO_ZERO	FP Result Flushed to Zero on page 91.
FP_SIR_FLUSH	FP SIR Flushes on page 92.

Table 7-6. Floating-point Execution Monitors (Derived)

Floating-Point Monitors	Description	Performance Monitor Equation
FP_OPS_RETIRED.d	FP Operations Retired	(4 * FP_OPS_RETIRED_HI) + FP_OPS_RETIRED_LO

As Table 7-7 describes, monitors for control and data speculation capture dynamic run-time information: the number of failed chk.s instructions (INST_FAILED_CHKS_RETIRED.ALL), the number of advanced load checks and check loads (ALAT_INST_CHKA_LDC.ALL) and failed advanced load checks and check loads (ALAT_INST_FAILED_CHKA_LDC.ALL) as seen by the ALAT. The number of retired chk.s instructions is monitored by the IA64_TAGGED_INST_RETIRED event with the appropriate opcode mask. Since the Itanium processor ALAT is updated by operations on mispredicted branch paths the number of advanced load checks and check loads needs an explicit event (ALAT_INST_CHKA_LDC.ALL). Finally, the ALAT_REPLACEMENT.ALL event can be used to monitor ALAT overflows.

Table 7-7. Control and Data Speculation Monitors

Control and Data Speculation Monitors	Description
INST_FAILED_CHKS_RETIRED.ALL	Failed Speculative Check Loads on page 93.
ALAT_INST_CHKA_LDC.ALL	Advanced Load Checks and Check Loads on page 65.
ALAT_INST_FAILED_CHKA_LDC.ALL	Failed Advanced Load Checks and Check Loads on page 66.
ALAT_REPLACEMENT.ALL	ALAT Entries Replaced by Any Instruction on page 64.

Using an instruction type unit mask the four control and data speculation events can be constrained to monitor integer, FP or all speculative instructions. With the Itanium processor speculation monitors, the performance metrics described in Table 7-8 can be computed.

Table 7-8. Control/Data Speculation Performance Metrics

Performance Metric	Performance Monitor Equation
Control Speculation Miss Ratio	INST_FAILED_CHKS_RETIRED.ALL / (IA64_TAGGED_INST_RETIRED[chk.s]-PREDICATE_SQUASHED_RETIRED[chk.s])
Data Speculation Miss Ratio	ALAT_INST_FAILED_CHKA_LDC.ALL / ALAT_INST_CHKA_LDC.ALL
ALAT Capacity Miss Ratio	ALAT_REPLACEMENT.ALL/ IA64_TAGGED_INST_RETIRED[ld.a,ld.sa,ld.c.nc, ldf.a, ldf.sa, ldf.c.nc]-PREDICATE_SQUASHED_RETIRED[ld.a, ld.sa, ld.c.nc, ldf.a, ldf.sa, ldf.c.nc])

The equations described in Table 7-8 for Control Speculation Miss Ratio and ALAT Capacity Miss Ratio involve subtracting PREDICATE_SQUASHED_RETIRED[some inst] from IA64_TAGGED_INST_RETIRED[some inst]. This is done because IA64_TAGGED_INST_RETIRED includes predicated off instructions in its count, which do not update architectural state and hence need to be discounted in computing any performance metric. Using the opcode matcher in PMC8 with PREDICATE_SQUASHED_RETIRED (along with IA64_TAGGED_INST_RETIRED) allows us to count the number of predicated off instances of that instruction as well. Note that computing the ALAT Capacity Miss Ratio will require multiple runs in order to obtain all the terms in the equation. This is done to the limitations imposed by the opcode matcher.

Finally, Table 7-9 defines six memory instruction retirement events to count retired loads and stores. These counts include RSE operations. The load counts include failed check load instructions.

Table 7-9. Memory Events

Memory Monitors	Description
LOADS_RETIRED	Retired Loads on page 104.
STORES_RETIRED	Retired Stores on page 107.
UC_LOADS_RETIRED	Retired Uncacheable Loads on page 107.
UC_STORES_RETIRED	Retired Uncacheable Stores on page 107.
MISALIGNED_LOADS_RETIRED	Retired Unaligned Load Instructions on page 104.
MISALIGNED_STORES_RETIRED	Retired Unaligned Store Instructions on page 105.

7.4 Cycle Accounting Events

As described in Section 6.1.1.4, “Cycle Accounting”, the Itanium processor provides eight directly measured stall cycle monitors. Table 7-10 lists the cycle accounting events.

The Itanium processor classifies every clock cycle into one of 4 cycle counters, namely DEPENDENCY_ALL_CYCLE, MEMORY_CYCLE, UNSTALLED_BACKEND_CYCLE, and PIPELINE_ALL_FLUSH_CYCLE. The values of these 4 counters should add up to CPU_CYCLES.

DEPENDENCY_ALL_CYCLE counts the number of cycles lost to instruction dispersal breaks (including both explicit and implicit stops), FP-related flushes and scoreboard stalls on GR or FR dependencies on non-load instructions. That is, the monitor does not count stalls that occur when an

instruction is waiting for source operands from the memory subsystem. Also note that this monitor does not count the number of cycles when the machine is executing instructions without stalls or flushes. The DEPENDENCY_SCOREBOARD_CYCLE monitor operates similarly, but does not include instruction dispersal breaks.

Table 7-10. Stall Cycle Monitors

Stall Accounting Monitors	Description
PIPELINE_BACKEND_FLUSH_CYCLE	Combination of Pipeline Flush Cycles caused by either a Branch Misprediction or an ExceptionCategory: Stall on page 105.
DATA_ACCESS_CYCLE	Data Access Stall Cycles on page 89.
DEPENDENCY_SCOREBOARD_CYCLE	Scoreboard Dependency Cycles on page 90.
INST_ACCESS_CYCLE	Instruction Access Cycles on page 93.
PIPELINE_ALL_FLUSH_CYCLE	Combination of Pipeline Flush Cycles caused by either a front-end or a back-end source on page 105.
MEMORY_CYCLE	Combined Memory Stall Cycles on page 104.
DEPENDENCY_ALL_CYCLE	Scoreboard Dependency and Dispersal Break Cycles on page 89.
UNSTALLED_BACKEND_CYCLE	Unstalled Back-end Cycles on page 108.

MEMORY_CYCLE counts the number of cycles that the pipeline is stalled when instructions are waiting for source operands from the memory subsystem, and for pipeline flushes related to memory-access (L1D way mispredictions, DTC flushes). It also counts the number of clocks that the pipeline stalls for the Register Stack Engine to spill or fill registers to/from memory. The DATA_ACCESS_CYCLE monitor operates similarly, but excludes RSE activity.

UNSTALLED_BACKEND_CYCLE counts the number of cycles that the back-end is processing instructions without delay and the decoupling buffer between the front-end and back-end is empty. In this situation, any effect on the front-end will appear at the back-end of the pipeline. Thus, this monitor reflects the number of cycles where there are no back-end stalls or flushes, and the decoupling buffer is empty, regardless of whether the L1I and ITLB are being hit or missed. The INST_ACCESS_CYCLE monitor includes those cycles where there are no back-end stalls or flushes, the decoupling buffer is empty, and the front-end is stalled waiting on an L1I or ITLB miss.

PIPELINE_ALL_FLUSH_CYCLE counts the number of cycles lost to branch related resteers. Resteers can be classified as branch prediction resteers (which occur when the front-end correctly predicts a taken branch) or as branch misprediction resteers (which occur when the back-end determines that the front-end incorrectly predicted a taken or not-taken branch). Note that taken branches incorrectly predicted by the front-end will not be counted twice. The branch misprediction flush that occurs in the back-end will override the front-end bubble. The monitor also counts ALAT flushes, serialization flushes, MMU-IEU bypass flushes, failed control speculation flushes and other exception flushes. The monitor PIPELINE_BACKEND_FLUSH_CYCLE operates similarly, but excludes front-end resteers to correctly predicted branches (commonly known as “branch bubbles”).

Table 7-11 defines derived stall cycle accounting monitors in terms of directly measured monitors.

Table 7-11. Stall Cycle Monitors (Derived)

Stall Cycle Monitors (Derived)	Description	Performance Monitor Equation
RSE_ACTIVE_CYCLE.d	RSE Active Cycles	MEMORY_CYCLE - DATA_ACCESS_CYCLE
ISSUE_LIMIT_CYCLE.d	Issue Limit Cycles	DEPENDENCY_ALL_CYCLE - DEPENDENCY_SCOREBOARD_CYCLE
TAKEN_BRANCH_CYCLE.d	Taken Branch Cycles	PIPELINE_ALL_FLUSH_CYCLE - PIPELINE_BACKEND_FLUSH_CYCLE
UNSTALLED_PIPELINE_CYCLE.d	Unstalled Pipeline Cycles	UNSTALLED_BACKEND_CYCLE - INST_ACCESS_CYCLE

7.5 Branch Events

The five measured Itanium processor branch events listed in Table 7-12 expand into over fifty measurable branch metrics by using the unit masks described on the event pages. BRANCH_PATH provides insight into the accuracy of taken/not-taken predicate predictions; unit masks allow classification by prediction, outcome and predictor type. BRANCH_PREDICTOR classifies how branches are predicted by different predictors as they move down the branch prediction pipeline; unit masks provide finer resolution and break down events into correct predictions, incorrect predicate predictions, and incorrect target predictions. BRANCH_MULTIWAY collects events exclusively for predictions on multiway branch bundles, from which their single-way counterparts can be derived. BRANCH_TAKEN_SLOT gives information regarding the position within a bundle that actually-taken branches occupy. BRANCH_EVENT counts the number of events captured in the branch trace buffer.

Table 7-13 defines derived branch monitors in terms of directly measure monitors.

Table 7-12. Branch Monitors

Branch Events	Description
BRANCH_PATH	Accuracy of predicate (taken/not-taken) predictions.
BRANCH_PREDICTOR	Classification of how the branches are predicted in the pipeline.
BRANCH_MULTIWAY	Details on multiway branch bundle predictions (details on single-way branch bundle predictions can be derived from this event).
BRANCH_TAKEN_SLOT	Location of taken branches (if any) in a bundle.
BRANCH_EVENT	Branch Event Captured.

Table 7-13. Branch Monitors (Derived)

Branch Events	Description	Performance Monitor Equation
BRANCH_MISPREDICTIONS.d	Branch Bundles Mispredicted	(BRANCH_PREDICTOR.ALL.ALL_PREDICTIONS - BRANCH_PREDICTOR.ALL.CORRECT_PREDICTIONS) or (BRANCH_PREDICTOR.ALL.WRONG_PATH + BRANCH_PREDICTOR.ALL.WRONG_TARGET)
BRANCH_1ST_STAGE_PREDICTIONS.d	Branch Bundles (Correctly or Incorrectly) Predicted in the 1st Pipeline Stage	BRANCH_PREDICTOR.1ST_STAGE.ALL_PREDICTIONS
BRANCH_1ST_STAGE_MISPREDICTIONS.d	Branch Bundles Incorrectly Predicted in the 1st Pipeline Stage	(BRANCH_PREDICTOR.ALL.ALL_PREDICTIONS - BRANCH_PREDICTOR.ALL.CORRECT_PREDICTIONS) or (BRANCH_PREDICTOR.1ST_STAGE.WRONG_PATH + BRANCH_PREDICTOR.1ST_STAGE.WRONG_TARGET)
BRANCH_2ND_STAGE_PREDICTIONS.d	Branch Bundles (Correctly or Incorrectly) Predicted in the 2nd Pipeline Stage	BRANCH_PREDICTOR.2ND_STAGE.ALL_PREDICTIONS
BRANCH_2ND_STAGE_MISPREDICTIONS.d	Branch Bundles Incorrectly Predicted in the 2nd Pipeline Stage	(BRANCH_PREDICTOR.ALL.ALL_PREDICTIONS - BRANCH_PREDICTOR.ALL.CORRECT_PREDICTIONS) or (BRANCH_PREDICTOR.2ND_STAGE.WRONG_PATH + BRANCH_PREDICTOR.2ND_STAGE.WRONG_TARGET)
BRANCH_3RD_STAGE_PREDICTIONS.d	Branch Bundles (Correctly or Incorrectly) Predicted in the 3rd Pipeline Stage	BRANCH_PREDICTOR.3RD_STAGE.ALL_PREDICTIONS
BRANCH_3RD_STAGE_MISPREDICTIONS.d	Branch Bundles Incorrectly Predicted in the 3rd Pipeline Stage	(BRANCH_PREDICTOR.ALL.ALL_PREDICTIONS - BRANCH_PREDICTOR.ALL.CORRECT_PREDICTIONS) or (BRANCH_PREDICTOR.3RD_STAGE.WRONG_PATH + BRANCH_PREDICTOR.3RD_STAGE.WRONG_TARGET)
BRANCH_MULTIWAY_COMPONENT.d	Multiway Branch Bundle Predictions Relative to All Prediction	BRANCH_MULTIWAY.ALL_PATHS.ALL_PREDICTIONS / BRANCH_PREDICTOR.ALL.ALL_PREDICTIONS

All branch events can be qualified by instruction address range and opcode matching as described in Section 6.1.3, “Event Qualification”. Since the instruction address range check is bundle granular, qualification of multiway branches by address range is straightforward. However, for opcode matching purposes, multiway branches (MBB or BBB bundle templates) are qualified up to and including the first taken branch as follows:

```
   ((address range and opcode match on instruction slot 0)
      and (branch in slot 0 is taken))
or ((address range and opcode match on instruction slot 1)
      and (branch in slot 0 is NOT taken)
      and (branch in slot 1 is taken))
or  ((address range and opcode match on instruction slot 0 or 1 or 2)
      and (branch in slot 0 is NOT taken)
      and (branch in slot 1 is NOT taken))
```

7.6 Memory Hierarchy

This section summarizes events related to the Itanium processor's memory hierarchy. The memory hierarchy events are grouped as follows:

- L1 Instruction Cache and Prefetch (Section 7.6.1)
- L1 Data Cache (Section 7.6.2)
- L2 Unified Cache (Section 7.6.3)
- L3 Unified Cache (Section 7.6.4)

An overview of the Itanium processor's three-level memory hierarchy and its event monitors is shown in Figure 7-1. The instruction and the data stream work through separate L1 caches. The L1 data cache is a write-through cache. A unified L2 cache serves both the L1 instruction and data caches, and is backed by a large unified L3 cache. Events for individual levels of the cache hierarchy are described in the following three sections. They can be used to compute the most common cache performance ratios summarized in Table 7-15.

For common performance metrics not directly measured by hardware, the equations listed in Table 7-14 can be used.

Figure 7-1. Event Monitors in the Intel® Itanium™ Processor Memory Hierarchy

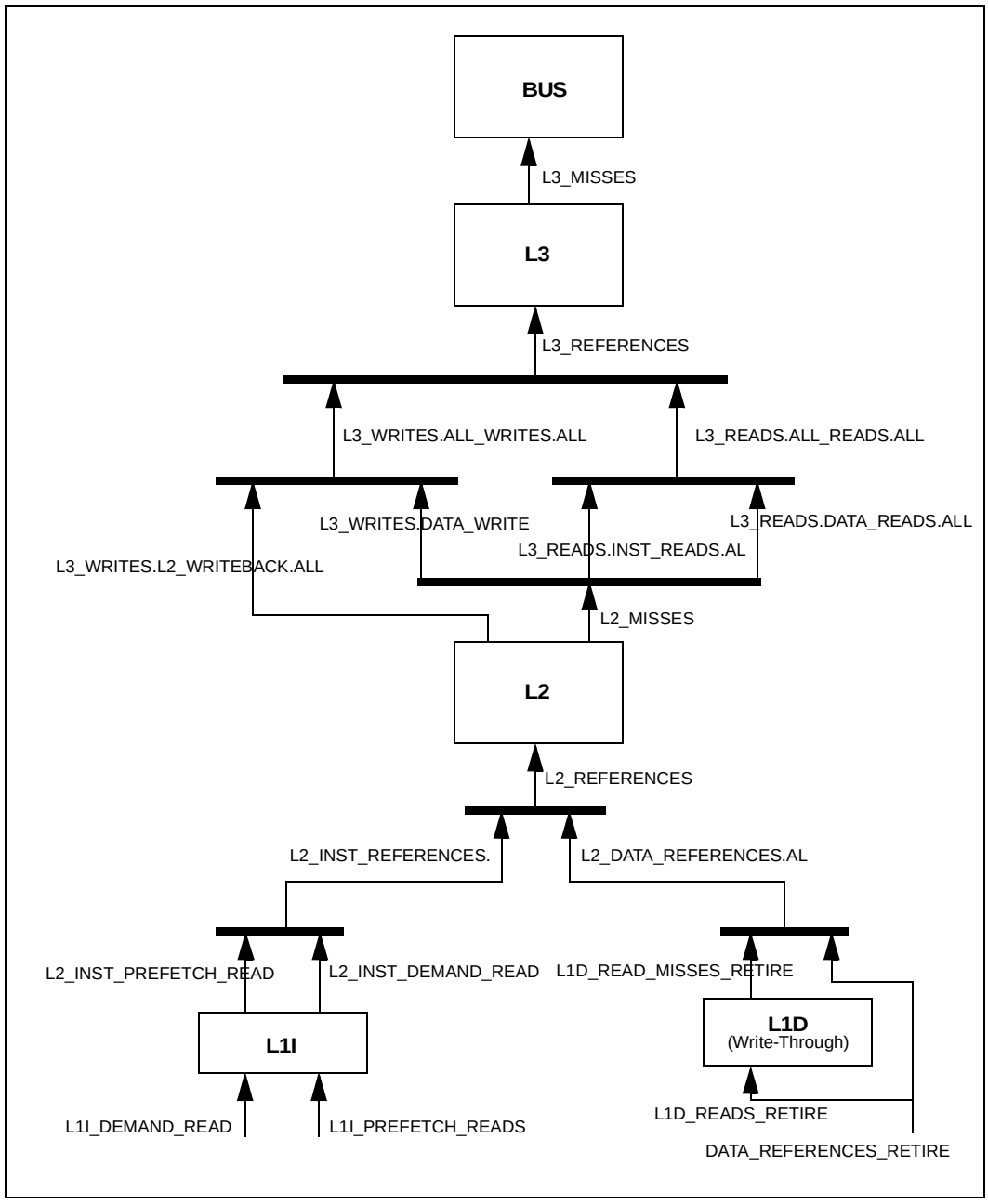


Table 7-14. Derived Memory Hierarchy Monitors

Memory Hierarchy Monitors (Derived)	Description	Performance Monitor Equation
L1I_REFERENCES.d	L1 Instruction Cache References	L1I_PREFETCH_READS + L1I_DEMAND_READS
L2_INST_REFERENCES.d	L2 Instruction References	L2_INST_DEMAND_READS + L2_INST_PREFETCH_READS
L3_DATA_REFERENCES.d	L3 Data References	L3_WRITES.DATA_WRITES.ALL+ L3_READS.DATA_READS.ALL
L3_CORRECTION_RATIO.d	L3 Correction Ratio	L2_MISSES/(L3_REFERENCES-L3_WRITES.L2_ WRITEBACK.ALL)

Because Itanium performance monitors for the L2 cache contain secondary misses from L1, and performance monitors for L3 do not, one cannot directly compare L2 and L3 performance monitors. In the performance metrics that follow in Table 7-15 where possible only events from an L2 view or an L3 view are used in computing the metric. However, several useful metrics cannot be calculated accurately this way. For those metrics we compute a correction ratio to scale L3 events to approximate a value that contains secondary misses. Table 7-14 contains the definition of this correction ratio.

Table 7-15. Cache Performance Ratios

Performance Metric	Performance Monitor Equation
L1I Miss Ratio	L2_INST_REFERENCES.d/L1I_REFERENCES.d
L1I Demand Miss Ratio	L2_INST_DEMAND_READS / L1I_DEMAND_READS
L1I Prefetch Miss Ratio	L2_INST_PREFETCH_READS/ L1I_PREFETCH_READS
L1D Read Miss Ratio	L1D_READ_MISSES_RETIRED / L1D_READS_RETIRED
L2 Miss Ratio	L2_MISSES / L2_REFERENCES
Approximate L2 Data Miss Ratio	(L3_DATA_REFERENCES.d / L2_DATA_REFERENCES.ALL)*L3_CORRECTION_RATIO.d
Approximate L2 Instruction Miss Ratio (includes prefetches)	(L3_READS.INST_READS.ALL / L2_INST_REFERENCES.d)*L3_CORRECTION_RATIO.d
Approximate L2 Data Read Miss Ratio	(L3_READS.DATA_READS.ALL / L2_DATA_REFERENCES.READS) * L3_CORRECTION_RATIO.d
Approximate L2 Data Write Miss Ratio	(L3_WRITES.DATA_WRITES.ALL / L2_DATA_REFERENCES.WRITES)*L3_CORRECTION_RATIO.d
L2 Instruction Ratio	L2_INST_REFERENCES.d/ L2_REFERENCES
L2 Data Ratio	L2_DATA_REFERENCES.ALL / L2_REFERENCES
L3 Miss Ratio	L3_MISSES /(L3_REFERENCES-L3_WRITES.L2_WRITEBACK.ALL)
L3 Data Miss Ratio	(L3_READS.DATA_READS.MISS + L3_WRITES.DATA_WRITES.MISS) / L3_DATA_REFERENCES.d
L3 Instruction Miss Ratio	L3_READS.INST_READS.MISS / L3_READS.INST_READS.ALL
L3 Data Read Ratio	L3_READS.DATA_READS.ALL / L3_DATA_REFERENCES.d
L3 Data Ratio	L3_DATA_REFERENCES.d / L3_REFERENCES
L3 Instruction Ratio	L3_READS.INST_READS.ALL / L3_REFERENCES

7.6.1 L1 Instruction Cache and Prefetch

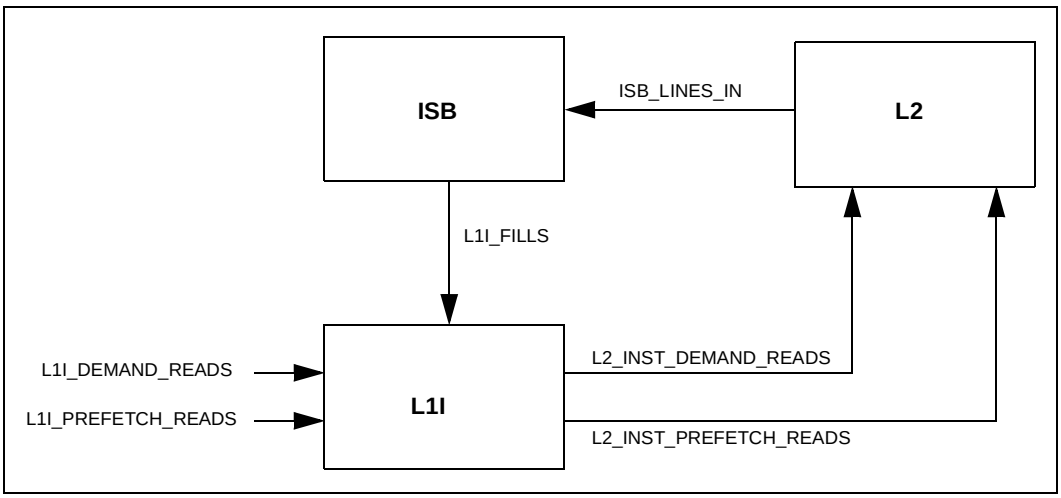
Table 7-16 and Figure 7-2 describes and summarizes the events that the Itanium processor provides to monitor the L1 instruction cache demand fetch and prefetch activity. Table 7-14 lists pertinent derived events. The instruction fetch monitors distinguish between demand fetch (L1I_DEMAND_READS, L2_INST_DEMAND_READS) and prefetch activity (L1I_PREFETCH_READS, L2_INST_PREFETCH_READS). The amount of data returned from the L2 into the L1 instruction cache and the Instruction Streaming Buffer is monitored by two events (L1I_FILLS, ISB_LINES_IN). The INSTRUCTION_EAR_EVENTS monitor (not shown in Figure 7-2) counts how many instruction cache or ITLB misses are captured by the instruction event address register.

The L1 instruction cache and prefetch events can be qualified by the instruction address range check, but not by the opcode matcher. Since instruction cache and prefetch events occur early in the processor pipeline, they include events caused by speculative, wrong-path as well as predicated off instructions. Since the address range check is not based on actually retired, but speculative instruction addresses, event counts may be inaccurate when the range checker is confined to address ranges smaller than the length of the processor pipeline (see Section 6.2.4, “Intel® Itanium™ Instruction Address Range Check Register (PMC[13])” for details).

Table 7-16. L1 Instruction Cache and Instruction Prefetch Monitors

L1I and I-Prefetch Monitors	Description
L1I_DEMAND_READS	L1I and ISB Instruction Demand Lookups on page 96.
L1I_FILLS	L1 Instruction Cache Fills on page 96.
L2_INST_DEMAND_READS	L2 Instruction Demand Fetch Requests on page 98.
INSTRUCTION_EAR_EVENTS	Instruction EAR Events on page 94.
L1I_PREFETCH_READS	L1I and ISB Instruction Prefetch Lookups on page 97.
L2_INST_PREFETCH_READS	L2 Instruction Prefetch Requests on page 99.
ISB_LINES_IN	Instruction Streaming Buffer Lines In on page 95.

Figure 7-2. L1 Instruction Cache and Prefetch Monitors



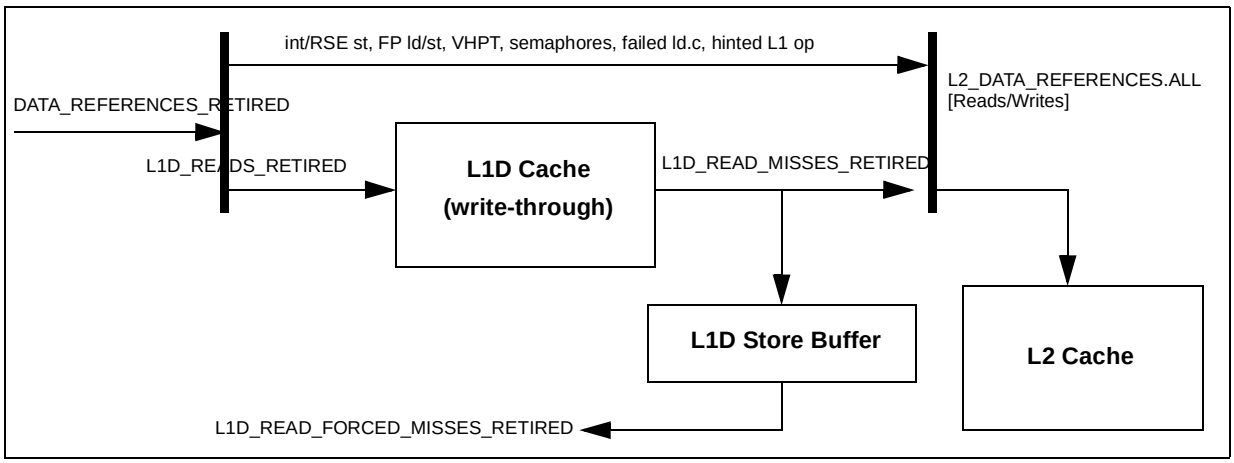
7.6.2 L1 Data Cache

Table 7-17 lists the Itanium processor's seven L1 data cache monitors. As shown in Figure 7-3, the write-through L1 data cache services cacheable loads, Integer and RSE stores, FP memory operations, VHPT references, semaphores, check loads and hinted L2 memory references. DATA_REFERENCES_RETIRED is the number of issued data memory references. L1 data cache reads (L1D_READS_RETIRED) and L1 data cache misses (L1D_READ_MISSES_RETIRED) monitor the read hit/miss rate for the L1 data cache. The number of L2 data references (L2_DATA_REFERENCES.ALL) is the number of data requests prior to cache line merging. Unit mask selections allow breaking down into reads and writes. The DATA_EAR_EVENTS monitor (not shown in Figure 7-3) counts how many data cache or DTLB misses are captured by the data event address register. RSE operations are included in all data cache monitors, but are not broken down explicitly.

Table 7-17. L1 Data Cache Monitors

L1D Monitors	Description
DATA_REFERENCES_RETIRED	Retired Data Memory References on page 89.
L1D_READS_RETIRED	L1 Data Cache Reads on page 96.
L1D_READ_MISSES_RETIRED	L1 Data Cache Read Misses on page 96.
PIPELINE_FLUSH.L1D_WAY_MISPREDICT	Pipeline Flush on page 106.
L1D_READ_FORCED_MISSES_RETIRED	L1 Data Cache Forced Load Misses on page 95.
L2_DATA_REFERENCES.ALL	L2 Data Read and Write References on page 97.
DATA_EAR_EVENTS	L1 Data Cache EAR Events on page 89.

Figure 7-3. L1 Data Cache Monitors



7.6.3 L2 Unified Cache

Table 7-18 summarizes the directly-measured events that monitor the Itanium processor L2 cache. Table 7-14 lists pertinent derived events. Refer to Figure 7-1 for a graphical view of the L2 cache monitors.

L2_REFERENCES, L2_INST_DEMAND_READS, L2_INST_PREFETCH_READS, L2_DATA_REFERENCES.ALL, and L2_MISSES are all counted in terms of number of requests seen by the L2. L2_FLUSHES and L2_FLUSH_DETAILS count and break-down the number of L2 flushes due to address conflicts, store buffer conflicts, bus rejects, and other reasons. L1D_READ_FORCED_MISSES_RETIRED counts the number of loads that were bypassed from an earlier store.

Table 7-18. L2 Cache Monitors

L1 Monitors	Description
L2_REFERENCES	L2 References on page 99.
L2_INST_PREFETCH_READS	L2 Instruction Prefetch Requests on page 99.
L2_INST_DEMAND_READS	L2 Instruction Demand Fetch Requests on page 98.
L2_DATA_REFERENCES.ALL	L2 Data Read and Write References on page 97.
L2_DATA_REFERENCES.READS	L2 Data Read References on page 97.
L2_DATA_REFERENCES.WRITES	L2 Data Write References on page 97.
L2_MISSES	L2 Misses on page 99.
L2_FLUSHES	L2 Flushes on page 98.
L2_FLUSH_DETAILS	L2 Flush Details on page 98.

7.6.4 L3 Unified Cache

Table 7-19 summarizes the directly-measured L3 cache events. Table 7-14 lists pertinent derived events. Refer to Figure 7-1 for a graphical view of the L3 cache monitors.

Table 7-19. L3 Cache Monitors

L2 Monitors	Description
L3_REFERENCES	L3 References on page 102.
L3_MISSES	L3 Misses on page 100.
L3_LINES_REPLACED	L3 Cache Lines Replaced on page 99.
L3_READS.ALL_READS.ALL	Instruction and Data L3 Reads on page 100.
L3_READS.ALL_READS.HIT	Instruction and Data L3 Read Hits on page 100.
L3_READS.ALL_READS.MISS	Instruction and Data L3 Read Misses on page 100.
L3_READS.DATA_READS.ALL	Data L3 Reads on page 100.
L3_READS.DATA_READS.HIT	Data L3 Read Hits on page 101.
L3_READS.DATA_READS.MISS	Data L3 Read Misses on page 101.
L3_READS.INST_READS.ALL	Instruction L3 Reads on page 101.
L3_READS.INST_READS.HIT	Instruction L3 Read Hits on page 101.
L3_READS.INST_READS.MISS	Instruction L3 Read Misses on page 101.
L3_WRITES.ALL_WRITES.ALL	L3 Writes on page 102.
L3_WRITES.ALL_WRITES.HIT	L3 Write Hits on page 102.

Table 7-19. L3 Cache Monitors (Continued)

L2 Monitors	Description
L3_WRITES.ALL_WRITES.MISS	L3 Write Misses on page 102.
L3_WRITES.L2_WRITEBACK.ALL	L3 Writebacks on page 103.
L3_WRITES.L2_WRITEBACK.HIT	L3 Writeback Hits on page 103.
L3_WRITES.L2_WRITEBACK.MISS	L3 Writeback Misses on page 103.
L3_WRITES.DATA_WRITES.ALL	L3 Data Writes on page 103.
L3_WRITES.DATA_WRITES.HIT	L3 Data Write Hits on page 103.
L3_WRITES.DATA_WRITES.MISS	L3 Data Write Misses on page 104.

7.6.5 Frontside Bus

Table 7-20 lists the frontside bus or system bus transaction monitors.

Table 7-20. Bus Events

L2 Monitors	Description
BUS_ALL	Bus Transactions on page 80.
BUS_PARTIAL	Bus Partial Transactions on page 84.
BUS_BURST	Bus Burst Transactions on page 82.
BUS_MEMORY	Bus Memory Transactions on page 84.
BUS_RD_ALL	Bus Read Transactions on page 84.
BUS_RD_DATA	Bus Read Data Transactions on page 84.
BUS_RD_PRTL	Bus Read Partial Transactions on page 86.
BUS_RD_HIT	Bus Read Hit Clean Non-local Cache Transactions on page 85.
BUS_RD_HITM	Bus Read Hit Modified Non-local Cache Transactions on page 85.
BUS_RD_INVAL	Bus Read Invalidated Line on page 85.
BUS_RD_INVAL_HITM	Bus BIL Transaction Results in HITM on page 86.
BUS_RD_INVAL_BST	Bus BRIL Burst Transactions on page 85.
BUS_RD_INVAL_BST_HITM	Bus BRIL Burst Transaction Results in HITM on page 86.
BUS_HITM	Bus Hit Modified Line Transactions on page 82.
BUS_WR_WB	Bus Write Back Transactions on page 88.
BUS_SNOOPS_HITM	Bus Snoops Hit Modified Cache Line on page 87.
BUS_SNOOPS	Bus Snoops Total on page 87.
BUS_SNOOP_STALL_CYCLES	Bus Snoop Stall Cycles on page 87.
BUS_SNOOPQ_REQ	Bus Snoop Queue Requests, Category: Frontside Bus on page 88.
BUS_BRQ_READ_REQ_INSERTED	BRQ Requests Inserted on page 81.
BUS_IO	IA-32 Compatible I/O Bus Transactions on page 82.
BUS_RD_IO	IA-32 Compatible I/O Read Transactions on page 86.
BUS_LOCK	IA-32 Compatible Bus Lock Transactions on page 83.
BUS_LOCK_CYCLES	IA-32 Compatible Bus Lock Cycles on page 83.

Table 7-21 lists the derived frontside bus transaction monitors.

Table 7-21. Frontside Bus Monitors (Derived)

Bus Monitors (Derived)	Description	Performance Monitor Equation
BUS_RD_INSTRUCTIONS.d	Bus Read Instructions	BUS_RD_ALL - BUS_RD_DATA
BUS_RD_INVAL_MEMORY.d	Bus BIL Transaction Satisfied from Memory	BUS_RD_INVAL - BUS_RD_INVAL_HITM
BUS_RD_INVAL_BST_MEMORY.d	Bus BRIL Burst Transaction Satisfied from Memory	BUS_RD_INVAL_BST - BUS_RD_INVAL_BST_HITM
BUS_ADDR_BPRI.d	Bus Used by I/O Agent	BUS_MEMORY.IOAGENT
BUS_IOQ_LIVE_REQ.d	In-order Bus Queue Requests	BUS_IOQ_LIVE_REQ_HI * 4 + BUS_IOQ_LIVE_REQ_LO
BUS_BRQ_LIVE_REQ.d	BRQ Live Requests	BUS_BRQ_LIVE_REQ_HI * 4 + BUS_BRQ_LIVE_REQ_LO

Most of the bus events in Section 7.6.5 can be qualified by the bus transaction initiator using the three way unit mask as described in Table 7-22.

Table 7-22. Unit Masks for Qualifying Bus Transaction Events by Initiator

Selection	PMC.umask[19:16]	Description
ANY	x001	Counts all bus transactions (initiated by any processor or non-processor bus masters)
SELF	x010	Counts bus transactions initiated by the local processor only
IO	x100	Counts bus transactions from IO agents, i.e. non-processor bus masters

Table 7-23 defines the conventions that will be used when describing the Itanium processor frontside bus transaction monitors in Section 7.6.5.

Table 7-23. Conventions for Frontside Bus Transactions

Name	Description
BRL	Memory Read (64 byte bursts). Includes code fetches and data loads from WB memory.
BRIL	Memory Read & Invalidate (64 byte bursts). Also known as read for ownership (RFO).
BIL	Memory Read & Invalidate (0 byte sized transaction). Caused by flush cache (`fc`) instruction only.
BWL	Memory Write (64 byte bursts). Explicit writebacks/coalesced writes.
BRP	Partial Memory Reads (<64 byte transactions). Typically, uncacheable reads.
BWP	Partial Memory Write (<64 byte transactions). Typically, uncacheable writes.
IORD	Partial IO Read (<64 byte transactions). Uncacheable read to IO port space.
IOWR	Partial IO Write (<64 byte transactions). Uncacheable write to IO port space.

Other transactions besides those listed in Table 7-23 include Deferred Reply, Special Transactions, Interrupt, Interrupt Acknowledge, and Purge TC. For the bus performance monitors in Section 7.6.5, note that the monitors will count if any transaction gets a retry response from the priority agent.

To support the analysis of snoop traffic in a multiprocessor system, the Itanium processor provides local processor and remote response monitors. The local processor snoop events (BUS_SNOOPS_HITM, BUS_SNOOPS, BUS_SNOOPQ_REQ) monitor inbound snoop traffic. The remote response events (BUS_RD_HIT, BUS_RD_HITM, BUS_RD_INVAL_HITM, BUS_RD_INVAL_BST_HITM) monitor the snoop responses of other processors to bus transactions that the monitoring processor originated. Table 7-24 summarizes the remote snoop events by bus transaction.

Table 7-24. Bus Events by Snoop Response

Remote Processor Response	BRL	BIL	BRIL
HIT	BUS_RD_HIT	NA	NA
HITM	BUS_RD_HITM	BUS_RD_INVAL_HITM	BUS_RD_INVAL_BST_HITM
ALL	BUS_RD_ALL	BUS_RD_INVAL	BUS_RD_INVAL

With the Itanium processor frontside bus monitors, the performance metrics described in Table 7-25 can be computed.

Table 7-25. Bus Performance Metrics

Performance Metric	Performance Monitor Equation
Cacheable Data Fetch Bus Transaction Ratio	BUS_RD_DATA/BUS_ALL or BUS_RD_DATA/BUS_MEMORY
Partial Access Ratio	BUS_PARTIAL/BUS_MEMORY
Read Partial Access Ratio	BUS_RD_PRTL/BUS_MEMORY
Read Hit To Shared Line Ratio	BUS_RD_HIT/BUS_RD_ALL or BUS_MEMORY
Read Hit to Modified Line Ratio	BUS_RD_HITM/BUS_RD_ALL or BUS_RD_HITM/BUS_MEMORY
BIL Ratio	BUS_RD_HIT/BUS_MEMORY
BIL Hit to Modified Line Ratio	BUS_RD_INVAL_HITM/BUS_MEMORY or BUS_RD_INVAL_HITM/BUS_RD_INVAL
BRIL Hit to Modified Line Ratio	BUS_RD_INVAL_BST_HITM/BUS_MEMORY or BUS_RD_INVAL_BST_HITM/BUS_RD_INVAL
Bus Modified Line Hit Ratio	BUS_RD_HITM/BUS_MEMORY or BUS_RD_HITM/BUS_BURST
Writeback Ratio	BUS_WR_WB/BUS_MEMORY or BUS_WR_WB/BUS_BURST
Cacheable Read Ratio	(BUS_RD_ALL + BUS_RD_INVAL_BST)/BUS_MEMORY
I/O Cycle Ratio	BUS_IO/BUS_ALL
I/O Read	BUS_RD_IO/BUS_ALL

7.7 System Events

Table 7-26 lists the directly measurable system and TLB events. Table 7-27 lists pertinent derived events. The debug register match events count how often the address in any instruction or data break-point register (IBR or DBR) matches the current retired instruction pointer (CODE_DEBUG_REGISTER_MATCHES.d) or the current data memory address (DATA_DEBUG_REGISTER_MATCHES.d). PIPELINE_FLUSH counts the number of times the Itanium processor pipeline is flushed due to a data translation cache miss, L1 data cache way mispredict, an exception flush or an instruction serialization event. CPU_CPL_CHANGES counts the number of privilege level transitions due to interruptions, system calls (epc) and returns (demoting branch), and `rfi` instructions. CPU_CYCLES counts the number of cycles the CPU is not powered down or in light HALT state.

Table 7-26. System and TLB Monitors

System and Processor TLB Monitors	Description
PIPELINE_FLUSH	Pipeline Flush on page 106.
CPU_CPL_CHANGES	Privilege level changes on page 88.
CPU_CYCLES	CPU Cycles on page 88.
ITLB_MISSES_FETCH	ITLB Demand Misses on page 95.
ITLB_INSERTS_HPW	Hardware Page Walker Inserts into the ITLB on page 95.
DTC_MISSES	DTC Misses on page 90.
DTLB_MISSES	DTLB Misses on page 90.
DTLB_INSERTS_HPW	Hardware Page Walker Inserts into the DTLB on page 90.

Table 7-27 defines derived system and TLB events that are computed from events directly measured by hardware.

Table 7-27. System and TLB Monitors (Derived)

Derived Memory Hierarchy Monitors	Description	Performance Monitor Equation
CODE_DEBUG_REGISTER_MATCHES.d	Code Debug Register Matches	IA64_TAGGED_INST_RETIRED
DATA_DEBUG_REGISTER_MATCHES.d	Data Debug Register Matches	LOADS_RETIRED + STORES_RETIRED
ITLB_REFERENCES.d	ITLB References	L1I_DEMAND_READS
ITLB_EAR_EVENT.d	ITLB EAR Event	INSTRUCTION_EAR_EVENTS
DTLB_REFERENCES.d	DTLB References	DATA_REFERENCES_RETIRED
DTLB_EAR_EVENT.d	DTLB EAR Event	DATA_EAR_EVENTS

The Itanium processor instruction and data TLBs and the virtual hash page table walker are monitored by the events described in Table 7-26 and Table 7-27. Figure 7-4 gives a graphical summary. Table 7-28 lists the TLB performance metrics that can be computed using these events.

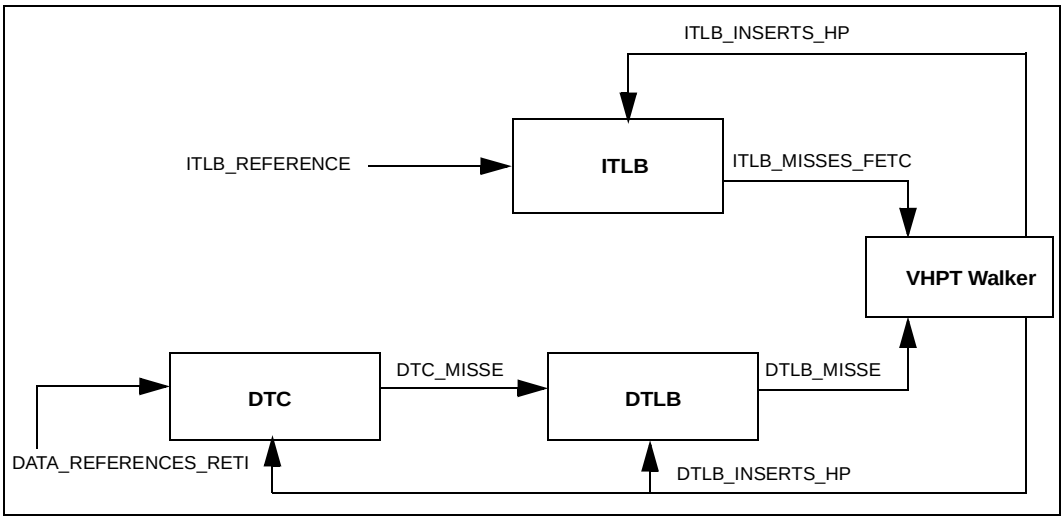
ITLB_REFERENCES.d and DTLB_REFERENCES.d are derived from the respective instruction/data cache access events. Note that ITLB_REFERENCES.d does not include prefetch requests made to the L1I cache (L1I_PREFETCH_READS). This is because prefetches are cancelled when they miss in the ITLB and thus do not trigger VHPT walks or software TLB miss handling. ITLB_MISSES_FETCH and DTLB_MISSES count TLB misses.

ITLB_INSERTS_HPW and DTLB_INSERTS_HPW count the number of instruction/data TLB inserts performed by the virtual hash page table walker. The Itanium processor data TLB is a two level TLB; DTC_MISSES counts the number of first level data TLB misses.

Table 7-28. TLB Performance Metrics

Performance Metric	Performance Monitor Equation
ITLB Miss Ratio	ITLB_MISSES_FETCH / ITLB_REFERENCES.d
DTLB Miss Ratio	DTLB_MISSES / DTLB_REFERENCES.d
DTC Miss Ratio	DTC_MISSES / DTLB_REFERENCES.d

Figure 7-4. Instruction and Data TLB Monitors



7.8 Performance Monitor Event List

This section enumerates Itanium processor performance monitoring events.

ALAT_REPLACEMENT.ALL

- **Title:** ALAT Entries Replaced by Any Instruction, **Category:** Execution
- **Definition:** ALAT_REPLACEMENT.ALL counts the number of times an advanced load (`ld.a` or `ld.as` or `ldfp.a` or `ldfp.as`) or a no-clear check load (`ld.c.nc` and variants of `ldf.c.nc`) displaced a valid entry in the ALAT
- **Event Code:** 0x38, **Umask:** xx11, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: yes

ALAT_REPLACEMENT.FP

- **Title:** ALAT Entries Replaced by FP Instructions, **Category:** Execution
- **Definition:** ALAT_REPLACEMENT.FP counts the number of times a FP advanced load (`ldfp.a` or `ldfp.as`) or a no-clear FP check load (variants of `ldf.c.nc`) displaced a valid entry in the ALAT
- **Event Code:** 0x38, **Umask:** xx10, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: yes

ALAT_REPLACEMENT.INTEGER

- **Title:** ALAT Entries Replaced by Integer Instructions, **Category:** Execution
- **Definition:** ALAT_REPLACEMENT.INTEGER counts the number of times an integer advanced load (`ld.a` or `ld.as`) or a no-clear integer check load (`ld.c.nc`) displaced a valid entry in the ALAT
- **Event Code:** 0x38, **Umask:** xx01, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: yes

ALAT_INST_CHKA_LDC.ALL

- **Title:** Advanced Load Checks and Check Loads, **Category:** Execution
- **Definition:** ALAT_INST_CHKA_LDC.ALL counts the number of all advanced load checks (`chk.a`) and check loads in both clear and no-clear forms (`ld.c.clr` or `ld.c.nc`, including FP variants) as seen by the ALAT
- **Event Code:** 0x36, **Umask:** xx11, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no for `chk.a`, and yes for `ld.c`

ALAT_INST_CHKA_LDC.FP

- **Title:** FP Advanced Load Checks and Check Loads, **Category:** Execution
- **Definition:** ALAT_INST_CHKA_LDC.FP counts all FP advanced load checks (`chk.a`) and all FP check loads in both clear and no-clear forms (`ld.c.clr` or `ld.c.nc`, FP variants only) as seen by the ALAT
- **Event Code:** 0x36, **Umask:** xx10, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no for `chk.a`, and yes for `ld.c`

ALAT_INST_CHKA_LDC.INTEGER

- **Title:** Integer Advanced Load Checks and Check Loads, **Category:** Execution
- **Definition:** ALAT_INST_CHKA_LDC.INTEGER counts all integer advanced load checks (`chk.a`) and all integer check loads in both clear and no-clear forms (`ld.c.clr` or `ld.c.nc`, excluding FP variants) as seen by the ALAT
- **Event Code:** 0x36, **Umask:** xx01, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no for `chk.a`, and yes for `ld.c`

ALAT_INST_FAILED_CHKA_LDC.ALL

- **Title:** Failed Advanced Load Checks and Check Loads, **Category:** Execution
- **Definition:** ALAT_INST_FAILED_CHKA_LDC.ALL counts failed advanced load checks (`chk.a`) and failed check loads in both clear and no-clear forms (`ld.c.clr` or `ld.c.nc`, including FP variants) as seen by the ALAT
- **Event Code:** 0x37, **Umask:** xx11, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no for `chk.a`, and yes for `ld.c`

ALAT_INST_FAILED_CHKA_LDC.FP

- **Title:** Failed FP Advanced Load Checks and Check Loads, **Category:** Execution
- **Definition:** ALAT_INST_FAILED_CHKA_LDC.FP counts failed FP advanced load checks (`chk.a`) and failed FP check loads in both clear and no-clear forms (`ld.c.clr` or `ld.c.nc`, FP variants only) as seen by the ALAT
- **Event Code:** 0x37, **Umask:** xx10, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no for `chk.a`, and yes for `ld.c`

ALAT_INST_FAILED_CHKA_LDC.INTEGER

- **Title:** Failed Integer Advanced Load Checks and Check Loads, **Category:** Execution
- **Definition:** ALAT_INST_FAILED_CHKA_LDC.INTEGER counts the number of failed integer advanced load checks (`chk.a`) and failed integer check loads in both clear and no-clear forms (`ld.c.clr` or `ld.c.nc`, excluding FP variants) as seen by the ALAT
- **Event Code:** 0x37, **Umask:** xx01, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no for `chk.a`, and yes for `ld.c`

ALL_STOPS_DISPERSED

- **Title:** Implicit and Explicit Stops Dispersed, **Category:** Instruction Issue
- **Definition:** ALL_STOPS_DISPERSED counts the sum of explicit programmer-specified stops (EXPL_STOPS_DISPERSED) and dispersal breaks due to resource limitations and branch instructions (independent of their predicate prediction).The sum includes stops encountered during hardware speculative wrong-path execution (i.e., in the shadow of a flush)
- **Event Code:** 0x2F, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

BRANCH_EVENT

- **Title:** Branch Event Captured, **Category:** Branch
- **Definition:** BRANCH_EVENT counts the number of branch events, including multiway branches captured by the Branch Trace Buffer.
- **Event Code:** 0x11, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.ALL_PATHS.ALL_PREDICTIONS

- **Title:** All Branch Predictions on Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.ALL_PATHS.ALL_PREDICTIONS counts all branch predictions made on multiway branch bundles
- **Event Code:** 0x0E, **Umask:** 0000, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.ALL_PATHS.CORRECT_PREDICTIONS

- **Title:** Correct Branch Predictions on Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.ALL_PATHS.CORRECT_PREDICTIONS counts all branch predictions on multiway branch bundles that do not necessitate a back-end branch misprediction flush
- **Event Code:** 0x0E, **Umask:** 0001, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.ALL_PATHS.WRONG_PATH

- **Title:** Incorrect Predicate Predictions on Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.ALL_PATHS.WRONG_PATH counts the number of multiway branch bundles whose combined predicate is incorrectly predicted. This includes bundles where all branch instructions are predicted not-taken and any one instruction is actually taken, and those bundles where a branch instruction was predicted taken and either a prior branch instruction in the bundle was actually taken or the predicted instruction was not taken. In any event, the processor resteers the front-end to the correct target, i.e., a given multiway bundle can only be mispredicted once
- **Event Code:** 0x0E, **Umask:** 0010, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.ALL_PATHS.WRONG_TARGET

- **Title:** Incorrect Target Predictions on Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.ALL_PATHS.WRONG_TARGET counts the number of multiway branch bundles where a branch instruction is correctly predicted taken, but its target is incorrect
- **Event Code:** 0x0E, **Umask:** 0011, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.NOT_TAKEN.ALL_PREDICTIONS

- **Title:** All Branch Predictions on Not-Taken Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.NOT_TAKEN.ALL_PREDICTIONS is analogous to BRANCH_MULTIWAY.ALL_PATHS.ALL_PREDICTIONS, except it applies only to multiway branch bundles where all branch instructions are actually not taken
- **Event Code:** 0x0E, **Umask:** 1000, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.NOT_TAKEN.CORRECT_PREDICTIONS

- **Title:** Correct Branch Predictions on Not-Taken Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.NOT_TAKEN.CORRECT_PREDICTIONS is analogous to BRANCH_MULTIWAY.ALL_PATHS.CORRECT_PREDICTIONS, except it applies only to multiway branch bundles where all branch instructions are actually not taken
- **Event Code:** 0x0E, **Umask:** 1001, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.NOT_TAKEN.WRONG_PATH

- **Title:** Incorrect Predicate Predictions on Not-Taken Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.NOT_TAKEN.WRONG_PATH is analogous to BRANCH_MULTIWAY.ALL_PATHS.WRONG_PATH, except it applies only to multi-way branch bundles where all branch instructions are actually not taken
- **Event Code:** 0x0E, **Umask:** 1010, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.NOT_TAKEN.WRONG_TARGET

- **Title:** Incorrect Target Predictions on Not-Taken Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.NOT_TAKEN.WRONG_TARGET should always count zero, as not-taken branches do not specify a branch target
- **Event Code:** 0x0E, **Umask:** 1011, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.TAKEN.ALL_PREDICTIONS

- **Title:** All Branch Predictions on Taken Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.TAKEN.ALL_PREDICTIONS is analogous to BRANCH_MULTIWAY.ALL_PATHS.ALL_PREDICTIONS, except it applies only to multiway branch bundles where at least one branch instruction is taken
- **Event Code:** 0x0E, **Umask:** 1100, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.TAKEN.CORRECT_PREDICTIONS

- **Title:** Correct Branch Predictions on Taken Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.TAKEN.CORRECT_PREDICTIONS is analogous to BRANCH_MULTIWAY.ALL_PATHS.CORRECT_PREDICTIONS, except it applies only to multiway branch bundles where at least one branch instruction is taken
- **Event Code:** 0x0E, **Umask:** 1101, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.TAKEN.WRONG_PATH

- **Title:** Incorrect Predicate Predictions on Taken Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.TAKEN.WRONG_PATH is analogous to BRANCH_MULTIWAY.ALL_PATHS.WRONG_PATH, except it applies only to multi-way branch bundles where at least one branch instruction is taken
- **Event Code:** 0x0E, **Umask:** 1110, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_MULTIWAY.TAKEN.WRONG_TARGET

- **Title:** Incorrect Target Predictions on Taken Multiway Bundles, **Category:** Branch
- **Definition:** BRANCH_MULTIWAY.TAKEN.WRONG_TARGET should equal BRANCH_MULTIWAY.ALL_PATHS.WRONG_TARGET, since only multiway branch bundles where at least one branch instruction is taken actually specify a target
- **Event Code:** 0x0E, **Umask:** 1111, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.ALL.NT_OUTCOMES_CORRECTLY_PREDICTED

- **Title:** Correct Not-Taken Predicate Predictions, **Category:** Branch
- **Definition:** BRANCH_PATH.ALL.NT_OUTCOMES_CORRECTLY_PREDICTED counts the number of correct not-taken predicate predictions on not-taken branches, independent of predictor
- **Event Code:** 0x0F, **Umask:** 0010, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.ALL.TK_OUTCOMES_CORRECTLY_PREDICTED

- **Title:** Correct Taken Predicate Predictions, **Category:** Branch
- **Definition:** BRANCH_PATH.ALL.TK_OUTCOMES_CORRECTLY_PREDICTED counts the number of correct taken predicate predictions on taken branches, independent of predictor. Only the predicate must be correct; resteers to incorrect targets are also counted by this monitor as long as the branch is actually taken
- **Event Code:** 0x0F, **Umask:** 0011, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.ALL.NT_OUTCOMES_INCORRECTLY_PREDICTED

- **Title:** Incorrect Taken Predicate Predictions, **Category:** Branch
- **Definition:** BRANCH_PATH.ALL.NT_OUTCOMES_INCORRECTLY_PREDICTED counts the number of incorrect taken predicate predictions on not-taken branches, independent of predictor
- **Event Code:** 0x0F, **Umask:** 0000, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.ALL.TK_OUTCOMES_INCORRECTLY_PREDICTED

- **Title:** Incorrect Not-Taken Predicate Predictions, **Category:** Branch
- **Definition:** BRANCH_PATH.ALL.TK_OUTCOMES_INCORRECTLY_PREDICTED counts the number of incorrect not-taken predicate predictions on taken branches, independent of predictor
- **Event Code:** 0x0F, **Umask:** 0001, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.1ST_STAGE.NT_OUTCOMES_CORRECTLY_PREDICTED

- **Title:** Correct Not-Taken Predicate Predictions made in the first pipeline stage,

  Category: Branch
- **Definition:** BRANCH_PATH.1ST_STAGE.NT_OUTCOMES_CORRECTLY_PREDICTED should always count zero, as the TAR is the only predictor in the first stage of the core pipeline and it only makes taken predictions
- **Event Code:** 0x0F, **Umask:** 0110, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.1ST_STAGE.TK_OUTCOMES_CORRECTLY_PREDICTED

- **Title:** Correct Taken Predicate Predictions made in the first pipeline stage, **Category:**

  Branch
- **Definition:** BRANCH_PATH.1ST_STAGE.TK_OUTCOMES_CORRECTLY_PREDICTED counts the number of correct taken predicate predictions on taken branches made by the TAR in the first stage of the core pipeline. Only the predicate must be correct; resteers to incorrect targets are also counted by this monitor as long as the branch is actually taken. There are 0 bubbles between the branch and its predicted target
- **Event Code:** 0x0F, **Umask:** 0111, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.1ST_STAGE.NT_OUTCOMES_INCORRECTLY_PREDICTED

- **Title:** Incorrect Taken Predicate Predictions made in the first pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PATH.1ST_STAGE.NT_OUTCOMES_INCORRECTLY_PREDICTED counts the number of incorrect taken predicate predictions on not-taken branches, made by the TAR in the first stage of the core pipeline
- **Event Code:** 0x0F, **Umask:** 0100, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.1ST_STAGE.TK_OUTCOMES_INCORRECTLY_PREDICTED

- **Title:** Incorrect Taken Predicate Predictions made in the first pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PATH.1ST_STAGE.TK_OUTCOMES_INCORRECTLY_PREDICTED should always count zero, as the TAR is the only predictor in the first stage of the core pipeline and it only makes taken predictions
- **Event Code:** 0x0F, **Umask:** 0101, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.2ND_STAGE.NT_OUTCOMES_CORRECTLY_PREDICTED

- **Title:** Correct Taken Predicate Predictions made in the second pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PATH.2ND_STAGE.NT_OUTCOMES_CORRECTLY_PREDICTED counts the number of correct not-taken predicate predictions on not-taken branches made by the BPT/MBPT in the second stage of the core pipeline
- **Event Code:** 0x0F, **Umask:** 1010, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.2ND_STAGE.TK_OUTCOMES_CORRECTLY_PREDICTED

- **Title:** Correct Taken Predicate Predictions made in the second pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PATH.2ND_STAGE.TK_OUTCOMES_CORRECTLY_PREDICTED counts the number of correct taken predicate predictions on taken branches by the BPT/MBPT or the TAC in the second stage of the core pipeline. Only the predicate must be correct; resteers to incorrect targets are also counted by this monitor as long as the branch is actually taken. There is 1 bubble between the branch and its predicted target
- **Event Code:** 0x0F, **Umask:** 1011, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.2ND_STAGE.NT_OUTCOMES_INCORRECTLY_PREDICTED

- **Title: Incorrect Taken Predicate Predictions made in the second pipeline stage Category:** Branch
- **Definition:** BRANCH_PATH.2ND_STAGE.NT_OUTCOMES_INCORRECTLY_PREDICTED counts the number of incorrect taken predicate predictions on not-taken branches made by the BPT/MBPT or the TAC in the second stage of the core pipeline
- **Event Code:** 0x0F, **Umask:** 1000, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.2ND_STAGE.TK_OUTCOMES_INCORRECTLY_PREDICTED

- **Title:** Incorrect Not-Taken Predicate Predictions made in the second pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PATH.2ND_STAGE.TK_OUTCOMES_INCORRECTLY_PREDICTED counts the number of incorrect not-taken predicate predictions on taken branches made by the BPT/MBPT in the second stage of the core pipeline
- **Event Code:** 0x0F, **Umask:** 1001, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.3RD_STAGE.NT_OUTCOMES_CORRECTLY_PREDICTED

- **Title:** Correct Not-Taken Predicate Predictions made in the third pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PATH.3RD_STAGE.NT_OUTCOMES_CORRECTLY_PREDICTED counts the number of correct not-taken predicate predictions on not-taken branches made by the BAC in the third stage of the core pipeline, including overrides of TAR taken predictions (made in the first stage) on the last instances of loop-closing branches
- **Event Code:** 0x0F, **Umask:** 1110, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.3RD_STAGE.TK_OUTCOMES_CORRECTLY_PREDICTED

- **Title:** Correct Taken Predicate Predictions made in the third pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PATH.3RD_STAGE.TK_OUTCOMES_CORRECTLY_PREDICTED counts the number of correct taken predicate predictions on taken branches made by the BAC in the third stage of the core pipeline. Only the predicate must be correct; resteers to incorrect targets are also counted by this monitor as long as the branch is actually taken. There are 2 bubbles between the branch and its predicted target (or 3, if the target must be computed for a branch syllable in slot 0 or 1)
- **Event Code:** 0x0F, **Umask:** 1111, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.3RD_STAGE.NT_OUTCOMES_INCORRECTLY_PREDICTED

- **Title:** Incorrect Taken Predicate Predictions made in the third pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PATH.3RD_STAGE.NT_OUTCOMES_INCORRECTLY_PREDICTED counts the number of incorrect taken predicate predictions on not-taken branches made by the BAC in the third stage of the core pipeline
- **Event Code:** 0x0F, **Umask:** 1100, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PATH.3RD_STAGE.TK_OUTCOMES_INCORRECTLY_PREDICTED

- **Title:** Incorrect Not-Taken Predicate Predictions made in the third pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PATH.3RD_STAGE.TK_OUTCOMES_INCORRECTLY_PREDICTED counts the number of incorrect not-taken predicate predictions on taken branches made by the BAC in the third stage of the core pipeline, including overrides of TAR taken predictions (made in the first stage) on the last instances of loop-closing branches
- **Event Code:** 0x0F, **Umask:** 1101, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.ALL.ALL_PREDICTIONS

- **Title:** All Branch Predictions, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.ALL.ALL_PREDICTIONS counts all branch predictions, which take place in the front-end of the processor. Note that this number does not necessarily equal the total number of branch instructions in the code, as branch predictions are made on a bundle basis (i.e., there is only one prediction per multiway branch bundle)
- **Event Code:** 0x10, **Umask:** 0000, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.ALL.CORRECT_PREDICTIONS

- **Title:** Correct Branch Predictions by All Predictors, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.ALL.CORRECT_PREDICTIONS counts all branch predictions that do not necessitate a back-end branch misprediction flush, independent of predictor. A mismatch between the predicted and actual values of the branch predicate or target results in a branch misprediction. Return branches must additionally predict privilege level and previous function state
- **Event Code:** 0x10, **Umask:** 0001, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.ALL.WRONG_PATH

- **Title:** Incorrect Predicate Predictions by All Predictors, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.ALL.WRONG_PATH counts branch mispredictions that result from a mismatch of the predicted and actual values of the branch predicate, independent of predictor
- **Event Code:** 0x10, **Umask:** 0010, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.ALL.WRONG_TARGET

- **Title:** Incorrect Target Predictions by All Predictors, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.ALL.WRONG_TARGET counts branch mispredictions that result from a mismatch of the predicted and actual values of the branch target, independent of predictor
- **Event Code:** 0x10, **Umask:** 0011, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.1ST_STAGE.ALL_PREDICTIONS

- **Title:** All Branch Predictions made in the first pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.1ST_STAGE.ALL_PREDICTIONS counts the number of branch predictions made in the first stage of the core pipeline by the TAR. The TAR is the only predictor operating in that stage of the pipeline and it only makes taken predictions. The PLP in the third stage may override a TAR predicate prediction on a loop-closing branch. The prediction flow is as follows:

```
if (TAR Hit)
   monitor++
   Read Target from TAR
```

- **Event Code:** 0x10, **Umask:** 0100, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.1ST_STAGE.CORRECT_PREDICTIONS

- **Title:** Correct Branch Predictions made in the first pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.1ST_STAGE.CORRECT_PREDICTIONS counts the number of branches correctly predicted taken by the TAR, both in predicate and target
- **Event Code:** 0x10, **Umask:** 0101, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.1ST_STAGE.WRONG_PATH

- **Title:** Incorrect Predicate Predictions made in the first pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.1ST_STAGE.WRONG_PATH counts the number of actually not-taken branches predicted by the TAR (excluding overrides by the PLP)
- **Event Code:** 0x10, **Umask:** 0110, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.1ST_STAGE.WRONG_TARGET

- **Title:** Incorrect Target Predictions made in the first pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.1ST_STAGE.WRONG_TARGET counts the number of taken branches that were resteered to an incorrect target by the TAR
- **Event Code:** 0x10, **Umask:** 0111, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.2ND_STAGE.ALL_PREDICTIONS

- **Title:** All Branch Predictions in the second pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.2ND_STAGE.ALL_PREDICTIONS counts the number of branch predictions made in the second stage of the core pipeline. The following structures operate in that stage: BPT and MBPT (for predicates), TAC and RSB (for targets). Predictions are made in the second stage only if no predictions were made during the first stage. Any prediction made in this stage will be counted, except when a taken predicate prediction is made by the BPT/MBPT on a non-return branch and no target is available from the TAC. The branch prediction structures interact in the following manner:

```
if ((BPT Hit) or (MBPT Hit))
    if (Predicted Taken)
        if (Predicted Return Branch)
            monitor++
            Read Target from RSB
        else
            if (TAC Hit)
                monitor++
                Read Target from TAC
            else
                Get Target from BAC in the 3rd Stage
    else
        monitor++
        Follow Sequential Path
else

    if (TAC Hit)
        monitor++
        Read Target from TAC
    else
        Follow Sequential Path
```

- **Event Code:** 0x10, **Umask:** 1000, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.2ND_STAGE.CORRECT_PREDICTIONS

- **Title:** Correct Branch Predictions made in the second pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.2ND_STAGE.CORRECT_PREDICTIONS counts the number of correct predicate predictions made by the BPT/MBPT or the TAC in the second stage of the core pipeline. If the predicate prediction is taken, the correct target must be provided during that stage by the RSB or the TAC. Correct taken predicate predictions made by the BPT/MBPT on non-return branches that miss the TAC require the BAC to provide a target in the third stage and are not counted by this monitor
- **Event Code:** 0x10, **Umask:** 1001, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.2ND_STAGE.WRONG_PATH

- **Title:** Incorrect Predicate Predictions made in the second pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.2ND_STAGE.WRONG_PATH counts the number of incorrect not-taken predicate predictions made in the second stage of the core pipeline, and the number of incorrect taken predicate predictions made in that stage if a target was also provided
- **Event Code:** 0x10, **Umask:** 1010, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.2ND_STAGE.WRONG_TARGET

- **Title:** Incorrect Target Predictions made in the second pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.2ND_STAGE.WRONG_TARGET counts the number of branches that were correctly predicted taken by the BPT/MBPT or TAC, but were resteered to an incorrect target by the RSB or the TAC
- **Event Code:** 0x10, **Umask:** 1011, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.3RD_STAGE.ALL_PREDICTIONS

- **Title:** All Branch Predictions made in the third pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.3RD_STAGE.ALL_PREDICTIONS counts the number of branch predictions made in the third stage of the core pipeline by the BAC. The BAC can make both predicate predictions (based on the whether hint field of the branch) and target predictions, in the following manner:

```
if (TAR Hit)
    if (Predicted Last Instance of Loop-Closing Branch)
        monitor++
        PLP Override of TAR Taken Prediction
        Resteer Frontend to Sequential Address
else
    if ((BPT Hit) or (MBPT Hit))
        if (Predicted Taken)
            if (not (TAC Hit))
                if (not (Predicted Return Branch))
                    monitor++
                    Compute Target
    else
        if (not (TAC Hit))
            monitor++
            Read Whether Hint Field for Predicate Prediction
            if (Predicted Taken)
                Read BType Field for Type Information
                if (Indirect Branch)
                    Read Target from RSB
                else
                    Compute Target
            else
                Follow Sequential Path
```

- **Event Code:** 0x10, **Umask:** 1100, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.3RD_STAGE.CORRECT_PREDICTIONS

- **Title:** Correct Branch Predictions made in the third pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.3RD_STAGE.CORRECT_PREDICTIONS counts the number of correct branch predictions made by the BAC, including target predictions of branches whose predicate was supplied by a different predictor. For predicted-taken branches, both predicate and target must be correct
- **Event Code:** 0x10, **Umask:** 1101, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.3RD_STAGE.WRONG_PATH

- **Title:** Incorrect Predicate Predictions made in the third pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.3RD_STAGE.WRONG_PATH counts branches whose predicate was incorrectly predicted by the BAC (based on the whether hint field of the branch), and not-taken branches whose taken predicate prediction by another predictor caused the BAC to supply a target
- **Event Code:** 0x10, **Umask:** 1110, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_PREDICTOR.3RD_STAGE.WRONG_TARGET

- **Title:** Incorrect Target Predictions made in the third pipeline stage, **Category:** Branch
- **Definition:** BRANCH_PREDICTOR.3RD_STAGE.WRONG_TARGET counts taken branches that were correctly predicted taken by any predictor, but whose target was incorrectly supplied by the BAC
- **Event Code:** 0x10, **Umask:** 1111, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

BRANCH_TAKEN_SLOT

- **Title:** Taken Branch Detail, **Category:** Branch
- **Definition:** BRANCH_TAKEN_SLOT monitors which slot number in a branch bundle (single-way or multiway) a taken branch occupies, or records that there were no taken branches in the given branch bundle. Use this monitor behind the downstream opcode matcher, rather than IA64_TAGGED_INST_RETIRED, to count dynamic br.calls and br.rets.
- **Event Code:** 0x0D, **Umask:** See below, **PMC/PMD:** 4,5,6,7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

  The SLOT_MASK unit mask defined by Table 7-29 allows profiling of taken branches based on their instruction slot number. If multiple bits are set in the SLOT_MASK, all the set cases are included in the event count. The processor uses the following equation to determine the event outcome in each cycle:

```
    (PMC.umask{16}
       and (branch in slot 0 is taken))
or (PMC.umask{17}
    and (branch in slot 0 is NOT taken)
    and (branch in slot 1 is taken))
or  (PMC.umask{18}
    and (branch in slot 0 is NOT taken)
    and (branch in slot 1 is NOT taken)
    and (branch in slot 2 is taken))
or  (PMC.umask{19}
    and (branch in slot 0 is NOT taken)
    and (branch in slot 1 is NOT taken)
    and (branch in slot 2 is NOT taken))
```

Table 7-29. Slot unit mask for BRANCH_TAKEN_SLOT

SLOT_MASK	PMC.umask {19:16}	Description
Instruction Slot 0	xxx1	Count if branch in slot 0 is first taken branch
Instruction Slot 1	xx1x	Count if branch in slot 1 is first taken branch
Instruction Slot 2	x1xx	Count if branch in slot 2 is first taken branch
No taken branch	1xxx	Count if NO branch was taken

BUS_ALL

- **Title:** Bus Transactions **Category:** Frontside Bus
- **Definition:** BUS_ALL counts all transactions issued on the bus. These include BRL, BRIL, BIL, BWL, BRP, BWP, IORD, IOWR, and the other transactions.
- **Event Code:** 0x47, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_BRQ_LIVE_REQ_LO and BUS_BRQ_LIVE_REQ_HI

- **Title:** BRQ Live Requests, **Category:** Frontside Bus
- **Definition:** BUS_BRQ_LIVE_REQ counts the number of live entries in the bus request queue (BRQ). These events include L3 cache reads, BRL, BRIL, BRP, and IORD memory transactions. The count excludes cache line write backs, partial writes (BWP and IOWR) and write coalescing read for ownership transactions, since these have their own write queue. This performance monitor increments its count each core clock (not bus clock).
- **Event Code:** 0x5c (HI), 0x5b (LO), **Umask:** Ignored, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 2 (each)
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

  Two hardware events are needed to count this:

  BUS_BRQ_LIVE_REQ_HI - counts the two most significant bit of the 4-bit outstanding BRQ request count

  BUS_BRQ_LIVE_REQ_LO - counts the two least significant bit of the 4-bit outstanding BRQ request count

BUS_BRQ_READ_REQ_INSERTED

- **Title:** BRQ Requests Inserted **Category:** Frontside Bus
- **Definition:** BUS_BRQ_READ_REQ_INSERTED counts the number of reads (BRL) and read for ownership (BRIL) requests that are inserted into the BRQ. The count excludes cache line write backs, partial and coalescing writes, since these have their own write queue.
- **Event Code:** 0x5d, **Umask:** Ignored, **PMC/PMD:**4, 5, 6, 7**Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

  BRQ inserts can be used to directly measure combined far cache/BUS latencies as follows:

  avg_brq_req_outstanding_per_cycle = (BUS_BRQ_LIVE_REQ/delta(cycles))

  avg_brq_latency = (BUS_BRQ_LIVE_REQ / BUS_BRQ_READ_REQ_INSERTED)

  The only caveat is that the tracked BRQ inserts holds read and read for ownership, but not write coalescing write backs.

BUS_BURST

- **Title:** Bus Burst Transactions **Category:** Frontside Bus
- **Definition:** BUS_BURST counts the number of full cache line (burst mode) bus memory transactions. These include BRL, BRIL, and BWL transactions.
- **Event Code:** 0x49, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_HITM

- **Title:** Bus Hit Modified Line Transactions **Category:** Frontside Bus
- **Definition:** BUS_HITM counts the number of memory transactions which caused HITM to be asserted. The following memory transactions are included in the performance monitor: BRL, BWL, BRIL, and BIL. Only events originated by this processor are counted.
- **Event Code:** 0x44, **Umask:** Ignored, **PMC/PMD:**4, 5, 6, 7**Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_IO

- **Title:** IA-32 Compatible I/O Bus Transactions **Category:** Frontside Bus
- **Definition:** BUS_IO counts the number of I/O transactions. These include either IORD or IOWR transactions.
- **Event Code:** 0x50, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

Note: only the “Any” and “Self” unit masks are supported.

BUS_IOQ_LIVE_REQ_LO and BUS_IOQ_LIVE_REQ_HI

- **Title:** In-Order Bus Queue Results, **Category:** Frontside Bus
- **Definition:** BUS_IOQ_LIVE_REQ counts the number of live bus requests in the in order bus queue. This performance monitor increments its count each core clock (not bus clock).
- **Event Code:** 0x58 (HI), 0x57 (LO), **Umask:** Ignored, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 3 (each)
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

  BUS_IOQ_LIVE_REQ can then be computed as BUS_IOQ_LIVE_REQ_HI*4 + BUS_IOQ_LIVE_REQ_LO

  Two hardware events are needed to count this:

  BUS_IOQ_LIVE_REQ_HI - counts the two most significant bit write backs of the 4-bit outstanding IOQ request count

  BUS_IOQ_LIVE_REQ_LO - counts the two least significant bits of the 4-bit outstanding IOQ request count

BUS_LOCK

- **Title:** IA-32 Compatible Bus Lock Transactions **Category:** Frontside Bus
- **Definition:** BUS_LOCK counts the number of IA-32 compatible bus lock transactions.
- **Event Code:** 0x53, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

Note: Only the “Any” unit mask is supported.

BUS_LOCK_CYCLES

- **Title:** IA-32 Compatible Bus Lock Cycles **Category:** Frontside Bus
- **Definition:** BUS_LOCK_CYCLES counts the number of bus clocks that the bus is locked due to IA-32 compatible bus lock transactions.
- **Event Code:** 0x54, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

Note: Only the “Any” unit mask is supported.

BUS_MEMORY

- **Title:** Bus Memory Transactions **Category:** Frontside Bus
- **Definition:** BUS_MEMORY counts the number of bus memory transactions. These include BRL, BRIL, BIL, BWL, BRP, and BWP transactions.
- **Event Code:** 0x4a, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_PARTIAL

- **Title:** Bus Partial Transactions **Category:** Frontside Bus
- **Definition:** BUS_PARTIAL counts the number of partial bus memory transactions. These include BRP and BWP transactions.
- **Event Code:** 0x48, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_RD_ALL

- **Title:** Bus Read Transactions **Category:** Frontside Bus
- **Definition:** BUS_RD_ALL counts the number of BRL memory transactions. These include both code and data BRL transactions.
- **Event Code:** 0x4b, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_RD_DATA

- **Title:** Bus Read Data Transactions **Category:** Frontside Bus
- **Definition:** BUS_RD_DATA counts the number of BRL data transactions.
- **Event Code:** 0x4c, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_RD_HIT

- **Title:** Bus Read Hit Clean Non-local Cache Transactions **Category:** Frontside Bus
- **Definition:** BUS_RD_HIT counts the number of BRL memory transactions which caused HIT to be asserted. Only events originated by this processor are counted.
- **Event Code:** 0x40, **Umask:** Ignored, **PMC/PMD:**4, 5, 6, 7**Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_RD_HITM

- **Title:** Bus Read Hit Modified Non-local Cache Transactions **Category:** Frontside Bus
- **Definition:** BUS_RD_HITM counts the number of BRL memory transactions which caused HITM to be asserted. Only events originated by this processor are counted.
- **Event Code:** 0x41, **Umask:** Ignored, **PMC/PMD:**4, 5, 6, 7**Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_RD_INVAL

- **Title:** Bus Read Invalidated Line **Category:** Frontside Bus
- **Definition:** BUS_RD_INVAL counts the number of BIL memory transactions. On Itanium processors, these transactions are only generated from flush cache instructions.
- **Event Code:** 0x4e, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_RD_INVAL_BST

- **Title:** Bus BRIL Burst Transactions **Category:** Frontside Bus
- **Definition:** BUS_RD_INVAL counts the number of BRIL memory transactions. These transactions are typically generated from memory stores, RFO (read for ownership) events.
- **Event Code:** 0x4f, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_RD_INVAL_HITM

- **Title:** Bus BIL Transaction Results in HITM**Category:** Frontside Bus
- **Definition:** BUS_RD_INVAL_HITM counts the number of BIL transactions which caused HITM to be asserted.Only events originated by this processor are counted.
- **Event Code:** 0x42, **Umask:** Ignored, **PMC/PMD:**4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_RD_INVAL_BST_HITM

- **Title:** Bus BRIL Burst Transaction Results in HITM **Category:** Frontside Bus
- **Definition:** BUS_RD_INVAL_BST_HITM counts the number of BRIL transactions which caused HITM to be asserted. Only events originated by this processor are counted.
- **Event Code:** 0x43, **Umask:** Ignored, **PMC/PMD:**4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_RD_IO

- **Title:** IA-32 Compatible I/O Read Transactions **Category:** Frontside Bus
- **Definition:** BUS_RD_IO counts the number of IORD transactions.
- **Event Code:** 0x51, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

Note: Only the “Any” and “Self” unit masks are supported.

BUS_RD_PRTL

- **Title:** Bus Read Partial Transactions **Category:** Frontside Bus
- **Definition:** BUS_RD_PRTL counts the number of partial read memory transactions. These include BRP transactions.
- **Event Code:** 0x4d, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_SNOOPS

- **Title:** Bus Snoops Total **Category:** Frontside Bus
- **Definition:** BUS_SNOOPS counts the number of internal snoops generated from bus memory transactions.
- **Event Code:** 0x46, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

Note: Only the “Any” unit mask is supported. “Any” counts the number of internal snoops generated from all bus transactions.

BUS_SNOOPS_HITM

- **Title:** Bus Snoops Hit Modified Cache Line **Category:** Frontside Bus
- **Definition:** BUS_SNOOPS_HITM counts the number of internal snoops (generated from bus memory transactions) which hit a modified line in the local processor.
- **Event Code:** 0x45, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

Note: Only the “Any” mask is supported. “Any” counts the number of internal snoops, generated from all transactions, which hit a modified line.

BUS_SNOOP_STALL_CYCLES

- **Title:** Bus Snoop Stall Cycles **Category:** Frontside Bus
- **Definition:** BUS_SNOOP_STALL_CYCLES counts the number of bus clocks that the bus is stalled due to snoop stalls.
- **Event Code:** 0x55, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

Note: Only “Self” and “Any” unit masks are supported. “Self” counts the number of snoop stalls generated due to memory transactions initiated by the local processor. “Any” counts all snoop stalls (those generated due to memory transactions initiated by the local processor, other processors, and the priority agent).

BUS_SNOOPQ_REQ

- **Title:** Bus Snoop Queue Requests, **Category**: Frontside Bus
- **Definition:** BUS_SNOOPQ_REQ counts the number of outstanding memory transactions that have not completed the snoop phase. This performance monitor increments its count each core clock (not bus clock). BUS_SNOOPQ_REQ is not equivalent to the number of valid entries in the snoop queue. This is due to the fact that entries can stay in the snoop queue beyond the snoop phase (e.g. for implicit write backs).
- **Event Code:** 0x56, **Umask:** Ignored, **PMC/PMD:**4, 5, **Max. Increment/Cycle:** 3
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

BUS_WR_WB

- **Title:** Bus Write Back Transactions **Category:** Frontside Bus
- **Definition:** BUS_WR_WB counts the number of BWL memory transactions. These transactions are generated from either explicit write backs or coalescing writes. Currently, these will count BWL (if snoops are disabled).
- **Event Code:** 0x52, **Umask:** See Section 7.6.5, **PMC/PMD:**4, 5, 6, 7

  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

CPU_CPL_CHANGES

- **Title:** Privilege level changes, **Category:** System
- **Definition:** CPU_CPL_CHANGES counts the number of privilege level changes
- **Event Code:** 0x34, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

CPU_CYCLES

- **Title:** CPU Cycles, **Category:** System
- **Definition:** CPU_CYCLES counts elapsed processor cycles
- **Event Code:** 0x12, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

DATA_ACCESS_CYCLE

- **Title:** Data Access Stall Cycles, **Category:** Stall
- **Definition:** DATA_ACCESS_CYCLE counts the number of cycles that the pipeline is stalled or flushed due to instructions waiting for data on cache misses, L1D way mispredictions, and DTC misses.
- **Event Code:** 0x03, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

DATA_EAR_EVENTS

- **Title:** L1 Data Cache EAR Events, **Category:** L1 Data Cache
- **Definition:** DATA_EAR_EVENTS counts the number of data cache or DTLB events captured by the Data Cache Unit Event Address Register
- **Event Code:** 0x67, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

DATA_REFERENCES_RETIRED

- **Title:** Retired Data Memory References, **Category:** L1 Data Cache
- **Definition:** DATA_REFERENCES_RETIRED counts the number of data memory references retired by the processor memory pipeline. The count includes check loads, uncacheable accesses, RSE operations, VHPT memory references, semaphores, and FP memory references. Predicated off operations are excluded
- **Event Code:** 0x63, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: yes

DEPENDENCY_ALL_CYCLE

- **Title:** Scoreboard Dependency and Dispersal Break Cycles, **Category:** Stall
- **Definition:** DEPENDENCY_ALL_CYCLE counts the number of cycles attributable to data (scoreboard) dependency on integer or FP operations (not counting cache/memory access), or issue-limit stalls (e.g., implicit and explicit stops). Floating-point flushes and delays due to control and application register reads and writes are factored in as well.
- **Event Code:** 0x06, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

DEPENDENCY_SCOREBOARD_CYCLE

- **Title:** Scoreboard Dependency Cycles, **Category:** Stall
- **Definition:** DEPENDENCY_SCOREBOARD_CYCLE counts the number of cycles attributable to data (scoreboard) dependency on integer or FP operations (not counting cache/memory access). Floating-point flushes and delays due to control and application register reads and writes are factored in as well.
- **Event Code:** 0x02, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

DTC_MISSES

- **Title:** DTC Misses, **Category:** System
- **Definition:** DTC_MISSES counts the number of DTC misses for data requests
- **Event Code:** 0x60, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

DTLB_INSERTS_HPW

- **Title:** Hardware Page Walker Inserts into the DTLB, **Category:** System
- **Definition:** DTLB_INSERTS_HPW counts the number of DTLB inserts completed by the hardware page table walker
- **Event Code:** 0x62, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

DTLB_MISSES

- **Title:** DTLB Misses, **Category:** System
- **Definition:** DTLB_MISSES counts the number of DTLB misses for demand requests
- **Event Code:** 0x61, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

EXPL_STOPS_DISPERSED

- **Title:** Explicit Stops Dispersed, **Category:** Instruction Issue
- **Definition:** EXPL_STOPS_DISPERSED counts the number of explicit programmer-specified stops, including those encountered during hardware speculative wrong-path execution
- **Event Code:** 0x2E, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

FP_OPS_RETIRED_HI

- **Title:** FP Operations Retired (High), **Category:** Execution
- **Definition:** FP_OPS_RETIRED_HI and FP_OPS_RETIRED_LO together compute the derived event FP_OPS_RETIRED.d which is the weighted sum of retired FP operations
- **Event Code:** 0x0A, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 3
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

  FP_OPS_RETIRED.d, a derived value, is computed as FP_OPS_RETIRED_HI * 4 + FP_OPS_RETIRED_LO. Weights for individual FP ops: `fnorm`=1, `fadd`=1, `fmpy=1`, `fma`=2, `fms`=2, `fsub`=1, `fpma`=4, `fpmpy`=4, `fpms`=4, `fnma`=2, `frcpa`=1, `frsqrta`=1, `fpnma`=4, `fprcpa`=2, `fprsqrta`=2, `xma`=0

Note: Integer multiply instructions (xma) are not counted as floating-point operations (even though they are executed in the floating-point multiplier).

FP_OPS_RETIRED_LO

- **Title:** FP Operations Retired (Low), **Category:** Execution
- **Definition:** FP_OPS_RETIRED_HI and FP_OPS_RETIRED_LO together compute the derived event FP_OPS_RETIRED.d which is the weighted sum of retired FP operations
- **Event Code:** 0x09, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 3
- **Qualification:** See FP_OPS_RETIRED_HI on page 91

FP_FLUSH_TO_ZERO

- **Title:** FP Result Flushed to Zero, **Category:** Execution
- **Definition:** FP_FLUSH_TO_ZERO counts the number of times a near zero result is flushed to zero in FTZ mode. Parallel FP operations which cause one or both results to flush to zero will increment the event count only by one (i.e. even if both results are flushed to zero)
- **Event Code:** 0x0B, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

FP_SIR_FLUSH

- **Title:** FP SIR Flushes, **Category:** Execution
- **Definition:** FP_SIR_FLUSH counts the number of times a Safe Instruction Recognition (SIR) flush occurs
- **Event Code:** 0x0C, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

IA32_INST_RETIRED

- **Title:** Retired IA-32 Instructions, **Category:** System
- **Definition:** IA32_INST_RETIRED counts the number of IA-32 instructions retired
- **Event Code:** 0x15, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

IA64_INST_RETIRED

- **Title:** Retired Itanium Instructions, **Category:** Execution
- **Definition:** IA64_INST_RETIRED counts all retired Itanium instructions. The count includes predicated on and off instructions, NOPs, but excludes hardware-inserted RSE operations. This event is equal to IA64_TAGGED_INST_RETIRED with a zero unit mask
- **Event Code:** 0x08, **Umask:** 0000, **PMC/PMD:** 4, 5 **Max. Increment/Cycle:** 6
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

IA64_TAGGED_INST_RETIRED

- **Title:** Retired Tagged Itanium Instructions**Category:** Execution
- **Definition:** IA64_TAGGED_INST_RETIRED is analogous to IA64_INST_RETIRED, except that it further qualifies event selection with the instruction address range and opcode match settings in the IBR and PMC registers
- **Event Code:** 0x08**Umask:**See below**PMC/PMD:**4, 5**Max. Increment/Cycle:**6
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

  The TAG_SELECT unit mask defined in Table 7-30 always qualifies the event count of IA64_TAGGED_INST_RETIRED with either the opcode match register PMC_8 or PMC_9. Note that the setting of PMC_8 qualifies all down-stream event monitors. To ensure that other monitored events are counted independent of the opcode matcher, all mifb and all mask bits of PMC_8 should be set to one (all opcodes match). The settings of PMC9 do not affect other event monitors.

Also, note that umask 0011 is distinct in that it also counts, in addition to instructions matched by the appropriate opode matcher, architecturally invisible RSE fills and spills when the parent instruction (such as an alloc or br.ret) causing them is matched by the combination in PMC8. Thus, the difference in counts obtained between using PMC8 and PMC9 as opcode matchers is the amount of RSE activity.

Table 7-30. Retired Event Selection by Opcode Match

TAG_SELECT	PMC.umask {19:16}	Description
PMC_8 tag	0011	Instruction tagged by opcode matcher PMC_8
PMC_9 tag	0010	Instruction tagged by opcode matcher PMC_9
All	0000	All retired instructions (regardless of whether they were tagged or not)
Undefined	All other umask settings	Undefined event count

INST_ACCESS_CYCLE

- **Title:** Instruction Access Cycles, **Category:** Stall
- **Definition:** INST_ACCESS_CYCLE counts the number of cycles where there are no back-end stalls or flushes, the decoupling buffer is empty, and the front-end is stalled waiting on an L1I or ITLB miss.
- **Event Code:** 0x01, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

INST_DISPERSED

- **Title:** Instructions Dispersed, **Category:** Instruction Issue
- **Definition:** INST_DISPERSED counts the number of instructions dispersed (including nops) from the front-end to the back-end of the machine. The count includes instruction dispersal on the wrong execution path; i.e., in the shadow of a branch misprediction flush or other back-end flush
- **Event Code:** 0x2D, **Umask:** Ignored, **PMC/PMD:** 4, 5 **Max. Increment/Cycle:** 6
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

INST_FAILED_CHKS_RETIRED.ALL

- **Title:** Failed Speculative Check Loads, **Category:** Execution
- **Definition:** INST_FAILED_CHKS_RETIRED.ALL counts the number of failed speculative check load instructions (`chk.s`). The count excludes predicated off `chk.s` instructions and includes both integer and FP variants
- **Event Code:** 0x35, **Umask:** xx11, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

INST_FAILED_CHKS_RETIRED.FP

- **Title:** Failed Speculative FP Check Loads, **Category:** Execution
- **Definition:** INST_FAILED_CHKS_RETIRED.FP counts the number of failed speculative check load instructions (`chk.s`). The count excludes predicated off `chk.s` instructions and includes only FP variants
- **Event Code:** 0x35, **Umask:** xx10, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no

INST_FAILED_CHKS_RETIRED.INTEGER

- **Title:** Failed Speculative Integer Check Loads, **Category:** Execution
- **Definition:** INST_FAILED_CHKS_RETIRED.INTEGER counts the number of failed speculative check load instructions (`chk.s`). The count excludes predicated off `chk.s` instructions and includes only integer variants
- **Event Code:** 0x35, **Umask:** xx01, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: no
- **Qualification:**

INSTRUCTION_EAR_EVENTS

- **Title:** Instruction EAR Events, **Category:** Instruction Cache
- **Definition:** INSTRUCTION_EAR_EVENTS counts the number of EAR captures for L1I and ITLB events
- **Event Code:** 0x23, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

ISA_TRANSITIONS

- **Title:** Itanium ISA to IA-32 ISA Transitions, **Category:** System
- **Definition:** ISA_TRANSITIONS counts the number of instruction set transitions from Itanium ISA to IA-32. This is the number of times the PSR.is bit toggles from 0 to 1 due to `br.ia` or `rfi` to IA-32 code
- **Event Code:** 0x14, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

ISB_LINES_IN

- **Title:** Instruction Streaming Buffer Lines In, **Category:** Instruction Cache
- **Definition:** ISB_LINES_IN counts the number of 32-byte L1I cache lines written from L2 (and beyond) into the Instruction Streaming Buffer as a consequence of instruction demand miss and instruction prefetch requests
- **Event Code:** 0x26, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

ITLB_INSERTS_HPW

- **Title:** Hardware Page Walker Inserts into the ITLB, **Category:** System
- **Definition:** ITLB_INSERTS_HPW counts the number of ITLB inserts done by the hardware page table walker
- **Event Code:** 0x28, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

ITLB_MISSES_FETCH

- **Title:** ITLB Demand Misses, **Category:** System
- **Definition:** ITLB_MISSES_FETCH counts the number of demand ITLB misses
- **Event Code:** 0x27, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

L1D_READ_FORCED_MISSES_RETIRED

- **Title:** L1 Data Cache Forced Load Misses, **Category:** L1 Data Cache
- **Definition:** L1D_READ_FORCED_MISSES_RETIRED counts the number of loads that were forced to miss the L1 data cache due to memory ordering constraints, predicted L1 data cache misses, Store Buffer hits, or simultaneous L2 data returns to the register file
- **Event Code:** 0x6B, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: yes

L1D_READ_MISSES_RETIRED

- **Title:** L1 Data Cache Read Misses, **Category:** L1 Data Cache
- **Definition:** L1D_READ_MISSES_RETIRED counts the number of committed L1 data cache read misses. The count includes any read reference that could have been serviced by the L1 data cache (see L1D_READS_RETIRED event for a detailed list) but missed the cache. False misses are included in the event count. Since the L1 data cache is write-through, write misses are NOT counted
- **Event Code:** 0x66, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: yes

L1D_READS_RETIRED

- **Title:** L1 Data Cache Reads, **Category:** L1 Data Cache
- **Definition:** L1D_READS_RETIRED counts the number of committed L1 data cache reads (integer and RSE references). Excluded from the count are VHPT loads, check loads, L1 hinted loads, semaphores, uncacheable and FP loads. Predicated-off loads are also excluded, but wrong-path operations are included in the count
- **Event Code:** 0x64, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: yes

L1I_DEMAND_READS

- **Title:** L1I and ISB Instruction Demand Lookups, **Category:** Instruction Cache
- **Definition:** L1I_DEMAND_READS counts the number of 32-byte instruction demand L1I/ISB lookups, independent of the hit/miss outcome
- **Event Code:** 0x20, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

  Qualifications based on instruction address range may be inaccurate

L1I_FILLS

- **Title:** L1 Instruction Cache Fills, **Category:** Instruction Cache
- **Definition:** L1I_FILLS counts the number of 32-byte lines moved from the Instruction Streaming Buffer into the L1 instruction cache
- **Event Code:** 0x21, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L1I_PREFETCH_READS

- **Title:** L1I and ISB Instruction Prefetch Lookups, **Category:** Instruction Cache
- **Definition:** L1I_PREFETCH_READS counts the number of 64-byte instruction prefetch L1I/ISB lookups, independent of the hit/miss outcome.
- **Event Code:** 0x24, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

L2_DATA_REFERENCES.ALL

- **Title:** L2 Data Read and Write References, **Category:** L2 Cache
- **Definition:** L2_DATA_REFERENCES.ALL counts all L2 data read and write accesses.The reported count is the number of requests prior to cache line merging. Semaphore operations are counted as one read and one write
- **Event Code:** 0x69, **Umask:** xx11, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: yes

L2_DATA_REFERENCES.READS

- **Title:** L2 Data Read References, **Category:** L2 Cache
- **Definition:** L2_DATA_REFERENCES.READS counts all L2 data read accesses. The reported count is the number of requests prior to cache line merging. Semaphore operations are counted as one read
- **Event Code:** 0x69, **Umask:** xx01, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: yes

L2_DATA_REFERENCES.WRITES

- **Title:** L2 Data Write References, **Category:** L2 Cache
- **Definition:** L2_DATA_REFERENCES.WRITES counts all L2 data write accesses. The reported count is the number of requests prior to cache line merging. Semaphore operations are counted as one write
- **Event Code:** 0x69, **Umask:** xx10, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode matching: yes, Data Address Range: yes

L2_FLUSH_DETAILS

- **Title:** L2 Flush Details, **Category:** L2 Cache
- **Definition:** L2_FLUSH_DETAILS allows a detailed breakdown of L2 pipeline flushes by cause. This event counts the number of L2 pipeline flushes constrained by the conditions specified in the 4-bit unit mask defined by Table 7-31 on page 98. All combinations of the four unit mask bits are supported
- **Event Code:** 0x77, **Umask:See below, PMC/PMD:** 4, 5, 6, 7, **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

Table 7-31. Unit Mask Bits {19:16} for L2_FLUSH_DETAILS Event

L2 Flush Reason	PMC.umask {19:16}	Description
L2_ST_BUFFER_FLUSH	xxx1	L2 store to store conflict due to (a) Same store buffer entry (b) Back to back stores
L2_ADDR_CONFLICT	xx1x	L2 flushed due to MESI update on load follows store
L2_BUS_REJECT	x1xx	L2 flushed due to bus constraints
L2_FULL_FLUSH	1xxx	L2 flushed due to one of: (a) Store buffer full (b) Load miss buffer full

L2_FLUSHES

- **Title:** L2 Flushes, **Category:** L2 Cache
- **Definition:** L2_FLUSHES counts the number of L2 pipeline flushes due to Store Buffer conflicts, address conflicts, full L3 and bus queues, and other such reasons
- **Event Code:** 0x76, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

L2_INST_DEMAND_READS

- **Title:** L2 Instruction Demand Fetch Requests, **Category:** Instruction Cache
- **Definition:** L2_INST_DEMAND_READS counts the number of L2 instruction requests due to L1I demand fetch misses. The monitor counts the number of demand fetch look-ups that miss in both the L1I and the ISB, regardless of whether they hit or miss in the Request Address Buffer (RAB); i.e., the count includes misses to a line that has already been requested (secondary misses)
- **Event Code:** 0x22, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

L2_INST_PREFETCH_READS

- **Title:** L2 Instruction Prefetch Requests, **Category:** Instruction Cache
- **Definition:** L2_INST_PREFETCH_READS counts all instruction prefetch requests issued to the unified L2 cache
- **Event Code:** 0x25, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

L2_MISSES

- **Title:** L2 Misses, **Category:** L2 Cache
- **Definition:** L2_MISSES counts the number of L2 cache misses (requests to uncacheable pages are excluded). The count includes misses caused by instruction fetch and prefetch, and data read and write operations. Secondary misses to the same L2 cache line will be counted as individual misses
- **Event Code:** 0x6A, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

L2_REFERENCES

- **Title:** L2 References, **Category:** L2 Cache
- **Definition:** L2_REFERENCES counts the number of L2 cache references (requests to uncacheable pages are excluded). The count includes references by instruction fetch and prefetch, and data reads and writes. The maximum per-cycle increment is three: one instruction fetch and two data references
- **Event Code:** 0x68, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 3
- **Qualification:** Instruction Address Range: yes, Opcode matching: no, Data Address Range: no

L3_LINES_REPLACED

- **Title:** L3 Cache Lines Replaced, **Category:** L3 Cache
- **Definition:** L3_LINES_REPLACED counts the number of valid L3 lines that have been victimized
- **Event Code:** 0x7F, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_MISSES

- **Title:** L3 Misses, **Category:** L3 Cache
- **Definition:** L3_MISSES counts the number of L3 misses. The number includes misses caused by both instruction and data requests and L2 line writebacks
- **Event Code:** 0x7C, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_READS.ALL_READS.ALL

- **Title:** Instruction and Data L3 Reads, **Category:** L3 Cache
- **Definition:** L3_READS.ALL_READS.ALL counts the number of all L3 read accesses, independent of the stream source (instruction or data) and the hit/miss outcome
- **Event Code:** 0x7D, **Umask:** 1111, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_READS.ALL_READS.HIT

- **Title:** Instruction and Data L3 Read Hits, **Category:** L3 Cache
- **Definition:** L3_READS.ALL_READS.HIT counts the number of all L3 read hits, independent of the stream source (instruction or data)
- **Event Code:** 0x7D, **Umask:** 1101, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_READS.ALL_READS.MISS

- **Title:** Instruction and Data L3 Read Misses, **Category:** L3 Cache
- **Definition:** L3_READS.ALL_READS.MISS counts the number of all L3 read misses, independent of the stream source (instruction or data)
- **Event Code:** 0x7D, **Umask:** 1110, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_READS.DATA_READS.ALL

- **Title:** Data L3 Reads, **Category:** L3 Cache
- **Definition:** L3_READS.DATA_READS.ALL counts the number of data L3 read accesses, independent of the hit/miss outcome
- **Event Code:** 0x7D, **Umask:** 1011, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_READS.DATA_READS.HIT

- **Title:** Data L3 Read Hits, **Category:** L3 Cache
- **Definition:** L3_READS.DATA_READS.HIT counts the number of data L3 read hits
- **Event Code:** 0x7D, **Umask:** 1001, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_READS.DATA_READS.MISS

- **Title:** Data L3 Read Misses, **Category:** L3 Cache
- **Definition:** L3_READS.DATA_READS.MISS counts the number of data L3 read misses
- **Event Code:** 0x7D, **Umask:** 1010, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_READS.INST_READS.ALL

- **Title:** Instruction L3 Reads, **Category:** L3 Cache
- **Definition:** L3_READS.INST_READS.ALL counts the number of instruction L3 read accesses, independent of the hit/miss outcome
- **Event Code:** 0x7D, **Umask:** 0111, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_READS.INST_READS.HIT

- **Title:** Instruction L3 Read Hits, **Category:** L3 Cache
- **Definition:** L3_READS.INST_READS.HIT counts the number of instruction L3 read hits
- **Event Code:** 0x7D, **Umask:** 0101, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_READS.INST_READS.MISS

- **Title:** Instruction L3 Read Misses, **Category:** L3 Cache
- **Definition:** L3_READS.INST_READS.MISS counts the number of instruction L3 read misses
- **Event Code:** 0x7D, **Umask:** 0110, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_REFERENCES

- **Title:** L3 References, **Category:** L3 Cache
- **Definition:** L3_REFERENCES counts the number of L3 cache references (requests to uncacheable pages are excluded). The count includes references by instruction fetch and prefetch, data reads and writes, and L2 cache line most significant bit writebacks.
- **Event Code:** 0x7B, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_WRITES.ALL_WRITES.ALL

- **Title:** L3 Writes, **Category:** L3 Cache
- **Definition:** L3_WRITES.ALL_WRITES.ALL counts the number of L3 write accesses independent of the hit/miss outcome. The count includes both data writes and L2 write-back accesses (including L3 read for ownership requests that satisfy stores)
- **Event Code:** 0x7E, **Umask:** 1111, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_WRITES.ALL_WRITES.HIT

- **Title:** L3 Write Hits, **Category:** L3 Cache
- **Definition:** L3_WRITES.ALL_WRITES.HIT counts the number of L3 write hits. The count includes both data writes and L2 writeback accesses (including L3 read for ownership requests that satisfy stores)
- **Event Code:** 0x7E, **Umask:** 1101, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_WRITES.ALL_WRITES.MISS

- **Title:** L3 Write Misses, **Category:** L3 Cache
- **Definition:** L3_WRITES.ALL_WRITES.MISS counts the number of L3 write misses. The count includes both data writes and L2 writeback accesses (including L3 read for ownership requests that satisfy stores)
- **Event Code:** 0x7E, **Umask:** 1110, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_WRITES.L2_WRITEBACK.ALL

- **Title:** L3 Writebacks, **Category:** L3 Cache
- **Definition:** L3_WRITES.L2_WRITEBACK.ALL counts the number of L3 write accesses that result from L2 writebacks, independent of hit/miss outcome
- **Event Code:** 0x7E, **Umask:** 1011, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_WRITES.L2_WRITEBACK.HIT

- **Title:** L3 Writeback Hits, **Category:** L3 Cache
- **Definition:** L3_WRITES.L2_WRITEBACK.HIT counts the number of L3 write hits that result from L2 writebacks
- **Event Code:** 0x7E, **Umask:** 1001, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_WRITES.L2_WRITEBACK.MISS

- **Title:** L3 Writeback Misses, **Category:** L3 Cache
- **Definition:** L3_WRITES.L2_WRITEBACK.MISS counts the number of L3 write misses that result from L2 writebacks
- **Event Code:** 0x7E, **Umask:** 1010, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_WRITES.DATA_WRITES.ALL

- **Title:** L3 Data Writes, **Category:** L3 Cache
- **Definition:** L3_WRITES.DATA_WRITES.ALL counts the number of L3 data write accesses independent of the hit/miss outcome
- **Event Code:** 0x7E, **Umask:** 0111, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_WRITES.DATA_WRITES.HIT

- **Title:** L3 Data Write Hits, **Category:** L3 Cache
- **Definition:** L3_WRITES.DATA_WRITES.HIT counts the number of L3 data write hits
- **Event Code:** 0x7E, **Umask:** 0101, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

L3_WRITES.DATA_WRITES.MISS

- **Title:** L3 Data Write Misses, **Category:** L3 Cache
- **Definition:** L3_WRITES.DATA_WRITES.MISS counts the number of L3 data write misses
- **Event Code:** 0x7E, **Umask:** 0110, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode matching: no, Data Address Range: no

LOADS_RETIRED

- **Title:** Retired Loads, **Category:** Memory
- **Definition:** LOADS_RETIRED counts the number of retired loads. The count includes integer, FP, RSE, VHPT, uncacheable loads and failed check loads (`ld.c`). Check loads that hit in the ALAT are *not* counted. Predicated-off operations are not counted
- **Event Code:** 0x6C, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: yes

MEMORY_CYCLE

- **Title:** Combined Memory Stall Cycles, **Category:** Stall
- **Definition:** MEMORY_CYCLE counts the number of cycles that the pipeline is stalled or flushed due to instructions waiting for data on cache misses, L1D way mispredictions, DTC misses, and RSE traffic.
- **Event Code:** 0x07, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

MISALIGNED_LOADS_RETIRED

- **Title:** Retired Unaligned Load Instructions, **Category:** Memory
- **Definition:** MISALIGNED_LOADS_RETIRED counts the number of retired unaligned loads that the hardware handled. The count includes integer, FP, and failed check loads (`ld.c`). Check loads that hit in the ALAT are *not* counted. Predicated-off operations are not counted
- **Event Code:** 0x70, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: yes

MISALIGNED_STORES_RETIRED

- **Title:** Retired Unaligned Store Instructions, **Category:** Memory
- **Definition:** MISALIGNED_STORES_RETIRED counts the number of retired unaligned store instructions that the hardware handled. The count includes integer, FP, and uncacheable stores. Predicated-off operations are not counted
- **Event Code:** 0x71, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: yes

NOPS_RETIRED

- **Title:** Retired Nop Instructions, **Category:** Execution
- **Definition:** NOPS_RETIRED counts the number of retired nop.i, nop.m or nop.b instructions. The count excludes predicated off nop instructions
- **Event Code:** 0x30, **Umask:** Ignored, **PMC/PMD:** 4, 5 **Max. Increment/Cycle:** 6
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

PIPELINE_ALL_FLUSH_CYCLE

- Title: Combination of Pipeline Flush Cycles caused by either a front-end or a back-end source, **Category**: Stall
- **Definition:** PIPELINE_ALL_FLUSH_CYCLE, for a given cycle, either counts the number of cycles spent during a front-end resteer of the pipeline (due to a correctly predicted taken branch), or counts the number of cycles spent during certain back-end resteers (due to a branch misprediction, ALAT flush or exception/serialization flush). This monitor does not count DTC flushes, way mispredictions, or floating-point flushes.
- **Event Code:** 0x04, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

PIPELINE_BACKEND_FLUSH_CYCLE

- **Title:** Combination of Pipeline Flush Cycles caused by either a Branch Misprediction or an Exception**Category:** Stall
- **Definition:** PIPELINE_BACKEND_FLUSH_CYCLE counts the number of cycles spent during back-end resteers of the pipeline (due to a branch misprediction, ALAT flush or exception/serialization flush). This monitor does not count DTC flushes, way mispredictions, or floating-point flushes.
- **Event Code:** 0x00, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

PIPELINE_FLUSH

- **Title:** Pipeline Flush, **Category:** System
- **Definition:** PIPELINE_FLUSH counts how often the Itanium processor pipeline is flushed due to IEU bypass conflict (caused by non-unit latency MMX operations such as variable shifts), data translation cache miss, L1 data cache way mispredict or other reasons such as an exception flush or an instruction serialization. Combinations of different flush reasons may be chosen by appropriately setting the umask. The monitor does not include branch misprediction flushes
- **Event Code:** 0x33, **Umask:** See below, **PMC/PMD:** 4, 5, 6, 7
  Max. Increment/Cycle: 1
- **Qualification:** Instruction Address Range: no, Opcode Matching: no, Data Address Range: no

Table 7-32. Unit Mask Bits {19:18} for PIPELINE_FLUSH Event

FLUSH_TYPE	PMC.umask {19:16}	Description
IEU_FLUSH	1xxx	IEU bypass flush
DTC_FLUSH	x1xx	Data Translation Cache Miss flush
L1D_WAYMP_FLUSH	xx1x	L1 Way Misprediction flush
OTHER_FLUSH	xxx1	Other flush reason: exception flush or an instruction serialization.

PREDICATE_SQUASHED_RETIRED

- **Title:** Instructions Squashed Due to Predicate Off, **Category:** Execution
- **Definition:** PREDICATE_SQUASHED_RETIRED counts the number of instructions squashed due to a false qualifying predicate. The count includes all predicated off nops except nop.b's. Predicated off B-syllables (including nop.b) are not counted
- **Event Code:** 0x31, **Umask:** Ignored, **PMC/PMD:** 4, 5 **Max. Increment/Cycle:** 6
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: no

RSE_LOADS_RETIRED

- **Title:** RSE Load Accesses, **Category:** Execution
- **Definition:** RSE_LOADS_RETIRED counts the number of retired RSE loads
- **Event Code:** 0x72, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Refer to RSE_REFERENCES_RETIRED on page 107

RSE_REFERENCES_RETIRED

- **Title:** RSE Accesses, **Category:** Execution
- **Definition:** RSE_REFERENCES_RETIRED counts the number of retired RSE loads and stores
- **Event Code:** 0x65, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: yes

  RSE loads and stores are considered tagged if the `alloc`, `loadrs`, `flushrs` or branch return or `rfi` that caused the RSE references was tagged by the instruction address range or the opcode matcher. For data address range checking, the RSE reference is tagged only if its hits the programmed DBR range

STORES_RETIRED

- **Title:** Retired Stores, **Category:** Memory
- **Definition:** STORES_RETIRED counts the number of retired stores. The count includes integer, FP, RSE, and uncacheable stores. Predicated-off operations are not counted
- **Event Code:** 0x6D, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: yes

UC_LOADS_RETIRED

- **Title:** Retired Uncacheable Loads, **Category:** Memory
- **Definition:** UC_LOADS_RETIRED counts the number of retired uncacheable or write coalescing loads. The count includes integer, FP, RSE, and VHPT loads and failed check loads (ld.c). Check loads that hit in the ALAT are NOT counted. Predicated-off operations are not counted
- **Event Code:** 0x6E, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: yes

UC_STORES_RETIRED

- **Title:** Retired Uncacheable Stores, **Category:** Memory
- **Definition:** UC_STORES_RETIRED counts the number of retired uncacheable or write coalescing stores.The count includes integer, FP, RSE, and uncacheable stores. Predicated-off operations are not counted
- **Event Code:** 0x6F, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 2
- **Qualification:** Instruction Address Range: yes, Opcode Matching: yes, Data Address Range: yes

UNSTALLED_BACKEND_CYCLE

- **Title:** Unstalled Back-end Cycles**Category:** Stall
- **Definition:** UNSTALLED_BACKEND_CYCLE counts the number of cycles that the back-end is processing instructions without delay and the decoupling buffer between the front-end and back-end is empty, so that any effect on the front-end will be propagated to the back-end of the pipeline. This monitor thus reflects the number of cycles where there are no back-end stalls or flushes, and the decoupling buffer is empty, regardless of whether the L1I and ITLB are being hit or missed.
- **Event Code:** 0x05, **Umask:** Ignored, **PMC/PMD:** 4, 5, 6, 7 **Max. Increment/Cycle:** 1

Instruction Address Range: no, Opcode matching: no, Data Address Range: no

Model Specific Behavior for IA-32 Instruction Execution 8

The Itanium processor is capable of executing IA-32 instructions in the IA-32 system environment (legacy lA-32 operating systems) provided the required platform and firmware support exists in the system. The Itanium processor is also capable of executing IA-32 instructions in the Itanium system environment (Itanium-based operating system). Itanium-based operating system support for the capability of running IA-32 applications is defined by the respective operating system vendor. For more details on IA-32 instruction execution on Itanium-based OS, please refer to Volume 1, Chapter 6 and Volume 2, Chapter 10 of the *Intel® Itanium™ Architecture Software Developer's Manual*.

Note that while Itanium processor supports execution of IA-32 applications, best performance and capabilities will be realized by using 64-bit optimized OSes and applications.

In general, the behavior of IA-32 instructions on the Itanium processor is similar to that of the Pentium III processor except where noted. The following sections describe some of the key differences in behavior between IA-32 instruction execution on an Itanium processor and on the Pentium III processor. These differences do not prevent IA-32 legacy operating systems or IA-32 applications from operating correctly.

8.1 Processor Reset and Initialization

When RESET# is asserted, all processors based on the Itanium architecture boot at a different reset location than IA-32 processors and start executing Itanium-based 64-bit code instead of IA-32 16-bit Real Mode code. Unlike IA-32 processors, processors based on the Itanium architecture execute PAL firmware to test and initialize the processor and then continue execution in the Itanium instruction set to boot the system. SAL firmware code can switch to the IA-32 instruction set as needed to execute IA-32 BIOS code. For more details on processor reset, please refer to Chapter 11 and Chapter 13 of Volume 2 of the *Intel® Itanium™ Architecture Software Developer's Manual*.

8.2 New JMPE Instruction

A new IA-32 instruction JMPE has been defined for processors based on the Itanium architecture. This instruction comes in two forms with an opcode for each. These opcodes will cause an Invalid Opcode fault on all IA-32 processors. For more details, refer to Chapter 1 of Volume 3 of the *Intel® Itanium™ Architecture Software Developer's Manual*.

8.3 System Management Mode (SMM)

SMM is superseded by the Itanium-based Platform Management definition. This mechanism is designed to provide platform level interrupt support for both IA-32 and Itanium-based operating systems. Please refer to Chapter 11 of Volume 2 of the *Intel® Itanium™ Architecture Software Developer's Manual* for more details on PMI.

The IA-32 SMM and I/O Port Restart feature is not supported on the Itanium processor. Dynamically, powering off/on I/O devices on an I/O Port reference via system logic is not possible for IA-32 Operating Systems or Itanium-based Operating Systems using the IA-32 SMM I/O Restart mechanism. I/O Restart has not been extended on processors based on the Itanium architecture to intercept I/O Port references from the Itanium instruction set via normal loads and stores on processors based on the Itanium architecture.

Execution of the IA-32 RSM (Resume from SMM) instruction results an Invalid Opcode fault on all processors based on the Itanium architecture.

8.4 CPUID Instruction Return Values for Caches and TLBs of the Intel® Itanium™ Processor

The following table provides information on how to decode return values of the CPUID instruction for the Itanium processor's internal caches and TLBs.

Table 8-1. Encoding of Cache and TLB Return Values for the Intel® Itanium™ Processor

Return Value	Cache or TLB Description
0x10	L0D: 16K 4-way set associative 32 bytes line
0x15	L0I: 16K 4-way set associative 32 bytes line
0x1A	L1: 96K on die 6-way set associative 64 byte line
0x88	L2: 2M 4-way set associative 64 bytes line
0x89	L2: 4M 4-way set associative 64 bytes line
0x8A	L2: 8M 4-way set associative 64 bytes line
0x90	ITLB: 4K to 256M pages, fully associative, 64 entries
0x96	DTLB0: 4K to 256M pages, fully associative, 32 entries
0x9B	DTLB1: 4K to 256M pages, fully associative, 96 entries

When the input value in register EAX is 2, the Itanium processor returns information about the processor's internal caches and TLBs in the EAX, EBX, ECX, and EDX registers. The following table describes the values returned.

Table 8-2. EAX, EBX, ECX, and EDX Return Values for the Intel® Itanium™ Processor

Register	Return Value (from MSB to LSB)
EAX	0x00, 0x15, 0x10, 0x01
EBX	0x00, 0x00, <L2>, 0x1A (<L2> is either 0x88, 0x89)
ECX	0x00, 0x9B, 0x96, 0x90
EDX	0x80, 0x00, 0x00, 0x00

8.5 Machine Check Abort (MCA)

The Itanium processor supports Pentium processor level machine checks in the IA-32 System Environment.

8.6 Model Specific Registers

The complete set of Model Specific Registers (MSRs) found on the Pentium III processor is not supported on the Itanium processor. For example, Model Specific Debug registers, Model Specific Test registers, Machine Check registers, and Model Specific Configuration registers are not supported.

Model Specific registers that are common to the Itanium processor and Pentium III processor use the Pentium III processor's bit definition and register assignment. The ITC, APIC_Base, MTRR and MAP registers are supported on the Itanium processor.

8.7 Cache Modes

Pentium processor and Pentium III processor SRAM Cache Mode is not supported on the Itanium processor.

SRAM is typically used on IA-32 processors to provide scratch RAM areas while running IA-32 boot and machine check code before memory is available. Both of these functions are now provided by Itanium-based firmware while running IA-32 and Itanium-based operating systems.

8.8 10-byte Floating-point Operand Reads and Writes

Many IA-32 FP instructions read and write 10 bytes to memory. Consider the case of 16-bit segment, where the read or write starts at offset 0xFFF8. Pentium III processor reads or writes 8 bytes then re-evaluates the linear address before reading or writing the final 2 bytes. Eight bytes are accessed at 0xfff8, and 2 bytes are accessed at 0x0000.

The Itanium processor evaluates the address once, then accesses all 10 bytes. Therefore, bytes 0xfff8 to 0x10001 will be accessed.

On a 10-byte operand read or write access, potential page faults and GP faults will return slightly different faulting addresses (linear addresses may wrap differently).

8.9 Floating-point Data Segment State

The Itanium processor reports a different value of the floating-point data segment state (FDS) after the execution of “FNOP” instruction (or any FP instruction that does not perform a memory reference). The contents of the data register are undefined if the prior non-control instruction did not have a memory operand. The Pentium III processor behaves as follows:

1. A FP non-transparent instruction which references memory will put the selector of the data segment used in the memory reference into FDS.
2. A FP non-transparent instruction which doesn’t reference memory will put the selector of SS into FDS and 0 into FEA.

If a segment override prefix is present on an instruction of the type specified in case 2, the overriding segment selector will be put into FDS instead of the selector of SS.

The Itanium processor behavior covers only case #1 described above. Note that this difference does not affect the running of IA-32 applications.

8.10 Writes to Reserved Bits during FXSAVE

During FXSAVE, the Itanium processor does not write any reserved bits, while the Pentium III processor may write reserved bits. The Itanium processor does one 10 byte access to save each FP register, whereas the Pentium III processor will do two 8 byte accesses causing writes to upper reserved bits.

8.11 Setting the Access/Dirty (A/D) Bit on Accesses that Cross a Page Boundary

In the IA-32 system environment, the Itanium processor sets a page's A/D bit even if a memory reference crosses a page boundary and the other page has a fault. This behavior is different from Pentium III processors which do not modify the A/D bit under the above conditions.

The above difference does not come into play in the Itanium system environment.

8.12 Enhanced Floating-point Instruction Accuracy

On the Itanium processor, FP transcendental instructions will return more accurate (hence slightly different) answers than Pentium III processor. This behavior falls into 3 categories:

- **F2XM1, FYL2X, FYL2XP1, FPATAN Instructions**
  More accurate algorithms will result in answers which may differ from Pentium III processor

by 1 **u**nit in the **l**ast **p**lace (ulp). Also, for FYL2X and FYL2XP1, when x or x+1 respectively is a power of two, the Precision exception is not signaled (since log(2^k) where, k is integral, is exact).

- **FPTAN, FSIN, FCOS, FSINCOS Instruction**s
  New algorithms on Itanium processor include a more accurate argument reduction scheme. Although more accurate, the algorithms implemented on Itanium processor can produce answers which are different from those returned on Pentium III processor.
- **FPREM, FPREM1 Instructions**
  No change.

8.13 RCPSS, RCPPS, RSQRTSS, RSQRTPS Instruction Differences

These four instructions are single and parallel approximations of divide and square root operations. The Itanium processor will calculate these functions to a higher accuracy than previous implementations. resulting in different answers. The Pentium III processor implementation of one of these functions can have a maximum relative error of $1.5 * 2^{-12}$. The Itanium processor, however, will calculate RCPPS/RCPSS functions with a maximum relative error of $2^{-17.75288} \sim = 1.1868 * 2^{-18}$ and the RSQRTPS/RSQRTSS functions with a maximum relative error of $2^{-17.06412} \sim = 1.9130 * 2^{-18}$.

8.14 Read/Write Access Ordering

In general, the order of reads/writes within any complex IA-32 instruction is model specific even among IA-32 processors. Different Intel processors have different access ordering behavior; for example, internal operation ordering varies between the 80486, Pentium, Pentium III and Itanium processors.

8.15 Multiple IOAPIC Redirection Table Entries

If multiple IOAPIC Redirection Table Entries (RTE) share the same vector, and at least one RTE is programmed as logical delivery mode in which the selected local APIC destinations overlap with the other RTEs with the same vector, some of the selected local APICs might not receive the interrupt when the pins that correspond to these RTEs are asserted.

8.16 Self Modifying Code (SMC)

The Itanium processor provides the same SMC support as the Pentium processor. Also, a branch instruction is required between the store that modifies instruction(s) and the modified code.

8.17 Raising an Alignment Check (AC) Fault

The Pentium III processor checks and raises AC fault before a page fault. The Itanium processor checks and raise a page fault before an AC fault.

8.18 Maximum Number of Processors Supported in MP System Running Legacy IA-32 OS (IA-32 System Environment)

Similar to the case of IA-32 processors in an MP system, the maximum number of processors based on the Itanium architecture supported in a MP system running legacy IA-32 OS (IA-32 system environment) is 16. However, in MP systems with IA-32 processors, the number of IA-32 processors can be extended beyond 16 with additional platform enhancements while the limit for the number of processors based on the Itanium architecture running IA-32 OS in a MP system is limited to 16.

Index

Entries in this index are described by the volume number and page or range of pages where the entries can be found. The volume number appears to the left of the colon. The page or range of pages appears to the right of the colon. A range of pages is separated by a hyphen.

Numerics

A

B

C

D

E

F

G

H

I

J

L

M

N

O

P

Q

R

S

T

U

V

W

X

Z