CERN TIMING ON PXI AND cRIO PLATFORMS

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Abstract

Given the time critical applications, the use of PXI and cRIO platforms in the accelerator complex at CERN, require the integration into the CERN timing system. In this paper the present state of integration of both PXI and cRIO platforms in the present General Machine Timing system and the White Rabbit Timing system, which is its successor, is described. PXI is used for LHC collimator control and for the new generation of control systems for the kicker magnets on all CERN accelerators. The cRIO platform is being introduced for transient recording on the CERN electricity distribution system and has potential for applications in other domains, because of its real-time OS, FPGA backbone and hot swap modules. The further development intended and what types of applications are most suitable for each platform will be discussed.

INTRODUCTION

At CERN, the accelerator operation requires nanosecond precise timing for many systems that act on the particle beams, such as for injection, acceleration, focusing, measurement and extraction. These systems are synchronised and triggered using the General Machine Timing (GMT) [1] system, which has been custom designed at CERN. GMT electronic boards have been developed for a several bus systems, mainly VME and cPCI. At the time of choice in 2004, PXI and cRIO were not mature enough [2], however, during the last 5 years their success in a large variety of industrial areas [3,4], together with the steady improvement of the graphical system design tools [5] have made the PXI and cRIO platforms an interesting candidate for accelerator systems. But no GMT electronic boards fit in the PXI and cRIO bus systems and the C++ driver software for Linux was not compatible with the operating systems used on these platforms.

The successor of the GMT system [6], called White Rabbit, provides improved timing accuracy and solves most of the GMT's shortcomings, and is actively being developed at CERN. An IEEE standardisation committee has been set up to incorporate it into a new IEEE-1588 standard.

In this paper we describe the adaptation of the GMT to the PXI, the White Rabbit timing on the cRIO and how we envision the White Rabbit on the PXI, to enable CERN engineers and physicists to profit from advantages of industrial platform with CERN timing features.

GMT ON PXI

The CERN accelerator control standards for front-end systems are the VME and cPCI busses. Several equipment groups have chosen PXI, because of their instrumentation needs. However, to be able to use the CERN timing (GMT) a VME or cPCI had to be added to house the timing receiver and run the timing software. The generated triggers were then wired into the PXI either by copper or optical links. When one timing receiver could serve many PXI systems, such as for the collimator control [7], this small overhead is acceptable. For systems with a few PXI crates it would be an advantage if the timing card could be housed in the PXI crate.

For the hardware we use a GMT timing receiver card in PMC format [8] developed at CERN and a PMC carrier for PXI [9] from industry. This carrier is actually a cPCI carrier and therefore compatible with standard PXI crates and PXI Express crates with hybrid slots (PXI/PXIe) (see slot 5 in Fig. 1).

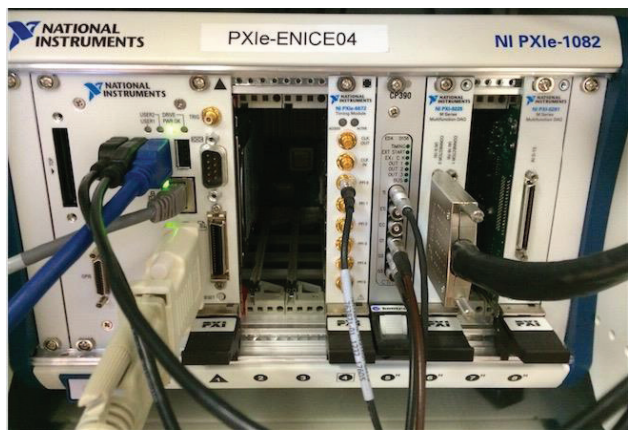

Figure 1: The GMT module installed in slot 5 of a PXI Express crate.

For the software we run a Hypervisor [10] on the PXI controller. This enabled us to run the existing timing library on Scientific Linux 6 on one core of the CPU and the LabVIEW RT system (Pharlap) on the other. In such a system the triggers generated by the GMT receiver were wired to a PXI trigger module that could provide bus triggers for commercial data acquisition cards in the rest of the PXI crate. The Hypervisor solution has also be used in other laboratories for the same purpose, such as in the Brazilian Synchrotron Light Laboratory (LNLS) [11] have used the Hypervisor to profit from the best features of two different operating systems.

WHITE RABBIT ON cRIO

The White Rabbit (WR) node is an open hardware design, accessible from CERN's open hardware repository [12]. Engineers at University of Zürich have used the WR design to build a C-series module for the cRIO platform [13], using the Module Development Kit of National Instruments. They adapted the module on FPGA code and wrote a driver in LabVIEW FPGA for the control and readout of the WR time stamp.

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The creators of the cRIO-WR module have made their design available in the open hardware repository on CERN's request [14]. We have had a series of 10 modules produced by a company that had previous WR module manufacturing experience [15].

During the testing we have optimised the LabVIEW FPGA driver code for minimum delay and jitter. Figure 2 shows the cRIO-WR test setup.

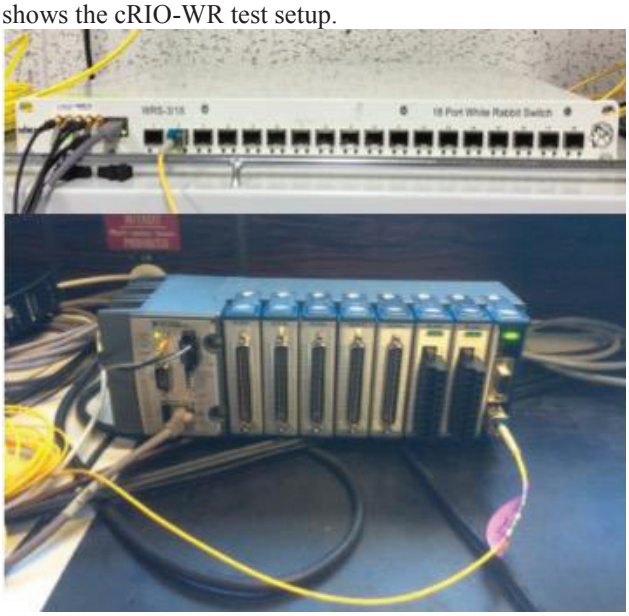

Figure 2: The test setup with the cRIO-WR module connected with the yellow fibre to the WR switch on top.

WHITE RABBIT ON PXI

A White Rabbit PXI Express module has not been manufactured yet, but preparatory work has been done and National Instruments has participated to a plugfest at the ISPCS 2015 conference [16]. National Instruments is one of the main players in the IEEE-1588 High Accuracy standardisation committee with the objective to complement the White Rabbit protocol with several other features. Once this standard has been agreed, I expect to see IEEE-1588 HA "White Rabbit" timing modules on PXIe. Such modules will be able to generate star triggers on the PXIe bus from a WR trigger, which will simultaneously trigger all modules in a crate to a high accuracy (< 0.5 ns skew).

CONCLUSION & FUTURE DEVELOPMENTS

CERN accelerator timing (GMT) modules have been custom designed for the VME, cPCI and PMC busses. This was done before the time PXI has become an interesting alternative. We have integrated the PMC version of the timing module by using a PMC carrier module for PXI and running the timing software on Scientific Linux 6 on a Hypervisor installed on a PXI controller. This allowed run the available Linux library and use all standard LabVIEW RT software and drivers on the same multi-core CPU.

We have profited from the open hardware design made by the University of Zürich of a White Rabbit timing module in cRIO. We have verified the design and had a series of modules produced using a WR partner company. This allowed us to test and optimise the FPGA driver to get optimum performance, which resulted in a minimum of 850 ns delay and 2 ns jitter.

CERN and National Instruments are two of the main players in the IEEE-1588 High Accuracy standardisation committee who's objective is to complement the White Rabbit protocol with several other features. Once this standard has been finalised, I expect to see IEEE-1588 HA "White Rabbit" timing modules on PXIe on the market.

Future developments point in the direction of having Linux RT on both cRIO and PXI platforms. For the new cRIO systems this is already the case and I expect to see Linux RT on PXI Express in the not too distant future. This operating system will allow the coexistence of commercial and open source software, which is what we have achieved with the Hypervisor, but a single OS will simplify the configuration, operation and maintenance of such systems and increase their performance.

We will pursue our objective of using commercial hardware for modules of which there is a large offer by multiple vendors and use custom designs for functions that are specific to CERN, where no commercial offer exists, or is mono vendor only.

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