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## **SVX', The New CDF Silicon Vertex Detector**

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# SVX', THE NEW CDF SILICON VERTEX DETECTOR

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## Abstract

The Collider Detector at Fermilab (CDF) radiation hardened silicon vertex detector (SVX') is described. The new detector has several improvements over its predecessor such as better signal to noise and higher efficiency. It's expected to have a radiation tolerance in excess of 1 Mrad. It has been taking data for several months and some preliminary results are shown.

## 1 Introduction

For Tevatron Collider run 1B a new silicon vertex detector (SVX') has been installed in the CDF detector to replace the SVX [1,2,3], the first silicon vertex detector to be successfully operated in a hadron collider environment. The new detector has the same overall configuration as the SVX; however several differences lead to significant improvements over its ancestor. For instance it is equipped with a radiation hard readout chip with higher gain [SVX IC, Rev H (SVXH3)] and it is AC coupled, so that radiation induced leakage currents will not saturate the input; it has lower noise (due mostly to the AC coupling), com-

plete  $\phi$  coverage and fewer dead strips.

## 2 Description of the SVX'

A complete description of the SVX detector can be found in refs [1,2]. The overall detector configuration remains unaltered for SVX' and is shown in Figure 1. We will emphasize the differences between the two detectors.

### 2.1 Geometry

SVX' modules (also referred to as *barrels*) consist of four layers of silicon strip detectors segmented into twelve 30 degrees wedges. Two such barrels are aligned along the beam direction with a gap between them of 2.15 cm at  $z=0$ . The basic detector element is called a *ladder* and is shown in Figure 2. There are 96 such elements in the complete detector. The geometry of the inner layer has been significantly changed in order to achieve complete  $\phi$  coverage. The *ladders* of the inner layer are tilted by 1 degree around their axes and they are overlapped at

the edges. A 0.17 degrees overlap is obtained for the SVX' corresponding to 0.24 strips whereas SVX had a 1.26 degrees gap. The inner layer is also closer to the beam line by  $\sim 1.5$  mm at a radius of 2.86 cm.

## 2.2 Front End Readout Chip

The front end readout circuit is the SVX chip Revision H (SVX was equipped with the SVX IC revision D [4,5]). It was fabricated in  $1.2 \mu\text{m}$  CMOS technology and the CMOS process was radiation hard. The chip is expected to tolerate more than 1 Mrad of radiation. The charge gain of the readout chip was determined by charge injection. Typical gains were around 21 mV/fC at the input capacitance typical of our detectors, which is approximately 30 pF for a full strip length of 25.5 cm.

## 2.3 Pedestal, Noise, Bad Channels

The silicon detectors used in the *ladder* construction are single-sided FOXFET biased and AC coupled [6]. The SVX was DC coupled and had to be operated in quadruple sample & hold mode in order to subtract the effect of varying strip to strip leakage currents. When the SVX chip is operated in quadruple sample & hold mode two successive charge integrations take place and the outgoing signal is the difference between the two integrated charges thus allowing a hardware subtraction of the leakage current contribution to the pedestals. The detector being AC coupled allows us to operate the SVX chip in double sample & hold mode with only one charge integration to determine the outgoing signal; this results in a noise which is lower by a factor  $\sqrt{2}$  compared to the SVX. Data taken without incident particles were analyzed to get the average pulse height (the pedestal) and standard deviation (the noise) of every channel. The noise was found by fitting a gaussian to the peak of the pulse height distribution. Typical values of the noise are around 1300 electrons (10.8 ADC counts) to be compared with a value of roughly 2200 electrons for SVX. Channels showing large deviations from the expected behavior (mostly higher noise) and channels that were skipped from the microbonding procedure because of the coupling capacitance being damaged or shorted correspond to only  $\simeq 1.7\%$  of the total to be compared with  $\simeq 2.9\%$  for SVX at the beginning of its operation. Another important improvement due to the AC coupling is the ability to operate the detector without saturating the SVXH3 readout chip preamp even when radiation damage to the silicon leads to a significant increase in leakage current for silicon strips. During its operation the SVX' is expected to receive a radiation dose of 60KRads. Measurements done on the SVX detector show a leakage current increase rate of 2.7 nA/Krad per strip for the inner layer. The SVXH3 preamp will saturate at 80 nA input current. Table 1 is a comparative summary of the features of SVX' and SVX.

## 3 Collider Data Analysis

Results reported in the following sections refer to the operation of the detector in CDF for the Tevatron Collider run 1B. Full event reconstruction using the latest version of the CDF offline was performed on samples of data from run 1B. Signal-to-noise ratio, hit efficiency, track quality, hit and impact parameter resolution measurements are preliminary.

### 3.1 Charge Collection

Clusters are defined as contiguous groups of strips whose pulse height,  $q$ , is greater than  $M$  times their noise,  $\sigma$ . We have chosen  $M = 4.0$  for one strip clusters,  $M = 2.5$  two strip clusters and  $M = 2.0$  for larger clusters; these were the same operational values used for the previous detector. Studies have been carried out both on cosmic ray data and collision data to reoptimize  $M$  for better hit efficiency and noise rejection and resulted in maintaining the previous values. The cluster position is defined as the charge centroid:  $x = \sum x_i q_i / \sum q_i$ . To select a clean sample of clusters, we require that they: a) belong to a four hit track reconstructed by the CDF tracking code [7,8], b) do not contain any bad channels. The resulting distribution (Figure 3) shows the most probable charge to be 155 ADC and a width of 23 ADC. Using the measured value of noise reported in section 2.3 we can quote a signal-to-noise ratio of about 15. Also shown in Figure 3 are the noise and signal values as measured in SVX.

### 3.2 Hit Efficiency

To determine the hit efficiency of a target layer, we select a sample of tracks having hits on three layers and look for a fourth hit in a window of  $\pm 10$  strips around the track intersection with the fourth layer. The efficiencies calculated in this way are 92.01% for the inner layer, 95.0% for the outer layer, 96.8% and 96.9% for the two internal layers. For all layers these numbers include inefficiencies due to the presence of microbonding regions (1.7% of the silicon region) between the three silicon crystals that make up a ladder as well as effects due to unusable channels (1.7% of the total number of channels) and effective detector inefficiency. The results for the inner and outer layers are additionally affected by geometric acceptance at  $z=0$  and at the edges of the detector. Figure 4 shows clearly the combination of these effects as a function of  $z$ . Comparing the expected inefficiency for the two internal layers due to microbonding regions and to unusable channels with the numbers quoted above, we find that the effective detector inefficiency is negligible (less than 1%).

### 3.3 Occupancy

The detector is operated in sparse mode to readout only channels whose signal content is above a hardware threshold; with this feature the readout time and data size are set by hit occupancy rather than total channel count. The value of the thresholds is optimized in order to provide minimum occupancy and 100% efficiency for half a MIP.

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The typical occupancy observed at these thresholds is 5%; peak values for occupancy (25%) are observed on one of the 12 sectors of the detector. After construction one of the ladders in that sector showed large deviations from the typical behaviour and in order to maintain the efficiency the thresholds on that sector had to be reoptimized, forcing an almost 100% occupancy on two out of eight ladders on that sector. It should be remarked that this solution doesn't cause signal loss. Typical values for occupancy in SVX were between 7% and 10%. The SVX chip is operated with a readout cycle of 2.1  $\mu$ s/channel for SVX' (was 2.7  $\mu$ s/channel for the SVX).

### 3.4 Position Resolution and Alignment

The position resolution of a target layer is evaluated using a sample of tracks having hits on the other layers; tracks are fitted using only these hits. We then plot the distribution of the distance of track intersections from reconstructed cluster centroids on a target layer (Figure 5). The mean of this residual distribution is used to evaluate the ladder alignment constants, while its width,  $\sigma_{res}$ , is related to the position resolution,  $\sigma_{pos}$ , by the equation:  $\sigma_{res}^2 = \sigma_{pos}^2 + \sigma_{fit}^2$ , where  $\sigma_{fit}$  is the contribution of the errors on fitted track parameters. For one, two and three strip clusters we find  $\sigma_{pos} = 13, 11, 16 \mu$ m. The alignment constants are used iteratively to correct for misalignments in  $z, \phi$  and radial direction, in respect to the nominal detector position. This alignment procedure has already produced significant improvements of track quality and resolution (Figures 5 and 6). When the alignment procedure is complete we expect a further improvement of the resolution values. A preliminary evaluation of the impact parameter resolution gives an asymptotic value  $\sigma_{impar} = 13 \mu$ m. In Figure 7 you can distinguish the contribution to the impact parameter resolution from multiple scattering at low Pt and from the intrinsic detector resolution at high Pt.

## 4 Conclusions

The new CDF silicon vertex detector is being operated at Fermilab for the Collider run 1B. The performance of the detector has been evaluated during several months of data taking. We measured a signal to noise of 15, a hit efficiency > 99%, an average position resolution of 11.6  $\mu$ m, and an asymptotic impact parameter resolution of 13  $\mu$ m.

### References

- [1] D. Amidei et al., *The CDF SVX: a Silicon Vertex Detector for a Hadron Collider*, NIM **A289** (1990), 388-399.
- [2] D. Amidei et al., *The Silicon Vertex Detector of the Collider Detector at Fermilab* FERMILAB-PUB-94/024-E. Submitted to NIM.
- [3] D. Amidei et al., *Status of Radiation Damage to the SVX*, CDF2061 (1993).

[4] S. A. Kleinfelder, IEEE Trans. Nucl. Sci. **35** (1988) 171.

[5] C. Haber et al., IEEE Trans. Nucl. Sci. **37** (1990) 1120.

[6] Manufactured by Micron Semiconductor LTD., 1 Royal Buildings, Marlborough Road, Churcill Ind. Estate, LANCING, SUSSEX BN15 8UN, ENGLAND.

[7] H. Wenzel, *Tracking in the SVX*, CDF1790 (1992).

[8] P. Derwent, *Changes to the SVX Tracking Package*, CDF2188 (1993).

### List of Figures

Fig.1: Isometric view of one barrel of the SVX'

Fig.2: Layer 2 ladder module

Fig.3: Pulse height distribution (ADC)

Fig.4: Inefficiency (distribution of missing hits in  $z$ )

Fig.5: Residuals for 2 and 3 strip clusters combined

Fig.6: Chi2 of reconstructed tracks

Fig.7: Impact parameter resolution ( $\sigma_{res}$  vs  $1/Pt$ )

Feature	SVX	SVX'
channels		46080
z coverage		51.1 cm
gap at $z=0$		2.15 cm
radius L0	3.0049 cm	2.8612 cm
radius L1		4.2560 cm
radius L2		5.6872 cm
radius L3		7.8658 cm
overlap L0	-1.26 deg (gap)	0.17 deg (0.24 strip)
overlap L1		0.32 deg (4 strip)
overlap L2		0.30 deg (4 strip)
overlap L3		0.04 deg (0 strip)
silicon		one-sided
passivation	DC	AC, FOXFET bias
atmosphere	none	polyimide
readout chip	Ar/Ethane+H20	dry nitrogen
sampling	SVX IC Rev.D	SVX IC Rev.H3
noise	quadruple	double
gain	2200 electrons	1300 electrons
reset/integrate	15 mv/fc	21 mv/fc
readout time		3.5 $\mu$ s
rad limit	2.7 $\mu$ s	2.1 $\mu$ s
bad channels	15-20 KRad	> 1 MRad
occupancy typical	2.93%	1.73%
occupancy max	7%-10%	5%
	12%-20%	25%

Table 1: Comparison of SVX and SVX'

FIG. 1

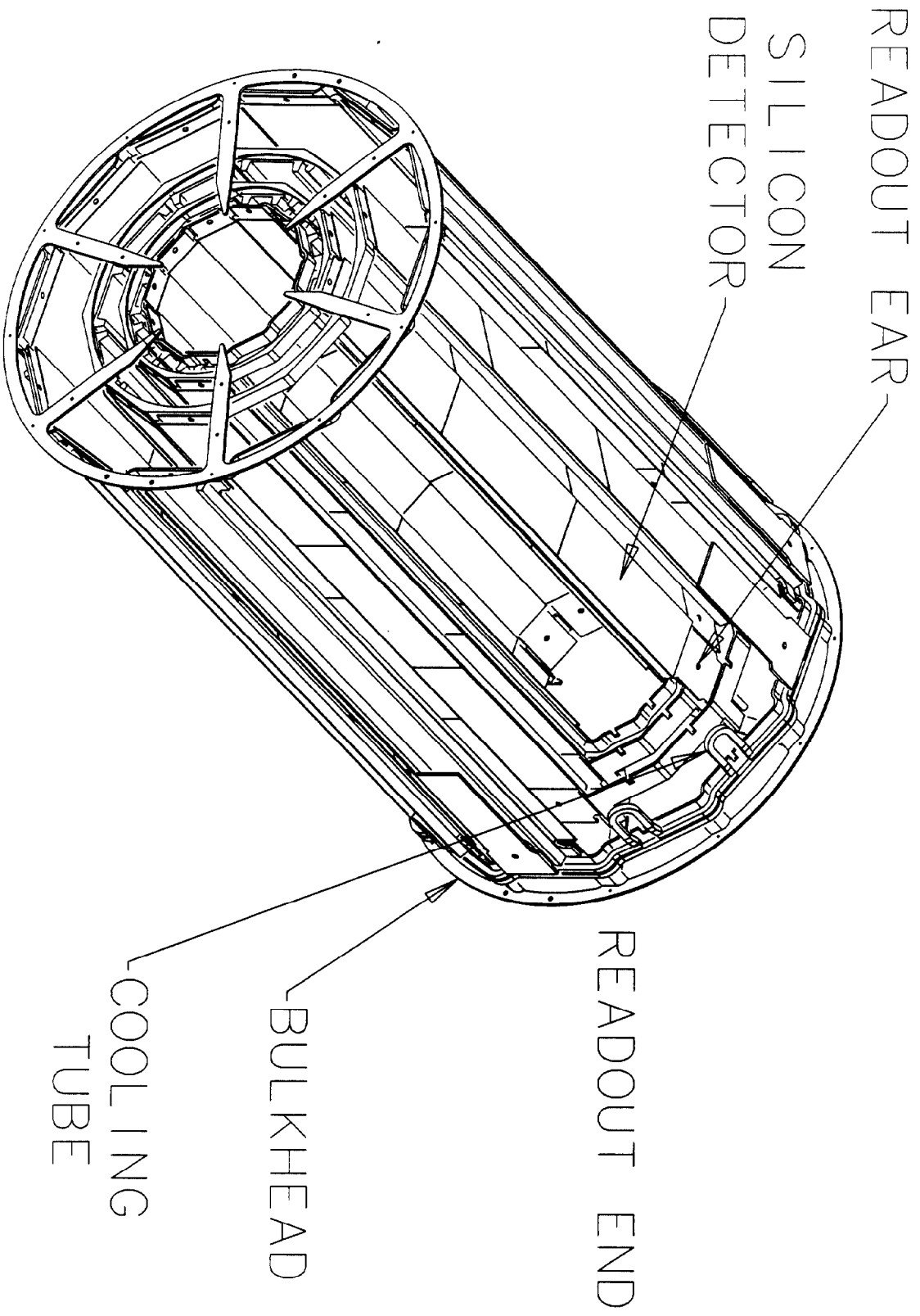


FIG. 2

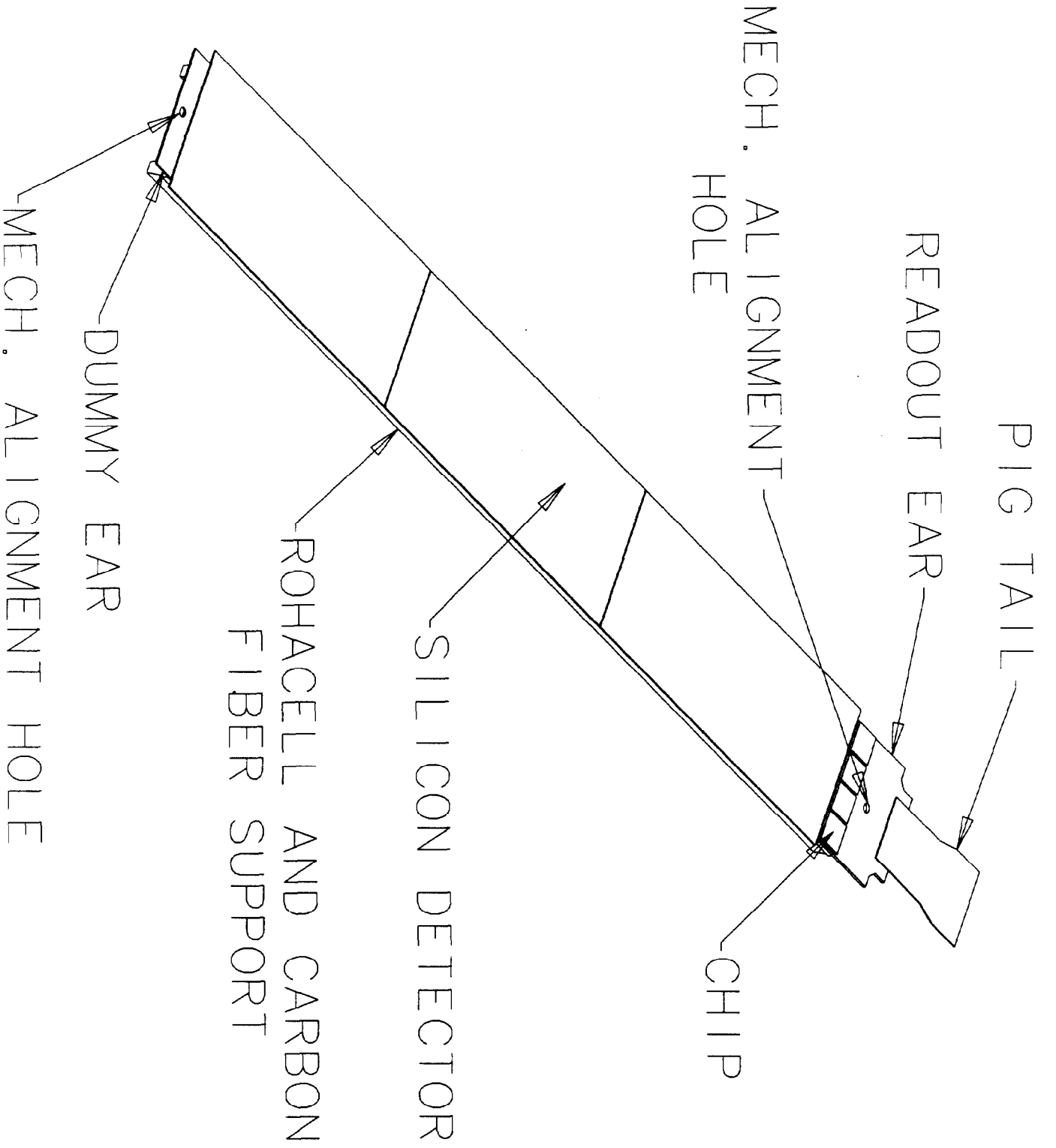




FIG.3

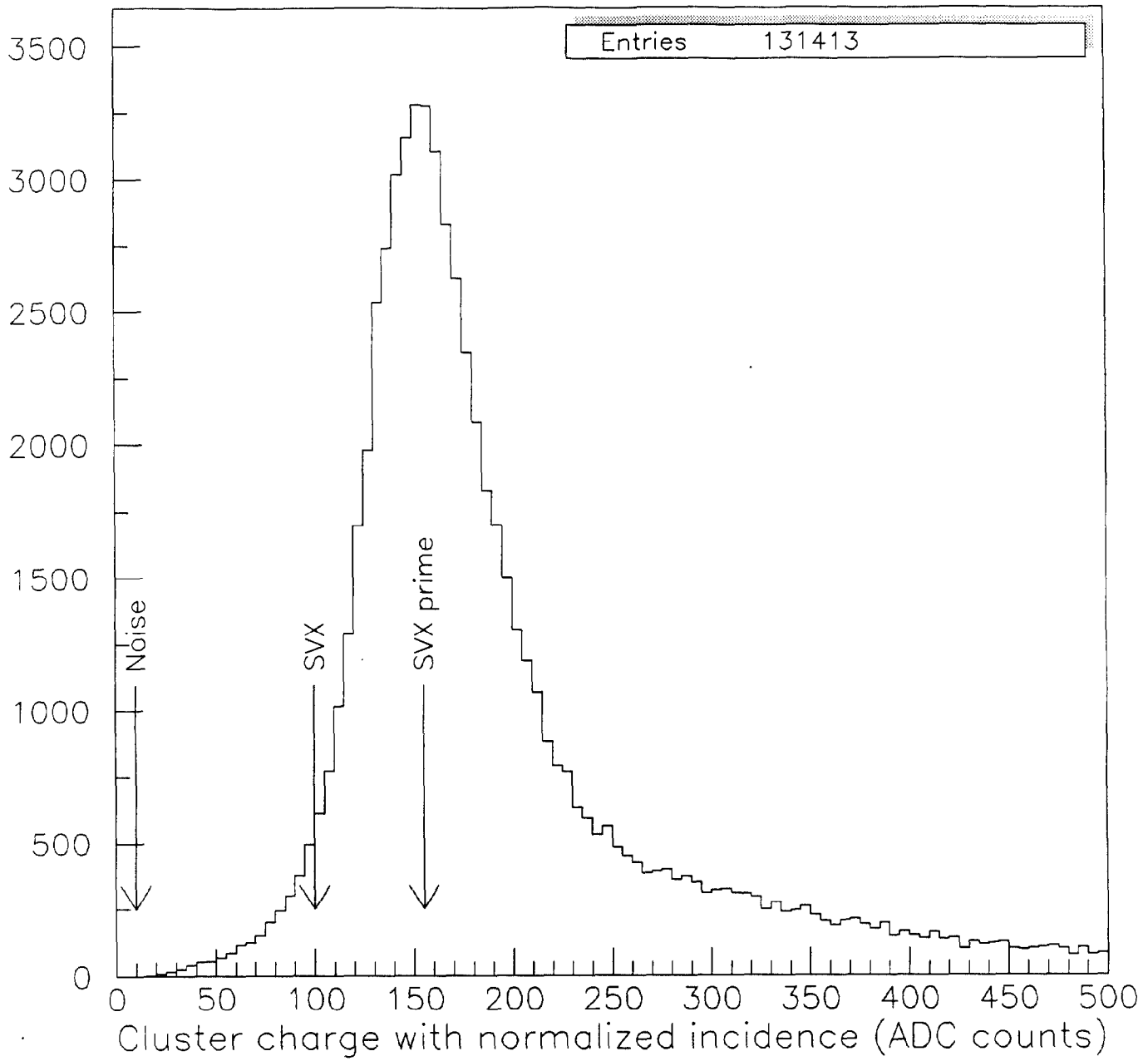


FIG. 4

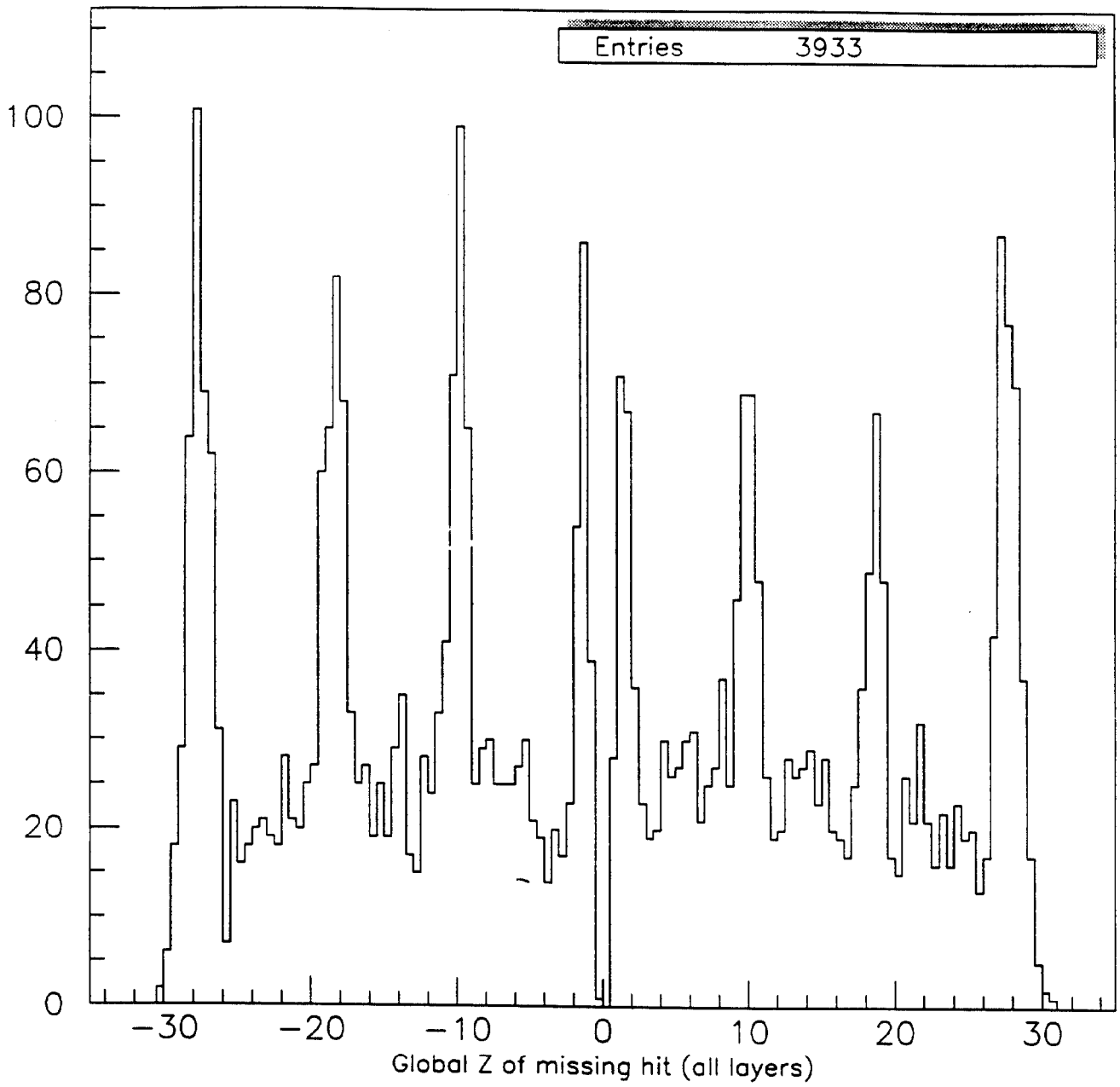


FIG. 5

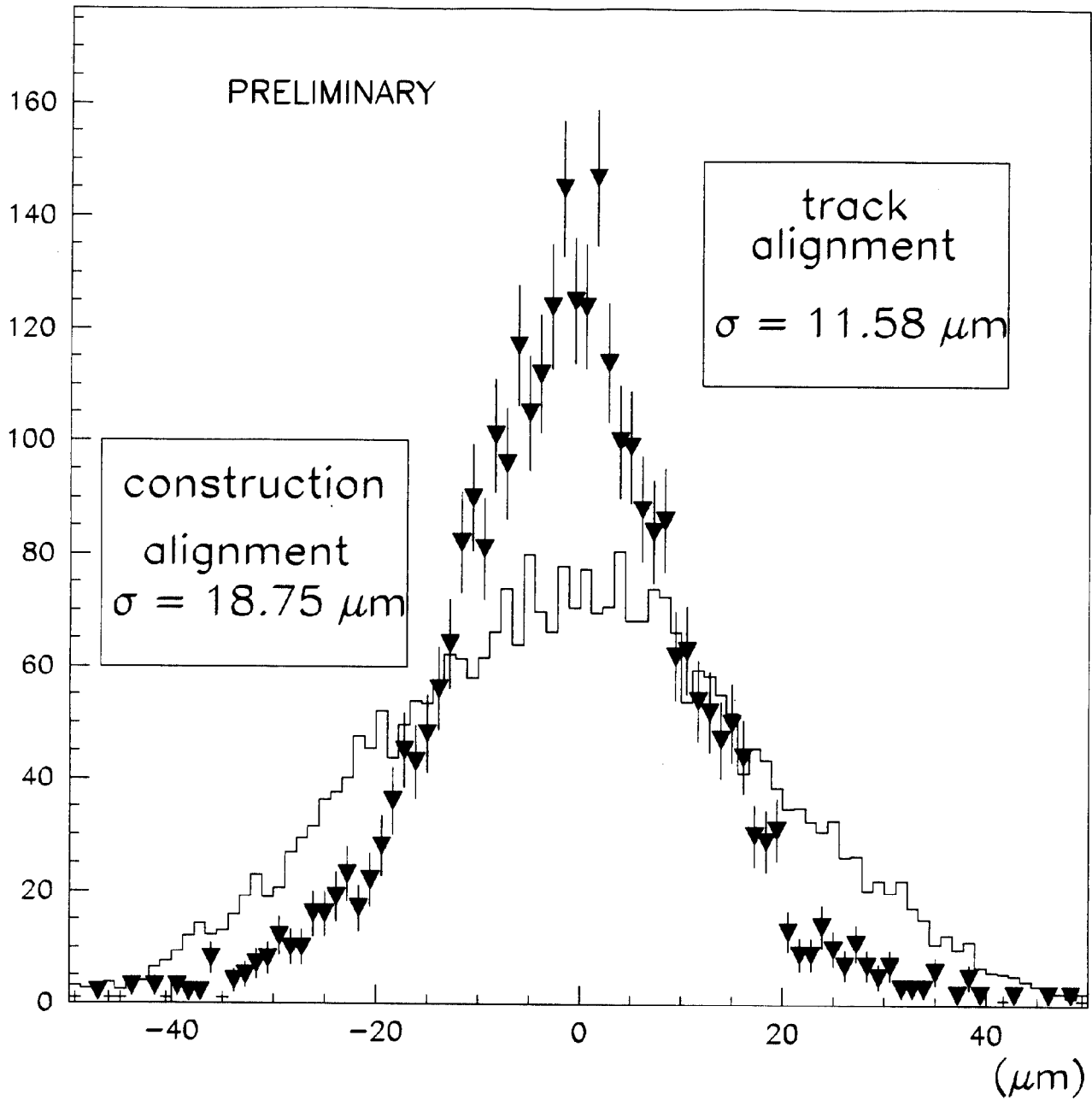


FIG. 6

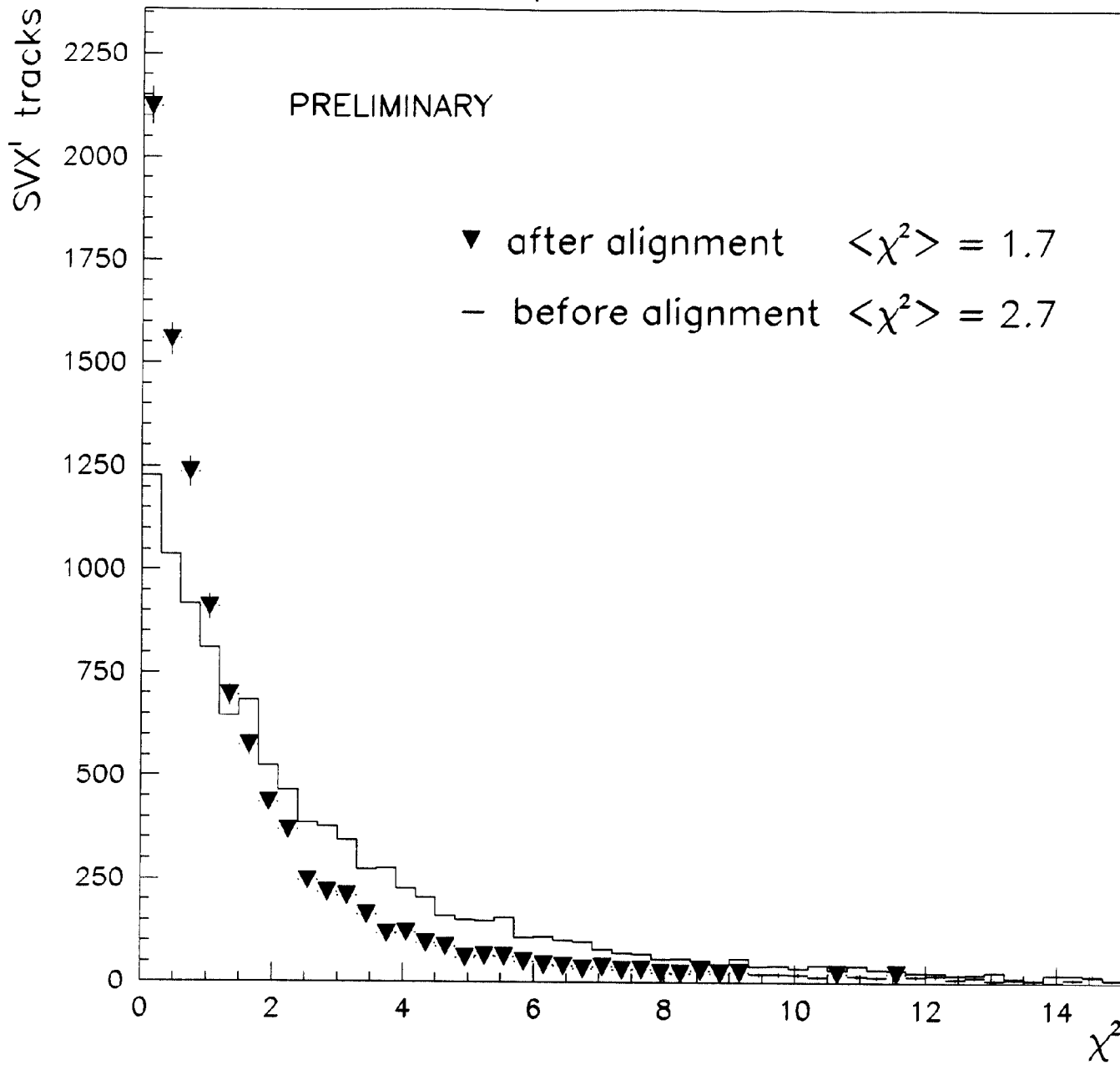


FIG. 7

