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Silicon Oxide (SiO_x) - A Promising Material for Resistance Switching?

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Abstract

Interest in resistance switching is currently growing apace. The promise of novel high density, low power, high speed non-volatile memory devices is appealing enough, but beyond that there are exciting future possibilities for applications in hardware acceleration for machine leaning and artificial intelligence, and neuromorphic computing. A very wide range of material systems exhibit resistance switching, a number of which – primarily transition metal oxides – are currently being investigated as CMOS-compatible technologies. Here we make the case for silicon oxide, perhaps the most CMOS-compatible dielectric, yet one that has had comparatively little attention as a resistance switching material. We present a taxonomy of switching mechanisms in silicon oxide, and summarise the current state of the art in

modelling, understanding fundamental switching mechanisms, and exciting device applications. We conclude that silicon oxide is an excellent choice for resistance switching technologies, offering a number of compelling advantages over competing material systems.

1. Introduction

Silicon oxide (SiO_x) has long played a vital role in semiconductor microelectronics. The dominance of silicon as the universal semiconductor has been driven in no small part by its ability to form readily a stable, wide-bandgap insulating oxide (SiO_2) with a near-perfect interface with Si, which enables the fabrication of field effect transistors (FETs) monolithically integrated onto silicon substrates. Silicon dioxide offers numerous technical advantages over other insulators, including a low density of interface states at the Si/SiO_2 interface, relatively low electron and hole trapping rates, large conduction band offset with silicon (3.1eV), and extreme compatibility with CMOS processing. While in recent years high- κ dielectrics such as HfO_2 have offered advantages in enabling devices with smaller effective oxide thicknesses (overcoming difficulties with gate oxide breakdown in ultra-thin SiO_2), silicon dioxide remains at the heart of CMOS technology. Despite decades of research, we are still uncovering hidden complexities and subtleties in the physics and electronic behaviour of silicon dioxide and related sub-oxides of silicon (SiO_x, $x<2$), including some complex structural and compositional dynamics under electrical stress that can lead to resistance switching[1].

Resistance switching describes the phenomenon of the reversible change in resistance state of electronic materials by the application of electrical stimuli. Importantly, this change is not necessarily simply permanent dielectric breakdown, but in many cases is reversible between at least two, typically non-volatile, states. There is a wide range of different device structures and materials that exhibit resistance switching, which can be governed by various physical

processes, ranging from phase change between amorphous and crystalline states[2], magnetoresistive effects[3,4], nanomechanical effects[5], pure electrical effects[6], to ionic redox processes[7]. Such effects are commonly exploited in non-volatile Resistive Random Access Memory (RRAM) devices, and show great promise for next-generation semiconductor memory technology. Redox-based Resistive Random Access Memory (ReRAM), which we will be mostly concerned with in this review, represents a subclass of broader Resistive RAM (RRAM)[8], in which resistance switching is governed by nanoionic redox processes and by correlation between electron and ion dynamics. In terms of applications, while resistance switching technology is principally investigated for use in memory devices[9], ongoing studies extend its application to a variety of functions beyond pure memory: computing[10], switches in integrated circuits[11], random number generators[12,13], and novel non-Von Neumann and neuromorphic architectures [14,15,16].

A ReRAM cell consists typically of a simple metal-insulator-metal (MIM) structure, though many variations are possible (either or both electrodes could be semiconducting, or the sandwiched insulating/switching material could consist of multiple layers). The pristine state of an as-fabricated cell is typically highly insulating. However, with application of suitable voltage bias, it is possible to induce soft breakdown, where the cell exhibits much higher electrical conduction post voltage stimulus. This process, with respect to ReRAM operation, is termed electroforming. An initial electroforming step is generally, though not always, needed to enable cell operation. Following electroforming, the ReRAM cell can be switched between at least two stable (typically non-volatile) resistance states: the Low Resistance State (LRS) and the High Resistance State (HRS). Under appropriate conditions, devices can be made to cycle between resistance states many times, while each state can be stable for a long time (more than 10 years) even at an elevated temperature (e.g., 85 ^{o}C) until the next electrical stimulus is applied. This makes devices particularly attractive for non-volatile memory

applications. While electrically-driven changes in resistance can be the result of many different physical processes, broadly speaking, they can be classified into two types: filamentary resistance switching, in which the resistance of a single filament bridging the insulating layer is changed, and homogeneous switching, in which the resistance of a continuous volume of material between electrodes varies. We shall discuss the former type, which is much more common.

Most materials used for ReRAM devices lack full compatibility (or are costly) with the dominant silicon complementary metal-oxide-semiconductor (CMOS) fabrication technology. In this report, we focus on silicon oxide (SiO_x, $x \leq 2$), historically one of the most studied oxide materials, as the switching material. Although one of the most widely deployed materials in modern electronics, we are still discovering its novel, remarkably rich, dynamics, which reveal many interesting electronic phenomena. While resistance changes in silicon oxide, other than destructive dielectric breakdown, have been somewhat neglected, it is in most cases a fully foundry-compatible material. Furthermore, SiO_x ReRAM devices have been the subject of differences of opinion - some literature suggests that resistance switching in metal-free silicon oxide is not possible [17]. On the contrary, it is very much possible and could potentially provide many advantages over other ReRAM material systems, as we shall demonstrate below.

Studies of resistance switching in silicon oxide date back to the 1960s and 1970s[18,19,20] at which time the focus was firmly on irreversible electrical breakdown. However, there has been a resurgence in interest in reversible soft breakdown (resistance switching) in silicon oxide in recent years[21,22,23,24,25,26]. Switching can result from a number of very different processes, and it can be diverse in terms of performance and device structures.

Here we aim to provide an overview, classification, and taxonomy of different physical mechanisms of silicon oxide resistance switching in Section 2. Details of electrochemical models of resistance switching are discussed in Section 3. We discuss the existing atomistic models that describe generation of mobile ionic species and early stages of oxide breakdown as well as physical and circuit models of breakdown and resistance switching in silicon oxides in Section 4. Performance comparison of silicon oxide-based ReRAMs with hafnium oxide-based ReRAMs is given in Section 5, and compatibility with fabrication processes and system integration is discussed in Section 6.

2. Phenomenological Classification and Taxonomy of Resistance Switching in Silicon Oxide

As mentioned above, resistance switching in silicon oxide can result from a number of very different processes. To bring some order to the different phenomena, we can begin by classifying the switching processes broadly into those that are intrinsic properties of the pure oxide – *intrinsic* switching – and those that require the indiffusion of conductive species such as metal ions, typically from one of the metallic electrodes, or for the oxide to be directly doped with metals – *extrinsic* switching[27]. We describe extrinsic switching in SiO_x in more detail in section 3, but here we will spend some time considering intrinsic switching, which is a term that describes several mechanisms. We can subdivide the classification depending on whether the switching occurs only in a non-oxidising (typically vacuum) ambient, or also in an oxygen-rich environment. The first type we shall term *air sensitive*, and the second one *air stable* resistance switching. The former typically, although not exclusively, occurs in devices with an exposed oxide surface, and only occasionally in the bulk of the oxide. Regardless of the device structure, which could have exposed oxide edges[21], internal pores[28], or bulk oxide between electrodes[23], air sensitive switching is only possible in vacuum or in devices that have been hermetically sealed/encapsulated to avoid oxidation of conductive filaments

generated during the electroforming that drives the initial chemical reduction of the oxide. On the other hand, air stable switching is possible in both oxygen-rich and vacuum environments, and can be seen as “true bulk switching”, occurring well away from exposed edges, and critically depends on oxide microstructure[22,29,30,31]. Clearly, the two switching mechanisms are fundamentally different, and driven by different physics. Air sensitive switching is generally thought to be governed by phase changes and crystallisation of silicon in oxygen deficient regions[32], although different mechanisms have also been proposed[33]. It is found to be exclusively unipolar; that is to say, the transitions between resistance states always occur in the same polarity, indicating a fundamental role for current-driven Joule heating in the process. Air stable switching, on the other hand, is driven by the generation of oxygen vacancies within the bulk of the oxide, and may be bipolar, unipolar or both[29]. Crucially, there is no evidence for the formation of crystalline inclusions in the oxide during the switching mechanism. The classification of silicon oxide-based ReRAM devices is summarised in **Figure 1**.

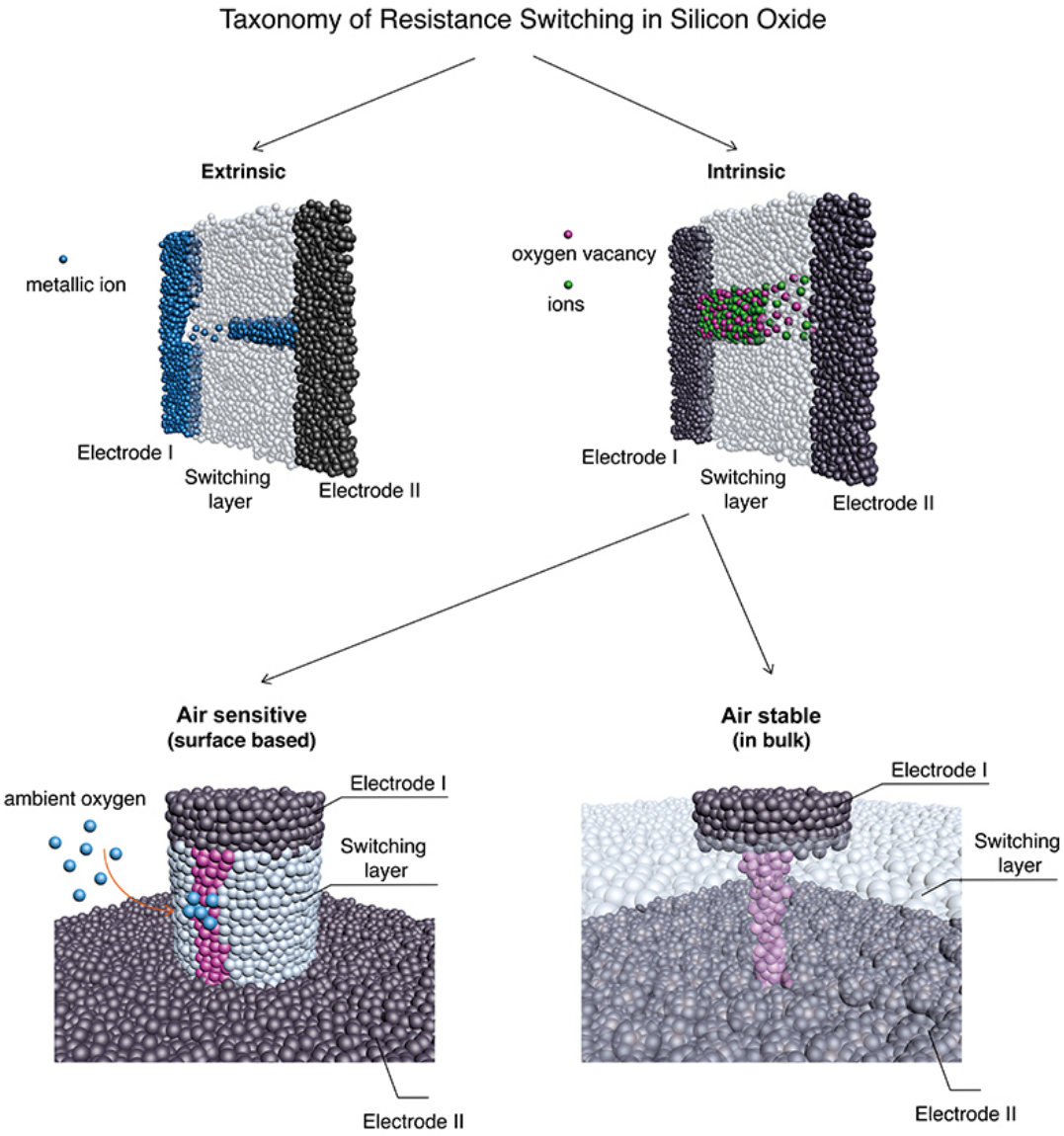

Figure 1. Taxonomy of resistance switching in silicon oxide. Upper LHS: schematic of extrinsic resistance switching. Upper RHS: Schematic of intrinsic resistance switching. Lower LHS: Air sensitive resistance switching: typically, electroforming and resistance switching occurs only in devices with an exposed oxide surface and not in bulk devices. This is attributed to re-oxidation of surface-based silicon filaments by an oxidising ambient. Lower RHS: Air stable resistance switching. This type of switching occurs in ambient (oxidising) conditions and is defined by the microstructure of the oxide material. Switching voltages are typically lower compared to air sensitive switching.

Extrinsic resistance switching in silicon oxide, more commonly known as Electrochemical Metallization (ECM) or Conductive Bridge (CBRAM), is shown schematically in Figure 1 (upper left panel). This type of switching is governed by the electrodeposition of mobile metallic ions (typically Ag or Cu) from an electrochemically active electrode onto a passive (electrochemically stable) electrode and formation of conductive filaments bridging the oxide

under application of a positive electrical bias (with respect to the electrochemically active electrode); a bias of the opposite polarity (negative electrical bias) triggers the dissolution of the conductive filament by removing metal ions from the oxide. This is clearly revealed by in-situ TEM analysis of planar SiO_2 ReRAM devices[34] where the abrupt current increase with the application of positive bias corresponds to the formation of a clearly distinguished silver conductive filament (or multiple partly formed filaments). Subsequent to this, application of a negative bias leads to the dissolution of the filament and a corresponding current drop. The conductive filament could also be non-continuous and consist of multiple metallic nanoclusters, where movement of metallic ions and clustering is governed by ion mobility and redox rates[35]. Extrinsic switching is exclusively bipolar, in the sense that the SET process (transition from HRS to LRS) and the RESET process (transition from LRS to HRS) always occur in opposite polarities. Further detailed discussion about ECM switching will be provided in the following sections.

Turning to intrinsic switching (**Figure 1** upper RHS) we note that air sensitive switching is only possible in non-oxidising atmospheres (**Figure 1** lower LHS). In most cases, for successful set and reset processes, devices must be operated in vacuum (<1mTorr). The device structure may be such that it accommodates filament formation on the exposed surface of silicon oxide – either the edge of a mesa structure, or the surface of planar devices[21,32]. However, it has been reported that bulk silicon oxide devices – ones with continuous silicon oxide layer – may also exhibit this behaviour[23], though in this case there must still be some indiffusion of oxygen into the oxide film. In both cases, the resistance switching exhibits unusual unipolar switching curves; the set voltage is higher than the reset voltage, which is the opposite to the case of the majority of other unipolar metal oxide ReRAM devices. While the switching mechanism is still under debate, here we mention two prominent models. The first model assumes that the electrically driven formation of silicon-rich regions is followed

by crystallisation and formation of silicon nanocrystals, as suggested by TEM analysis[32]. Significantly, the observed silicon nanocrystals are proposed to be semi-metallic Si-III and Si-VII phases rather than the conventional Si-I semiconducting phase. The reset process is governed by thermally induced amorphisation of silicon and shrinking of nanocrystals. The second model is based around a proton exchange reaction[33]. It is suggested that, during the fabrication process (e.g. plasma-enhanced deposition), hydrogen is incorporated into SiO_x to form stable $(SiH)_2$ defects. The SET process is modelled as proton release from $(SiH)_2$ to form conductive hydrogen bridge Si-H-Si defects, while the RESET process involves proton recapture to recover non-conductive $(SiH)_2$. Both models explain the observed unipolar switching I-V curves.

Air stable switching (**Figure 1** lower RHS) is phenomenologically different, and occurs in either oxygen-rich atmospheres or vacuum, although it seems that only oxygen-rich environments lead to a full reset process[24]. Switching could be either unipolar (typical unipolar, with set voltages higher than reset voltages) or bipolar; with the possibility of both types coexisting in the same ReRAM cell. The switching is critically defined by the microstructure of the oxide material[1], and typically exhibits much lower programming voltages (especially the electroforming voltages) than air sensitive intrinsic switching[36]. The switching mechanism is governed by breakage of silicon-oxygen bonds, followed by the creation of Frenkel pairs, consisting of oxygen vacancies and interstitial oxygen ions. Interstitial oxygen ions can easily drift in the oxide under applied field, as they experience low migration barriers of around 0.2 eV[37]. Oxygen vacancies are conductive sites that enable the formation of conductive channels or filaments[38]. The proposed atomistic mechanism of bond breakage is discussed in Section 4. Importantly, there is no evidence of crystallisation of silicon in samples that exhibit this mode of switching, but there is a clear indication of field-driven oxide segregation into silicon-rich and oxygen-rich regions [1].

As mentioned above, microstructure plays an important role in enabling and defining the properties of resistance switching. It has been reported that thermal oxide does not easily electroform and that resistance switching is generally not observed[21]. However, in amorphous oxide films that exhibit columnar growth the defect-rich edges of internal columns can provide favourable sites for filament formation. This explains the observed low electroforming and switching voltages. Columnar growth may be promoted by increasing the roughness between bottom electrode and oxide – rougher interfaces resulting in an atomic shadowing effect and formation of columns[39]. Air stable switching is typically seen in moderately thick oxides (30-40nm), although it can be observed in even thinner, chemically produced oxides[31,40] if the microstructure is appropriate.

2.1. Summary of performance of intrinsic silicon oxide ReRAM devices

Intrinsic resistance switching, with no movement of metallic ions, has better compatibility with CMOS processing technologies than extrinsic switching, as there is no risk of ionic diffusion into surrounding electronics. Moreover, there has been significant progress in recent years to achieve excellent silicon oxide device performance, with metrics in many cases exceeding those reported for other metal oxide ReRAM devices. Table 1. summarises the current state of the art switching metrics, including electroforming voltage, operational voltages (both sweeping and pulsing), endurance, retention and resistance contrast ratio, for various instances of SiO_x ReRAM devices. Additional functionalities, such as high-temperature retention (250°C or more)[36], multiple stable resistance states[28], high self-rectification[31], in-built nonlinearity[29], suitability for flexible and transparent electronics[41], quantised conductance[42], neuromorphic functionalities[33,43,44], and optically driven switching[45] have all been reported. This table highlights the suitability of intrinsic silicon oxide for non-volatile memories. For comparison, we include two highly studied metal oxides

(TaO_x and HfO_x), that have shown the best switching properties. Performance metrics of other metal oxide ReRAM devices could be found in [46].

Table 1. Performance comparison of intrinsic silicon oxide ReRAM devices: electroforming voltage, set voltage (both in sweep and pulsing mode), reset voltage (both in sweep and pulsing mode), endurance, retention, contrast ratio between the resistance states and classification of the switching mechanism.

Structure	Electroforming voltage (V)	Set voltage sweep (pulse) (V)	Reset voltage sweep (pulse) (V)	Endurance (cycles)	Retention (s)	Contrast ratio	Class
Edge SiOx [21]	>20	8(13)	3.5(6)	$>10^5$	$>10^5$	Up to 10^5	air sensitive
Porous SiOx [28]	1.7 (breaking voltage)	3 (5)	8 (15)	$>10^5$	$>10^5$	Up to 10^7	air sensitive
Ta/SiOx/n-Si [47]	17	6	12	Up to 10^7	10^4	10^6	air sensitive
Au/Ti/SiOx/Zr [48]	-5	-3 (-5)	3.5 (5)	$>10^4$	-	Up to 10^4	air stable
TiN/SiO_2/p-Si [49]	5	1.2 (4)	-1.5 (-3)	$>10^5$	$>10^4$	$>10^2$	air stable
Mo/SiOx/Au [36]	-2.7	-1.2 (-1.7)	1.2 (2.5)	$>10^7$	$>10^4$	Up to 10^4	air stable
Mo/SiO_x(HSQ)/Pt [40]	-1.6	-0.8 (-1.05)	1 (1.1)	$>10^7$	$>10^4$	Up to 10^4	air stable
p-Si/SiO_2/n-Si [31]*	7.5	7.5 (10)	4.5 (7)	>100	$>10^5$	Up to 10^4	air stable
Ta_2O_{5-x}/TaO_{2-x} [50]	2.5-3V	1.1 (4.5)	1.9 (6)	$>10^{12}$	$>10^5$	~10	air stable
HfO_2 [51,52,53]	3V	0.8 (1.5)	1 – 1.5 (1.4)	$>10^{10}$	$>10^5$	>100	air stable

*In the case of system reported in [31], the devices are tested in crossbar arrays, thus the switching voltages include the voltage drop on the crossbar wires. The listed metrics for other systems are obtained from single devices.

3. Extrinsic switching: electrochemical reactions and electrochemical metallisation (ECM) resistance switching in SiO_2

We shall now turn our attention to extrinsic resistance switching, and the electrochemical origins of the governing processes.

SiO_2 is one of the mostly studied electronic materials when considered from both fundamental and applications points of view. Reasons for such interest in SiO_2 as a resistance switching medium include its chemical robustness and CMOS compatibility, making device integration easy[54,55]. As discussed above, ReRAM cells using SiO_2 as a switching layer show two different types of switching mechanism, depending on the electrode material – intrinsic and extrinsic ECM/CBRAM. Intrinsic switching is observed for inert electrodes (mainly symmetric) such as Pt, TiN, doped-Si etc.[31,56] . Devices and processes based on intrinsic switching mechanisms are discussed more thoroughly elsewhere in this review.

Extrinsic switching (ECM or CBRAM) requires electrochemically active electrodes such as Ag or Cu, and is based on the formation and rupture of a silver or copper metallic filament. SiO_2 is used either as a pure host medium[57,58,59] or is in some cases doped by thermal annealing[60,61], with a thickness typically between 5 nm and 20 nm. The counter electrode is an inert electrode such as Pt, Ir, TiN etc. and should not be able to dissolve and electrochemically react during the switching processes. In addition, SiO_2 is often used as a barrier (or second layer), significantly improving the device characteristics[62,63,64]. SiO_2-based ECM devices were reported to switch at very low currents and low power[65,66], to be fast[67], extremely stable against radiation[68] and can operate at temperatures as low as 7K[61].

3.1. Electrode redox reactions

Electrode reactions with Ag and Cu precede resistance switching in ReRAMs. SiO_2, as many other oxides, is a high band gap material that can be expected to show insulating properties. However, nanoscale effects, extreme electrochemical conditions and the presence of protons blur the borders between insulators and electronic/mixed conductors, allowing macroscopically insulating oxides to transport ions/electrons and allow electrode redox

reactions[69,70]. Redox reactions preceding resistance switching were first reported for the Cu/SiO_2 system[57,71]. **Figure 2** shows the redox peaks of a Cu^{x+}/Cu (x=1, 2) half-cell during cyclic voltammetry using $Cu/SiO_2/Pt$ cells.

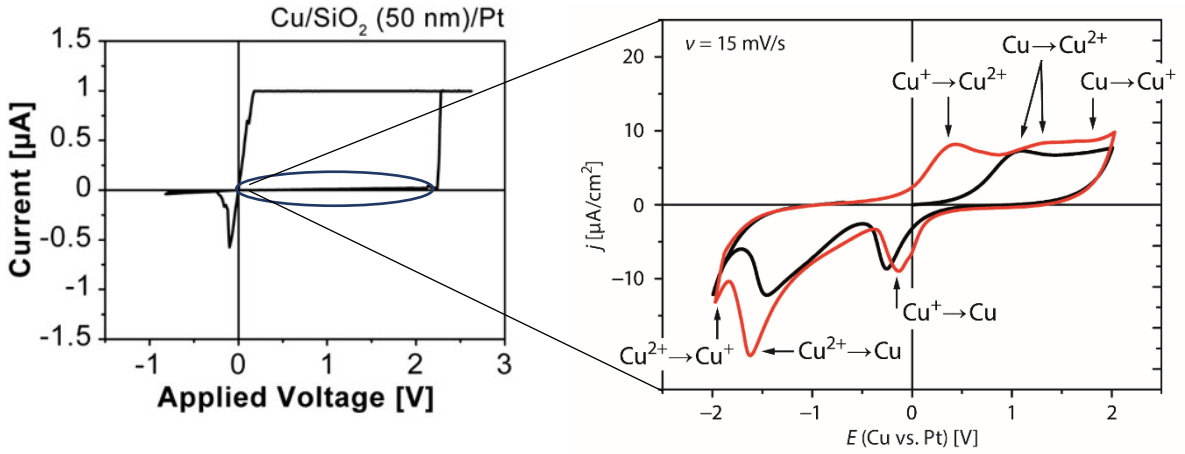

Figure 2. I-V sweep for a switching cycle (left) and cyclic voltammetry (right) for the system performed in a voltage window that does not allow formation of a filament/switching. The figure is adapted from [57].

From the I-V sweep one cannot immediately conclude that there is any electrochemical reaction, because the increase of the current at positive voltages is directly related to the short circuit due to the formed metallic filament. However, increasing the instrument sensitivity and limiting the positive vertex potential we ensure conditions where the electrochemical reactions responsible for the resistance switching can be detected and characterized. Therefore, this was the first direct evidence that electrochemical reactions of the active electrode precede, and are responsible for, the subsequent process of resistance switching. Nevertheless, it is not always easy to find the proper experimental parameters to resolve the redox peaks. Several parameters should be carefully considered, such as the oxide material, the partial electronic conductivity, film thickness, voltage sweep rate, density and ambient. In some cases the sweep rate must be low e.g. [71,72,73,74], but in others it should be very high e.g.[75]. Thus, finding the proper conditions is material-specific.

Silver and copper behave differently regarding redox reactions and transport. From a thermodynamic point of view the half-cell potentials and polarizability of both metals is different as well as their oxidation states, predetermining different numbers of exchanged electrons. For these reasons the overvoltage and also the switching voltages using Ag active electrodes are in generally lower than those for Cu electrodes[58]. The diffusion and stability of Ag and Cu ions is also different. Whereas Ag forms weaker bonds to the SiO_2 matrix, Cu ions form stronger bonds, resulting in higher activation energies for transport, and a correspondingly lower diffusion coefficient[76].

In addition, it has been recently observed that metals considered as inert, such as Pt and Pd, can behave and act as active electrodes, allowing for electrochemical reactions and even filament formation/rupture [77,78]. Moreover, ions such as Ta and Ti were also found mobile within SiO_2 [79,80], showing even superior performance compared to Cu and Ag[80].
Not only is the active electrode important, but also the choice of the counter electrode is crucial[72]. The reason for this strong influence is the electrochemical nature of the process of filament formation. Formation of the filament begins at the counter electrode (negatively biased during the SET process) and its catalytic activity towards reduction reactions is extremely important. It has been found that several reactions can compete at the counter electrode, such as reactions of moisture and of the active ions[58]. Cyclic voltammograms for different counter electrode materials are presented in **Figure 3**.

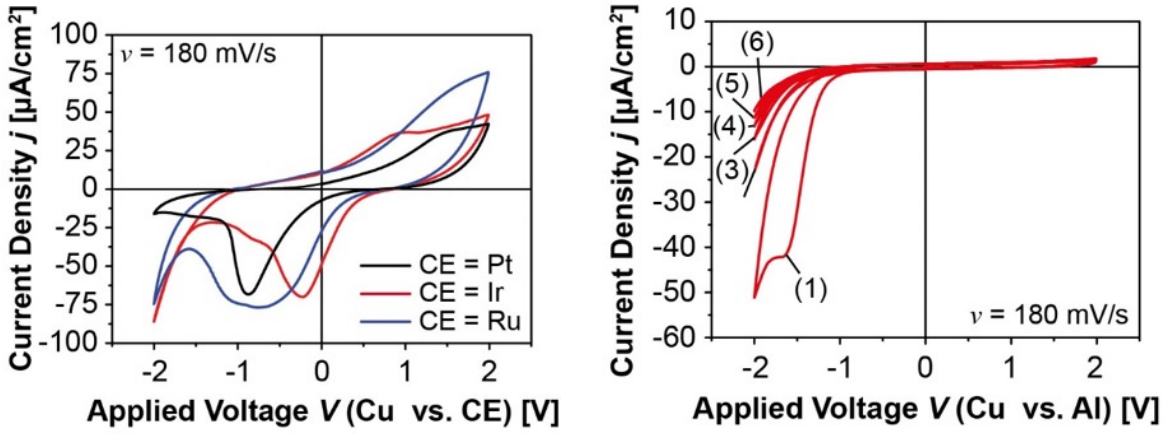

Figure 3. Cyclic voltammograms for the Cu/SiO_2/Me system. Me denotes different counter electrodes. Characteristics of noble metal electrodes (left) and Al electrode (right). The figure is adapted from [72].

As can be seen, the noble metal electrodes show different catalytic activities; the most catalytically active appears to be Ir, followed by Ru (close to Ir) and Pt. Thus, from an electrochemical point of view devices using Ir or Ru electrodes should demonstrate better performance, at least regarding switching time. Electrodes with a high affinity to oxygen such as Al or Ta passivate easily and block further reactions. The obtained results have shown that in fact the counter electrode reaction has a lower reaction rate (compared to that of the active electrode), and therefore determines the reaction rate of the whole system. Thus, increasing the counter electrode reaction rate will lead to a higher reaction rate also of the active electrode and thus, a shorter switching time. Experiments on the switching kinetics in Cu/SiO_2/Me devices using different counter electrodes have clearly confirmed these conclusions [59].

Knowledge of the processes occurring prior to and during resistance switching were implemented in a physical based model including all possible rate limiting steps during SET and RESET such as nucleation, growth, dissolution and Joule heating[81,82,83]. The model shows that the strongest influence on the switching time is the process of phase formation (nucleation). Moreover, the type of switching and the form and direction of growth of the

metallic filament is determined by a combination of fundamental properties such as ion mobility and reaction rates[77].

The electrochemical nature of ReRAM devices also has another implication, namely the nanobattery effect[84]. The nanobattery effect is in fact an electromotive force generated by factors such as chemical asymmetry of the electrodes (Nernst potential), inhomogeneous distribution and mobility of ions (diffusion potential), or in the case of nano-size particles/filaments also the increased surface energy effect (Gibbs-Thomson potential). The different contributions can occur individually or together, influencing the ON and OFF states and also the SET and RESET kinetics[84,85]. The nanobattery effect is often modulated by interface interactions between the electrode and SiO_2. It has been found that, irrespective of the macroscopic thermodynamic predictions, oxide thin films always form at the interface between active metals and SiO_2 [58,86]. This oxide film, for example in the case of Cu/SiO_2, provides an important source of Cu ions.

3.2. Influence of moisture and device performance

Both electrochemical reactions and device performance in SiO_2-based memristive cells are strongly influenced by moisture. It has been found that moisture can easily penetrate into SiO_2, but also can be evaporated easily in vacuum[87]. Cells and devices without any moisture within the oxide are not able to be formed at all[58]. The switching itself was also found much more reliable in the presence of moisture. The role of the moisture is twofold – firstly, it provides the necessary counter charge reaction that is essential for the proper operation of the whole cell, but it also influences the nanobattery effect, which impacts the stability of the device[58]. It has also been demonstrated that, in fact, the influence of the counter electrode material is mainly due to enhanced reaction rate, enabling higher reaction rate of the active electrode and the corresponding formation of a larger number of active ions that can

participate in the process of filament formation[59]. The moisture is absorbed within the nanoporous oxide matrix and can also serve as "dissolving agent", enhancing ion mobility.

Figure 4 shows the SET kinetics for Ag/SiO_2/Me devices using different counter electrode materials.

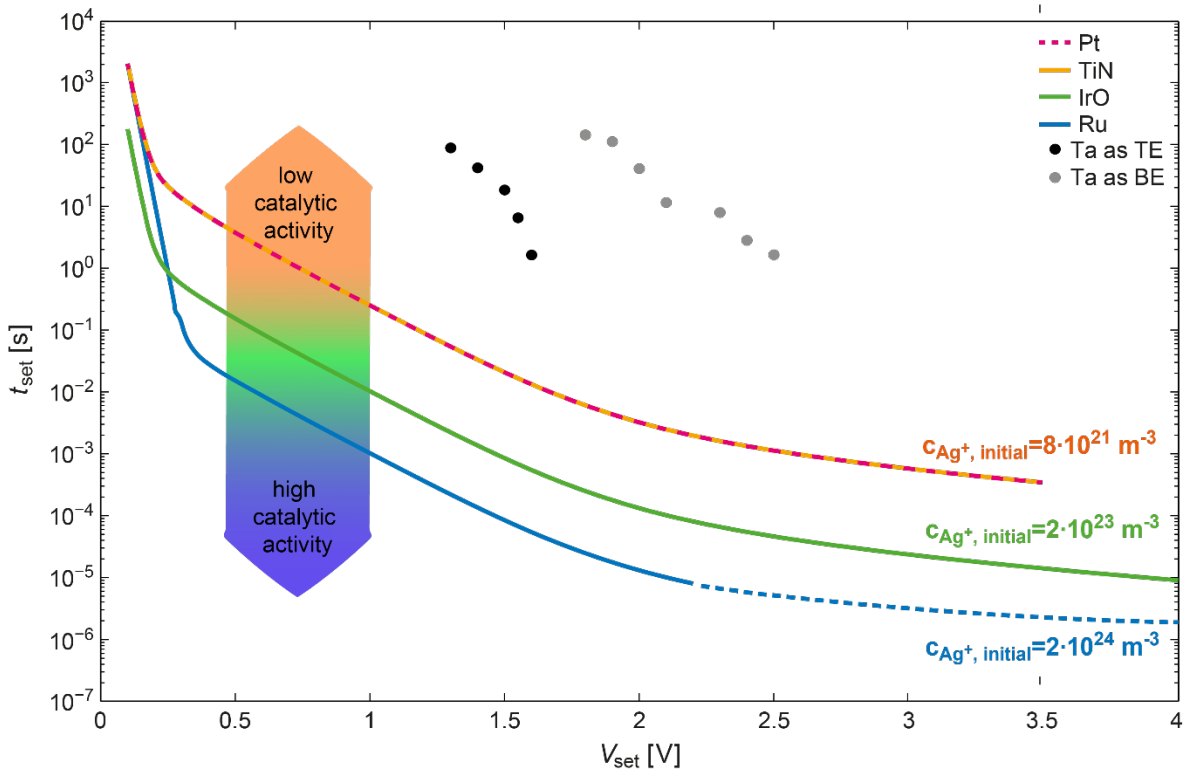

Figure 4. SET kinetics for Ag/SiO_2/Me devices, using various counter electrodes. The figure is reproduced from[59].

The results demonstrate the correlation between the catalytic activity of the counter electrode, the number of generated active ions and the switching kinetic, SET time. Thus, the device kinetics and performance are inherently related to the presence of some residual moisture/protons that can be incorporated either during the preparation processes/steps or from the local environment.

ECM (extrinsic) devices based on SiO_2 still suffer from large variability that hinders their commercialization. This variability is caused on one hand by the changing properties of SiO_2 during cycling (enrichment with Ag/Cu ions), and on the other hand due to their

inhomogeneous distribution and variable concentration of moisture/protons being also sensitive to temperature, particular encapsulation, local structure, operating voltages/currents. Further improvements may include doping of SiO_2 with selected elements in order to eliminate the dependence on moisture and to stabilize the filament. In addition, different combinations of active/counter electrode materials can be tested for optimal device performance. Interface engineering is also expected to significantly modulate the kinetics, endurance and retention [88]. More recently, there has been a lot of interest in using silicon oxide ECM devices in volatile type switching for select devices in crossbar arrays[80, 89, 90]. Both Ag and Cu have been used as top electrodes, and it has been shown that by controlling current compliance it is possible to induce either non-volatile or volatile switching. In the case of Ag/SiOx devices, current compliance lower than 80 μA produces volatile switching with very high resistance contrast ratios (more than eight orders of magnitude) and virtually infinite transition slope[80]. Furthermore, it is possible to utilise defect engineering of a graphene layer (between the SiO_x and the Ag electrode) to obtain both highly desirable low operational current (~10μA) memory and high driving current (~1mA) selector devices[90].

This remains a fertile field of research, and further significant improvements in extrinsic (ECM) device performance can be expected in the coming years.

4. Physical and circuit models of breakdown and resistance switching in silicon oxide

We now turn from an electrochemical description of resistance switching to models that take inspiration from the underlying physics to generate circuit models that can be used to develop circuit- and system-level design rules.

4.1 Phenomenological models of oxide degradation and breakdown

Since the earliest observations of resistance switching in silicon oxide (SiO_x), the phenomenon has been unquestionably linked to filamentary-type conduction, *i.e.* to electron transport through an oxide layer that has locally lost its insulating capability. The filament we are dealing with is often thought to consist of a chain of oxygen vacancies (VCM) or metal atoms (ECM) that allows the transit of electrons from one electrode to the opposite one in a variety of ways depending on the material bulk properties and its interfaces. The formation and dissolution of a gap region along this filament caused by the movement of atomic species determines whether the system is in the low (LRS) or high (HRS) resistance state. Depending on the lateral size of the conducting pathway, the magnitude of the current in both states can be lower or higher, which in turn determines the modelling framework.

In order to understand the evolution of the ideas concerning physical and circuital models for resistance switching in SiO_x, it is important to realize that two lines of research developed almost in parallel starting some sixty years ago until recently. First, one related to the investigation of the resistance switching phenomenon itself from a pure materials science perspective and, second, a more practical and focused approach related to thin oxide reliability issues in the context of conventional electron devices such as MOS capacitors and transistors. In this latter case, the switching property of the oxide layer was not specifically pursued but instead the mechanisms leading to the filament formation (oxide breakdown) and its final consequence on the output characteristic of the devices (post-breakdown conduction mode) were extensively investigated[91, 92]. Understandably, because of the aims of microelectronics industry, the focus of research was initially placed on the driving forces behind the wear-out and breakdown phases of thermally grown SiO_2[93,94,95,96,97]. Later on, the interest shifted to high-κ films and to their potential use as switching elements in non-volatile memories[98,99,100,101]. Stress conditions and degradation are connected through acceleration laws that depend on the electric field or voltage applied to the structure [102]. The use of MOS

devices for the study of the SiO_2 wear-out and breakdown is widely accepted. A central difference with MIM devices is the potential drop in the semiconductor substrate.

Different measurement techniques contribute to the understanding of the physics involved: constant current or voltage [103], dynamical stress[104], or radiation-induced degradation[105]. In the past, the SiO_2 degradation process was attributed to dipole flipping[106], hole injection[107] and hydrogen release [108]. In general, electron traps, hole traps and interface states have been linked to oxide breakdown [109,110]. During degradation traps or defects are generated until a critical density is reached and a percolation path formed. This final step is identified with the breakdown of the oxide layer [111, 112, 113]. Remarkably, percolation models are able to explain the area and thickness dependence of the failure statistical distributions (Weibull plot). Percolation mechanisms have been considered for resistance switching devices as well[114]. Electron conduction in SiO_2 during the degradation stage has also received extensive attention. In thick oxides (t_{ox}>10 nm), Fower-Nordheim conduction is affected by charge trapping[115, 116]. In thin oxides (t_{ox}<7 nm), stress induced leakage current (SILC) is the dominant mechanism at low biases[117,118, 119]. Fowler-Nordheim tunneling as well as SILC have been used to sense the degradation level of MOS devices[120,121,122].

On the contrary, the physics of SiO_2 post-breakdown conduction has been much less investigated. Many of the breakdown models proposed in the past remain to be more deeply explored in this regard, but others have survived and evolved and now form part of the battery of models available for explaining resistance switching in SiO_x. Abrupt or gradual changes of the conductance occur in a damaged oxide depending on the thickness of the dielectric, the area of the device and the stress magnitude[123, 124]. The first post-breakdown studies in SiO_2 were carried out by Klein *et al.*[125,126,127], who explored the transitions of the films to the "high-conduction" state. Shatzkes *et al.*[128] further investigated this issue confirming that conduction was filamentary and mainly governed by the applied voltage and not the electric

field. Oxide thickness and device area were found to play a minor role[23]. Hickmott[129], Dearnaley *et al.*[130], and Buden *et al.*[131] investigated filamentary conduction in materials such as SiO_x, TiO_x, LiF, CaF_2, and Ta_2O_5. Reports about the reversibility of the conduction state of electroformed SiO_x started to appear in the literature[132,133]. Measurements at that time were based on thick (t_{ox}≈20-100 nm) oxides, so important thermal damage in the devices was commonly observed. In addition, these devices only exhibited linear conduction characteristics typical of a resistor[134,135]. In the 90s, the growth of thinner oxides (t_{ox}≈5-7 nm) allowed to explore the signature of the dielectric breakdown mechanism[136,137]. Fukuda *et al.*[138] drawn the attention on the existence of a new failure mode in SiO_2 with a current several orders of magnitude lower than that observed before. This new breakdown mode was termed B-SILC[139], quasi[140], partial[141], or soft breakdown[142, 143] (SBD). This is what we call today the high resistance state (HRS). The final, catastrophic, or hard breakdown (HBD) mode is referred to as the low resistance state (LRS). **Figure 5a** shows the occurrence of SBD and HBD failure events in a thin SiO_2 film (4.3 nm). Fowler-Nordheim and SILC are also included in the plot. As shown in **Figure 5b**, multiple failure events can occur in the same device. Each jump in the conduction characteristic corresponds to a new filamentary pathway spanning the dielectric film.

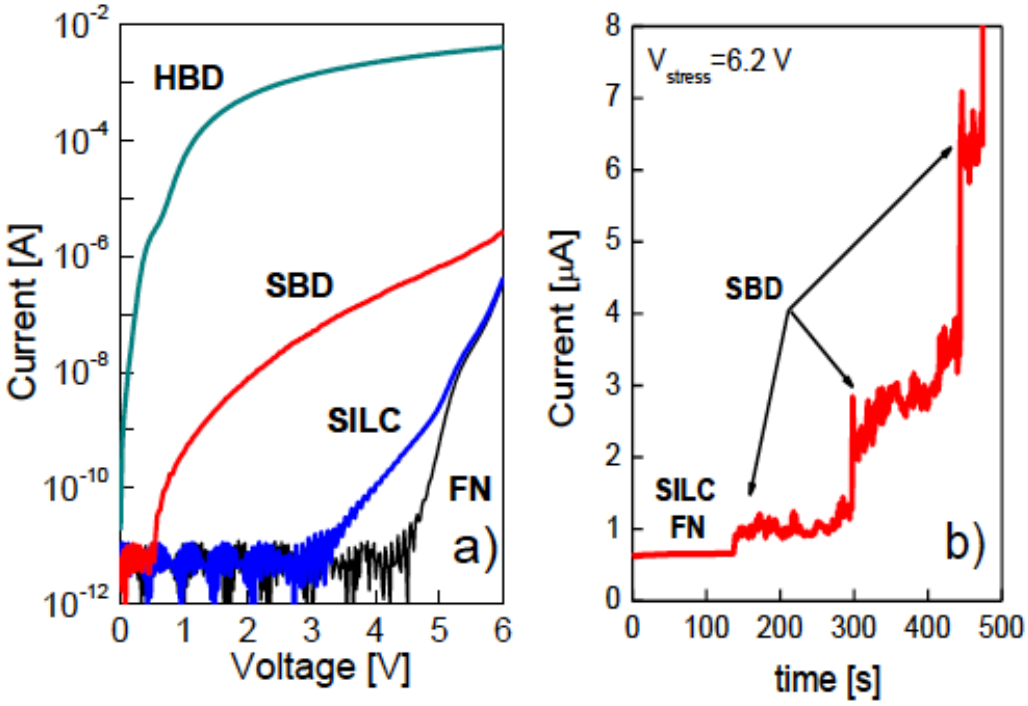

Figure 5. a) Different conduction modes observed in the *I-V* curve of a thin oxide layer (t_{ox}=4.3 nm): Fowler-Nordheim, SILC, SBD and HBD. b) Observation of successive SBD events occurring in the same device. Each jump reveals the appearance of a new breakdown path.

Most of the mechanisms considered for electron transport in dielectrics have been invoked to explain the post-breakdown conduction in SiO_x. In general, they are used to account for the SBD mode exclusively. HBD is often assumed to be Ohmic-type conduction. Unfortunately, the term Ohmic is indiscriminately used to describe linear conduction (many conduction mechanisms are linear at low biases). One of the most considered approaches to describe filamentary conduction in SiO_2 consists in the diode equation with series resistance[136,144,145,146]. According to Umeda *et al.*[147], the post-breakdown *I-V* curve is consistent with the current in a pn-junction diode affected by the spreading resistance effect. Multilevel conduction in SiO_x can also be modelled using an array of diodes with series resistance[148] and more recently diode-like conduction was also proposed for SiO_x-based RS devices[31]. Okada *et al.* showed that variable-range hopping (VRH) can be used to represent

the SBD *I-V* curve[149, 150]. In VRH, conduction is mediated by traps and interface states with different energies. In this case, the *I-V* characteristic is described by a *sinh(x)*-based expression[151]. More recently, Chang *et al.* have also considered hopping in combination with proton exchange reactions for SiO_x RS devices[152]. Houssa *et al.* considered a nonlinear conductor network with percolation thresholds for SBD [153,154]. In this model, traps in the SiO_2 lattice form a conducting backbone from one electrode to the other. Electron scattering accounts for the temperature dependence[152] and Lévy flights describe the current fluctuations[155]. Lee *et al.*[140] proposed that SBD can be represented using a direct tunneling (DT) model (trapezoidal potential barrier) with degradation effects localized in the anodic region. The idea is that the impact of electrons causes a local reduction of the oxide thickness or thinning process. Yoshida *et al.* proposed a similar mechanism[156]. Houssa *et al.* found that a tunneling model of this kind requires unphysical barrier height values[154]. HBD has also been explained using thinned potential barriers[157]. Lowering of the SiO_2 barrier height has been proposed for SBD as well [158,159]. In this case, hole trapping would reduce the insulator band gap affecting the insulating capability of the material. Resonant (RT) and trap-assisted (TAT) tunneling are also among the candidates for SBD and HBD conduction in SiO_2 and SiO_x [23,160, 161, 162]. Ting[163] suggested that crowding effects of the electron wave functions into nanoscale wires in the oxide layer could explain both SBD and HBD. Nigam *et al.*[164,165] claimed that single electron tunneling could deal with both the temperature and voltage dependencies of the SBD current. According to this model, the breakdown path can be represented by isolated islands distributed along the oxide layer. The transit of electrons from one electrode to the other would follow uncorrelated tunnel events determined by the local electrostatic potentials caused by the trapped charges. Both SBD and HBD were modeled using a quantum point-contact (QPC) approach in [166]. In this model, the breakdown path is ideally treated as an atom-sized constriction with adiabatic shape[167]. The confinement of the electron wavefunction induces the quantization of the transverse momentum giving rise to

conduction subbands acting as potential barriers for the injected electrons. Remarkably, these are not material barriers but barriers that appear as a consequence of the low dimensionality of the filamentary path, like the discrete energy levels occurring in a quantum well[168]. The difference between the right- and left-going conduction modes that arise from the relative position of the quasi-Fermi levels at the electrodes and the barrier height is reflected in the conductance of the filament. The barrier profile was obtained using inverse modeling[169]. The QPC model was initially invoked to explain the heavy ion-induced conduction[170], the *I-V* curves in hyperthin oxides[171], the noise figure after HBD[172], and the effects of temperature on the leakage current[173,174,175].

In recent years, Degraeve *et al.* proposed an extension of the model to account for the RS dynamics in HfO_2[176]. Discrete conductance steps of the order of the quantum conductance unit $G_0=2e^2/h$ have been reported to occur in Ta_2O_5 layers by Tsuruoka *et al.*[177] and by Chen *et al.*[178]. Long *et al.* reported similar results for the reset transitions of Pt/HfO_2/Pt devices[179]. The conductance jumps were associated with atomic-size modifications of the filament cross-section. Zhu *et al.* showed conductance quantization in Nb/ZnO/Pt and ITO/ZnO/ITO devices[180], Miranda *et al.* in CeO_x/SiO_2-based RS devices[181], and Mehonic *et al.*[42] reported similar effects in SiO_x resistive switches (see **Figure 6**). Gao *et al.* considered quantization in Ag/SiO_2/In occurring at integer and half integer values of G_0 [182]. Results pointing out in the same direction were also presented by a number of authors[183,184,185,186,187,188] indicating that the idea of quantum conduction is more than a reasonable hypothesis. More conventional mechanisms such as Poole-Frenkel conduction[189,190,23 ,191] and Schottky emission[192] are also frequently invoked to model the high resistance state of SiO_x films. Unfortunately, in the vast majority of the cases, the consistency with the temperature and bias dependence expected for these mechanisms is not demonstrated. This requires deeper understanding of the atomistic processes during resistance

switching and soft breakdown. 3D atomistic simulations of resistance switching and soft breakdown in SiO_x combining field and temperature-assisted electron and ion transport were carried out in [193]. They used atomistic models of oxide degradation processes to describe resistance switching and soft breakdown in SiO_x and provide a new insight into the mechanisms of these processes. These models are considered in more detail below.

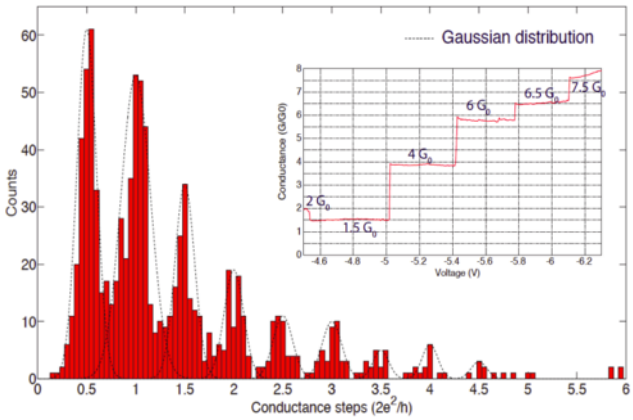

Figure 6. a) Histogram of conductance changes during ~1,000 conductance steps. Clear peaks are evident at half-integer multiples of G_0, which have been fitted with a series of Gaussian distributions as a guide to the eye (dotted lines). b) Conductance-voltage curves for a device showing linear behaviour in the voltage range between -4.5V and -6.1V. Several level conductance plateaux can be seen at half-integer multiples of G_0. Reproduced with permission.[42] Copyright 2018, The Authors.

4.2. Atomistic models of early stages of degradation of SiO_x

As discussed above, the soft breakdown and hard breakdown of complementary metal-oxide-semiconductor (CMOS) devices[194] and resistance switching in ReRAM devices[1, 21, 22, 24, 32] are often attributed to the aggregation of oxygen vacancies as a result of electrically stressing amorphous SiO_x (x = 1.3–2) films. In spite of the intuitive appeal of these models, the atomistic mechanisms behind vacancy aggregation processes remain unclear. They are attributed to the creation of additional oxygen vacancies[1,32,37] near pre-existing vacancies and diffusion and attraction of vacancies[21,22]. Recent simulations[195] shed some light on the feasibility of such mechanisms. Using computational modelling, the structures and binding energies of vacancy dimers and trimers in a-SiO_2, the energy barriers for individual vacancy

diffusion, as well as the effects of trapping extra electrons at vacancies on their mobility have been investigated. These calculations demonstrated the existence of favourable sites for di- and tri-vacancy cluster aggregation in a-SiO_2 with maximum binding energies of approximately 0.13 eV and 0.18 eV, respectively. The calculated barriers for neutral O vacancy diffusion range between 3.2 eV and 5.6 eV, with the average value about 4.6 eV. This shows that effective clustering of randomly distributed neutral O vacancies via diffusion at room temperature is unfeasible. When the system's Fermi level is above 6.4 eV with respect to the top of the SiO_2 valence band, oxygen vacancies can trap up to two extra electrons from Si substrate or metal electrode. Average diffusion barriers for doubly charged vacancies are reduced to about 2.0 eV. However, the relatively high probability of losing the trapped electrons into the SiO_2 conduction band strongly reduces the efficiency of this diffusion channel.

These results suggest that clustering of oxygen vacancies in a-SiO_2 via thermally activated diffusion of vacancies is inefficient and that alternative mechanisms for aggregation of O vacancies under electrical bias should be considered. Here one can turn to existing models of SDB and HDB. In particular, according to the thermochemical ***E*** model the generation of defects within the dielectric is caused by weakening of the inter-atomic bonds due to the interaction with an external electric field[196,197]. The probability of breaking a Si-O bond depends exponentially on the bond strength, ΔH_0, as well as on the strength of the field, ***E***. Increasing the latter lowers the energy barrier for bond breaking and creating a stable pair of defects in the amorphous network. The thermochemical ***E*** model predicts an exponential dependence of time to breakdown on the field strength ***E***. Although this behavior has been observed experimentally in thin dielectric films at low stress voltages, the ***E***-model does not explain the field polarity dependence of dielectric breakdown. The experimental results also show different breakdown times for the same field in devices of different dielectric

thicknesses[198]. Describing oxide degradation as a purely field driven process is therefore an over-simplification[199] .

More recent results suggest that the generally accepted time-dependent DB (TDDB) observations can be better explained when field-induced polar bond weakening is facilitated by current-induced processes in the dielectric[197]. However, the products of bond breaking in an oxide film are difficult to detect directly. Recent experiments combining *in situ* electrical biasing measurements with residual gas analysis using a secondary ion mass spectrometer revealed the ejection of oxygen molecules from a TiN/a-SiO_x/TiN stack[1]. Furthermore, surface deformation of the top electrode correlated with oxygen ejection has been observed using atomic force microscopy (AFM) and transmission electron microscopy (TEM) measurements. The occurrence of such deformations in titanium and silicon oxides[24, 200] has been attributed to oxygen gas emission. The detection of oxygen emission during electrical stressing shows that mobile interstitial oxygen is produced in the film. However, the mechanism of oxygen generation is still poorly understood due to the luck of experimental data and atomistic modelling.

A mechanism proposed in [37] suggests that oxygen vacancy aggregation and oxygen gas generation can be facilitated by electron injection into the oxide from an electrode during electrical stress. It has been demonstrated recently that extra electrons injected into a-SiO_2 can be trapped at intrinsic sites in a-SiO_2 network and create deep states in the band gap[201]. These intrinsic trapping sites are formed by wide O-Si-O angles (>132^o) in the otherwise continuous random network and can accommodate up to two electrons, accompanied by strong network distortion. The structure, optical absorption and EPR signatures of these intrinsic electron traps are described in refs. 1, 201 and 202. As a result of trapping two electrons, the energy barrier to break one of the Si-O bonds adjacent to the trap is lowered to

around 0.7 eV on average, with barriers in some locations being as low as 0.4 eV[37]. Electrical stress can reduce this barrier even further, leading to the formation of a pair of neutral O vacancy, V_O^0, and negatively charged interstitial O^{2-} ion. Unlike other types of defect pairs, e.g. V_O^{2+} and O^{2-} interstitial ions, neutral V_O^0 and negatively charged O^{2-} ions created by this mechanism cannot recombine easily as V_O^0 is occupied by two electrons. After they separate, interstitial O^{2-} ions can diffuse in a-SiO_2 by an efficient pivot mechanism[1] characterized by a low energy barrier of about 0.3 eV, and drift in the electric field towards a positive electrode. This mechanism is illustrated in **Figure 7 (1-3)**. It can explain the formation of both V_O^0, required to support electron current through the a-SiO_2 film, and mobile O ions. However, a more detailed understanding of the mechanism of O_2 gas release observed experimentally[1] requires further analysis of the interaction of O^{2-} ions with the top electrode and oxygen diffusion through the electrode, which is still missing.

Thus the key component of this mechanism is the electron trapping at intrinsic trapping sites in a-SiO_2, which are absent in crystalline SiO_2. The concentration of these sites in a-SiO_2 has been estimated at about 4×10^{19} cm^{-3} [201]. To further relate this mechanism to HDB and electroforming processes one needs to demonstrate that it can explain the growth of leakage current and eventual catastrophic breakdown process and predict the experimentally observed voltage and temperature dependence of time to DB. Calculations [203] have demonstrated that neutral O vacancies can support electron transport via TAT through the oxide. Further simulations [204] have demonstrated that they can be responsible for TAT and leakage current in the SiO_2 and SiO_2/HfO_2 gate dielectric stacks. The HDB mechanism of thin a-SiO_2 films based on creation of V_O^0 caused by electron injection under electrical stress and electron current through the oxide via TAT has been explored in ref. 205. This work developed a multiscale model that combines the atomistic mechanisms of O vacancy generation described above with the electron transport models through an oxide film, including direct tunneling,

defect assisted tunneling in the framework of the multi-phonon TAT model [204], and carrier drift across either the conduction/valence bands or defect sub-bands. The TDDB distributions were simulated at different stress voltages. The basic events leading to initial oxide degradation are shown schematically in **Figure 7**.

Wide O–Si–O bond angle intrinsic electron trapping sites were randomly generated for every simulated sample with a uniform spatial distribution and described by the energy parameters within the ranges reported in refs. 37, 203 and 204. Initially, the electrons injected into the a-SiO_2 film are trapped at intrinsic trapping sites in the film and new defects are generated almost uniformly across the oxide volume. Due to the local perturbation of the electric field induced by their charge state, the probability of generating V_O^0 is slightly higher close to the pre-existing ones. Electron transport through TAT mechanism increases as more new vacancies are generated. This, in turn, causes power dissipation and local temperature increases. The temperature increase further enhances the defect generation rate in the proximity of the higher temperature oxide regions. This process culminates in the random formation of a dominant V_O^0 cluster (comprised of around 25 vacancies with a mutual distance of no more than 0.6 nm) leading to a substantial increase of the local power dissipation, and a temperature increase of 20K. Enhanced defect generation in the surroundings of the hot spot triggers a thermally driven positive feedback between current, temperature, and V_O^0 generation rates that quickly leads to the creation of a breakdown spot formed at a highly oxygen deficient region. This results in the current runaway, which can be controlled only by limiting the maximum current flowing through the film, i.e., the current compliance, as is common for electroforming in ReRAM devices. The good agreement with the experimentally observed time to breakdown dependence on applied bias obtained in simulations [205] supports the atomistic mechanism of V_O^0 generation described above.

A more accurate model accounting for correlation in defect creation, i.e. processes by which pre-existing vacancies affect the formation of new vacancies was suggested in [206]. This is particularly important for the reduced samples used in refs. 22 and 1. The cost of creating an oxygen vacancy depends greatly on the local environment. Not only is there a spread of formation energies owing to disorder, but pre-existing vacancies can affect both the position and the barrier for forming a new vacancy. This mechanism is shown schematically in **Figure 7**. It can explain why electroforming in strongly reduced SiO_x films is much more efficient than in high quality thermal oxide films: the probability of creating new O vacancies near pre-existing vacancies upon electron trapping is higher than in pristine structure.

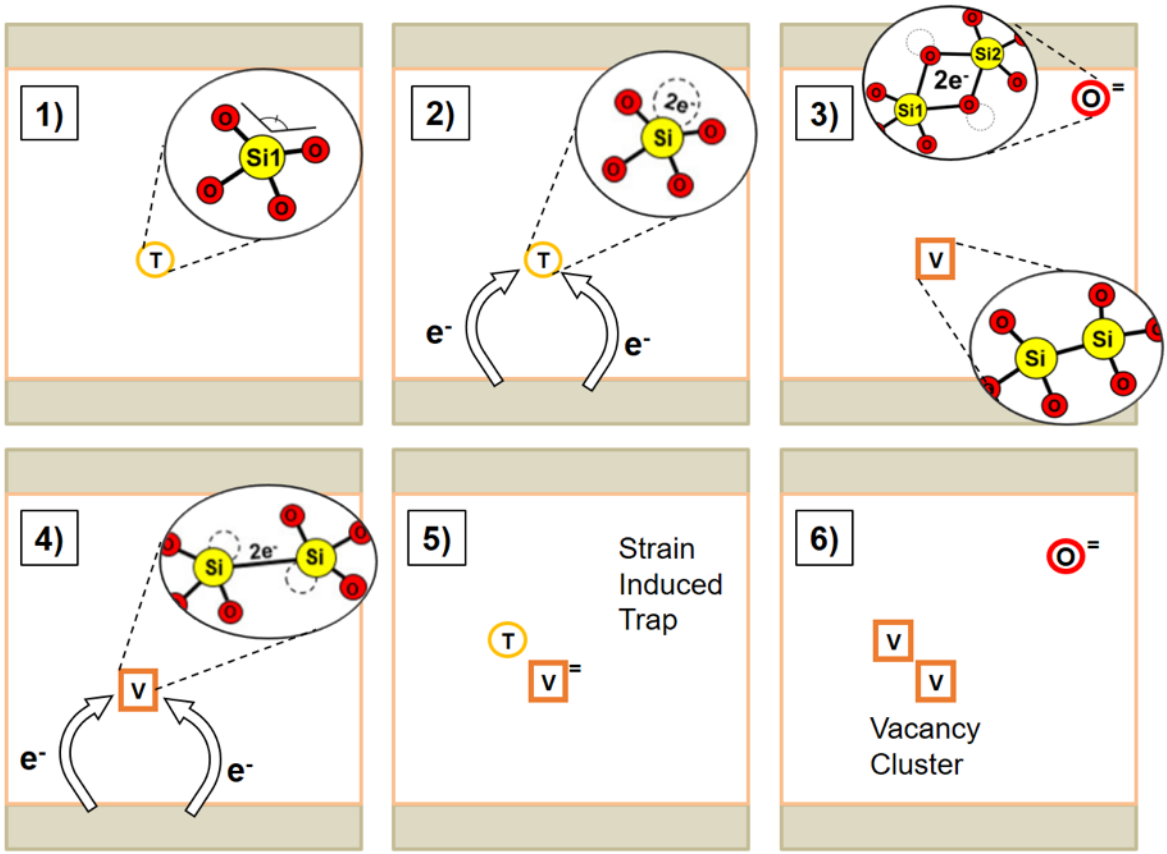

Figure 7. A schematic of the electron injection facilitated defect creation mechanism in a-SiO_2. (1) Naturally occurring wide O-Si-O angles can act as electron traps in the amorphous structure. (2) The intrinsic trap (T) captures two electrons from the substrate, reducing the barrier for forming Frenkel defects. (3) A neutral O vacancy (V) and a rapidly diffusing O^{2-} ion are formed. (4) Two electrons can trap on the newly created O vacancy. (5) The strain resulting from this a new intrinsic trap. (6) Another O vacancy and interstitial O^{2-} ion are formed, resulting in a di-vacancy. Further electron trapping results in the formation of more O vacancies nearby.

4.3 Circuit models of resistance switching

Besides physical models for stable filamentary conduction in SiO_x, the transitions HRS↔LRS typical of resistance switching devices have also captured the attention of the circuit modeling community. Applications for both the analog[31, 207] and digital[208,209] worlds have been presented. The use of SiO_x for selector devices in crossbar-type configurations has also raised significant interest[80]. To our knowledge, there is no specific circuit model for SiO_x since the existing models are general and interchangeable for a wide variety of materials. As such these models do not attempt to deal with the physics of the device at the microscopic level, but deal with the implementation of dynamical behaviors. In order to include physical considerations, the model needs to be edited and addressed to the particular features of the system under study. In what follows, we will only refer to bipolar resistance switching devices, but the discussion can be extended to unipolar devices as well.

The hysteretic loop in the *I-V* characteristic of thin oxides has been interpreted in the last years in terms of memristors or memristive systems. Leon Chua proposed in 1971 the corresponding theory. Basically, Chua's theory links charge and flux linkage through a new circuit element called memristance [210, 211] . This is a resistor with memory. The theory was extended to ReRAMs in 2011[212]. Memristive devices are two-terminal structures whose behavior is determined by two coupled equations: one for the electron transport (short response time) and one for the displacement of atomic species within the device (long response time) [213,214,215]. The first equation is often expressed as an Ohmic-type relationship between voltage and current and the second equation is generally written as an incremental relationship for an internal parameter or state variable. Strukov's [216] model for the dopant drift in TiO_2 layers represented a breakthrough in this field. The model has been widely explored[217,218], but requires the introduction of additional constraints in the memory

equation: the so-called window functions[213,219, 220]. Concerning equivalent circuit modeling, Szot *et al.*[221] attributed the LRS-HRS transitions to a change in the transmission properties of dislocations. According to Szot's model the switching process is basically a consequence of the local modulation of the oxygen content in the material. The electrical behavior of such system is compatible with a network formed by resistors and diodes. Yang *et al.*[222] also considered equivalent circuit modeling. The hysteretic *I-V* characteristics are modelled using memristors and rectifying structures that define a family of reconfigurable circuit elements[223]. The device behavior is explained in terms of changes in the potential barrier heights at the metal/dielectric interfaces caused by the field-induced displacement of oxygen vacancies. Borghetti *et al.*[224] considered linear conduction for LRS and exponential conduction for HRS. HRS was ascribed to a tunneling mechanism and the switching to changes in the concentration of vacancies in the gap region. Pickett *et al.*[225] considered modifications of the tunneling barrier width. Hur *et al.*[226] proposed a modulation of a Schottky barrier originated in the movement of oxygen vacancies. Miranda *et al.*[227] have also considered diode-like conduction in combination with the hysteron structure for the memory state (see **Figure 8**). The memdiode model was recently written for circuit simulation environments such as LTspice[228] and is able to represent the intermediate states exhibited by many RS devices.

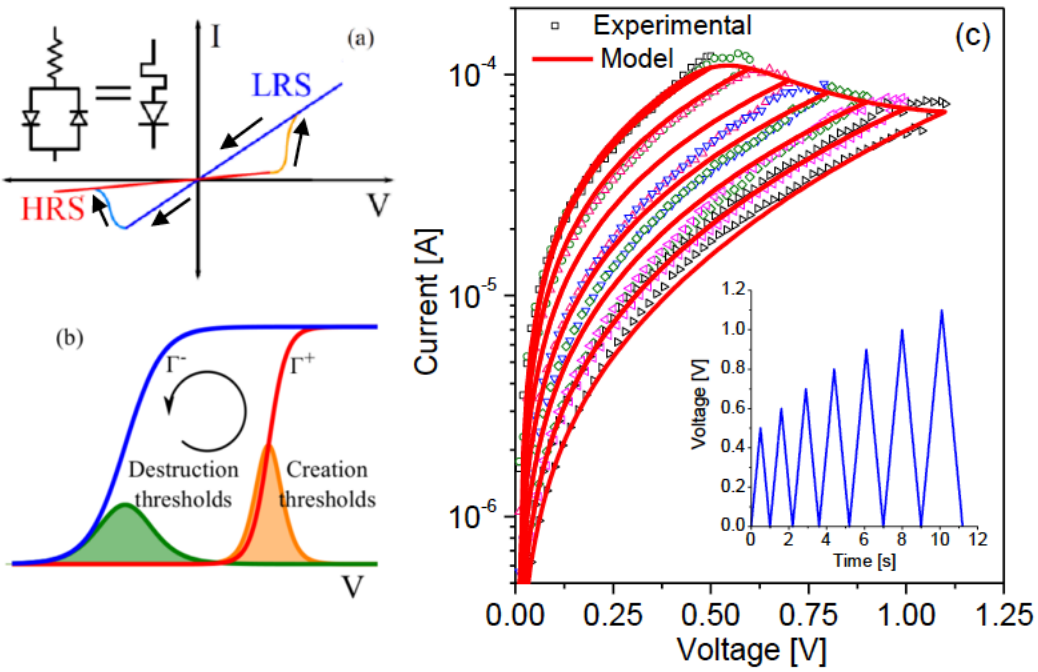

Figure 8. a) The memdiode model consists of two opposite biased diodes and a single series resistance. b)The model parameters are driven by a hysteron map that accounts for the creation and destruction of conducting channels. c) This figure shows some experimental and simulation results for the reset characteristics of SiOx using the memdiode model. Notice the control of the intermediate memory states. The inset shows the input signal. The devices were fabricated at UCL.

Interestingly, the HRS current in electroformed devices is often described using a *sinh(x)* dependence. This specific dependence with the applied voltage is consistent with the pinched current loops, with the symmetry of the *I-V* characteristics for opposite voltages, with the Ohmic-type behavior at low applied voltages, and with the exponential dependence at large applied voltages. In many cases, this choice was mainly motivated for practical reasons[221, 229]. A physics-based explanation was first given by Simmons and Verderber[230]. Guan *et al.*[231] also considered a *sinh*(*x*) expression for their tunneling model with variable barrier width. Finally, it is worth pointing out that the quantum point-contact (QPC) model [232] has also been used to model the resistance switching effect. The approach is consistent with a *sinh(x)* dependence too. In this case, the barrier height or width is used as the state variable of the model.

5. Comparison of silicon oxide ReRAMs to metal oxide ReRAMs (e.g. HfO_2)

Our opening contention was that silicon oxide offers some advantages as a resistance switching material over competing, mainly transition metal oxide, systems.

Given the large band gap and high resistivity of SiO_2, ReRAM devices based on this material usually benefit from a relatively high resistance of the high resistance state (HRS), and a relatively large resistance window, compared to other metal oxide ReRAM technologies (see Table 1). In this section, we will compare SiO_2-based ReRAM devices and HfO_2-based ReRAM devices in more detail, because these two material systems have the most complete comparitive data. In the HfO_2 ReRAM device, the Si-doped HfO_2 dielectric layer was deposited in an amorphous phase on top of a TiN bottom electrode. The bottom electrode size was 40 nm, and the HfO_2 thickness was 10 nm[233]. In the SiO_x ReRAM device, the 3-nm thick SiO_x layer was deposited by e-beam evaporation on a C-based bottom electrode of 70 nm size. In both cases, Ti electrode are used. We make a comparison between devices without discussing the switching mechanism in detail, but rather as viable technologies. However, we note that the two types of device have very similar structures. Although, in most cases, only Ag and Cu electrodes are considered as electrochemically diffusive, we cannot dismiss the diffusion of Ti in this case, as even platinum group metals have been reported to diffuse in sputtered SiO_x[234]. **Figure 9** shows the measured I-V curves of ReRAM devices based on HfO_2 (a) and SiO_x (b), with x around 1[235,236]. The I-V curves were collected by the application of triangular pulses of positive and negative voltage, while the current was measured by an oscilloscope. The pulse width was t_P = 1 μs and 100 μs for HfO_2 (a) and SiO_x (b), respectively. In both cases, an integrated field effect transistor (FET) was connected to the ReRAM device to limit the maximum current during the set transition, i.e., the compliance current I_C = 50 μA. In both cases, devices were measured after an initial forming operation,

consisting of a positive voltage sweep leading to soft breakdown of the dielectric layer, where the current was limited to the same I_C as in the figure.

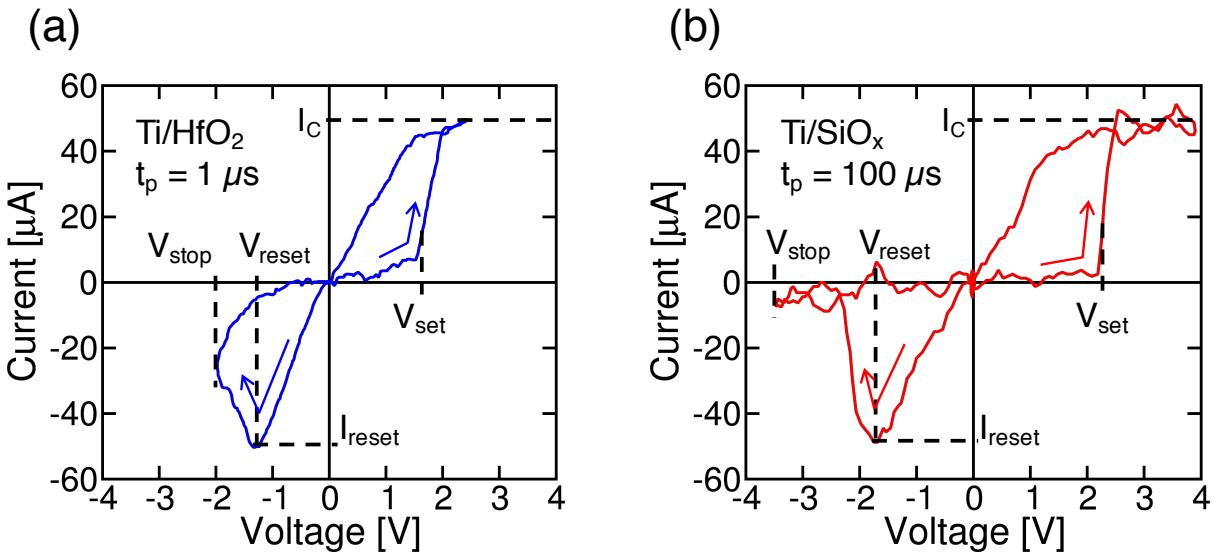

Figure 9. Current-voltage characteristics of the HfO_2 and SiO_x ReRAM devices described in the text. (a) Measured I-V curves of the HfO_2 ReRAM [235] and (b) the SiO_x ReRAM [236]. The two devices show similar set and reset transitions with bipolar switching operation and LRS resistance controlled by the compliance current I_C = 50 μA. However, the SiO_x ReRAM shows a larger resistance window due to the higher resistance of the HRS. Reprinted with permission from [235] and [236]. Copyright IEEE (2014) and (2018).

Both devices show comparable bipolar switching operation, with the exception of the relatively larger resistance of the HRS for SiO_x, and a correspondingly higher set voltage V_{set}, which is slightly higher than 2 V for SiO_x and slightly lower than 2 V for HfO_2. Detailed DC measurements on the same devices confirm that the resistance window is about 1 order of magnitude for HfO_2[237], compared to about 4 orders of magnitude for SiO_x[236]. Such a significant change of the resistance window can be attributed to the larger band gap of the SiO_x dielectric layer and the corresponding high resistivity. On the other hand, the HRS in HfO_2 is severely affected by the first forming operation, where the generation of defects, such as oxygen vacancies, causes the presence of a low-resistivity conductive path across the HfO_2 layer even in the HRS. Negligible degradation seems to take place in the SiO_2 layer, possibly due to the higher temperature stability and stronger bonding between silicon and oxygen in SiO_x. ReRAMs based on other metal oxides, such as TiO_x[238] and TaO_x[239], behave similarly

to HfO_x in this respect, thus evidencing the inherent advantages of SiO_x-based ReRAM with respect to metal oxide technology.

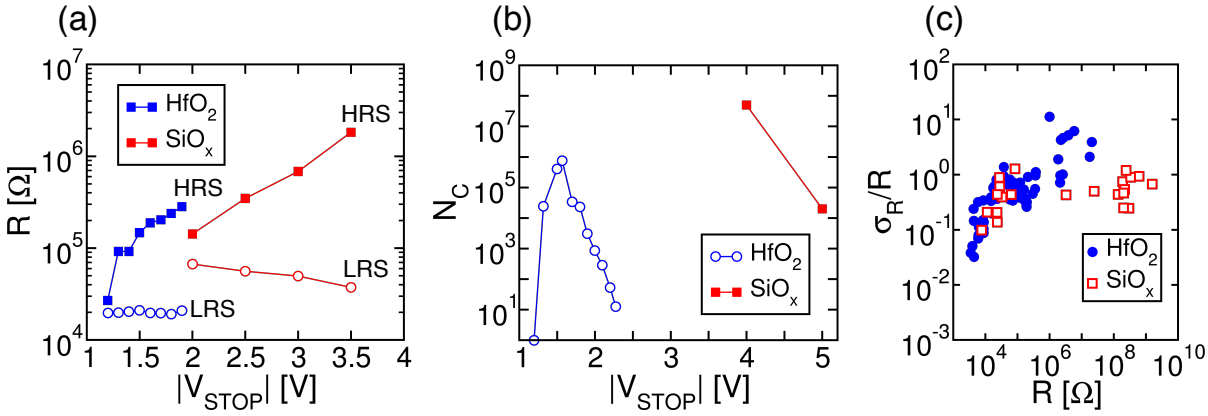

Figure 10. Programming and reliability characteristics of HfO_2 and SiO_x ReRAM devices. a) Measured resistance for the LRS and HRS, b) cycling endurance and c) relative standard deviation σ_R/R for HfO_2 and SiO_x ReRAM devices. SiO_x ReRAM shows higher resistance window, higher endurance, and lower resistance variability compared to HfO_2 ReRAM. Reprinted with permission from [236]. Copyright IEEE (2018).

Figure 10a shows the average resistance for the low resistance state (LRS) and the high resistance state (HRS) for HfO_2 ReRAM[235] and SiO_x ReRAM[236]. Both LRS and HRS were measured under triangular pulse conditions with pulse widths t_P = 1 μs for HfO_2 ReRAM and t_P = 100 μs for SiO_x ReRAM. A compliance current I_C = 50 μA was used for the set transition. Data in the figure are shown as a function of V_{stop}, namely the maximum negative voltage in the reset pulse. Increasing V_{stop} results in a deeper HRS thanks to the gradual reset transition (see e.g., **Figure 9a**), which reflects the increasing depleted width at increasing V_{stop}[240]. As a result, the average value of HRS increases with V_{stop}, thus broadening the resistance window between LRS and HRS. For SiO_x ReRAM, V_{stop} also affects LRS, which decreases at increasing V_{stop} due to the higher average field across the depleted band gap[236]. From data in **Figure 10a**, it appears that SiO_x ReRAM displays a higher resistance window, which reaches about a factor 50 for the maximum V_{stop} considered in the figure, compared to a factor of 15 for the HfO_2 ReRAM in **Figure 10a**.

It should be noted that the value of V_{stop} is larger for SiO_2 than HfO_2, which might be due to the higher energy barrier for defect migration in SiO_2, which thus requires higher Joule heating and a higher electric field to induce a similar migration rate in the two materials. However, it was shown that V_{stop} drives the ReRAM reliability degradation, resulting in window reduction and dielectric breakdown[241]. To study the cycling reliability of the two ReRAM technologies, **Figure 10b** shows the endurance, namely the number of cycles to final failure, as a function of V_{stop} for HfO_2 and SiO_x ReRAM devices. As a general trend, the endurance decreases for increasing V_{stop}, due to the increasing voltage stress affecting the bottom electrode interface[241,242]. The failure event for HfO_2 ReRAM was evaluated as the set process under negative voltage, where the reset process was expected instead[242]. For SiO_x ReRAM, on the other hand, endurance failure was assumed to correspond to window closure below a factor of 2 between the LRS and HRS, the latter resistance decreasing at increasing cycles as a result of the increasing degradation of the SiO_x layer[236]. Data in **Figure 10b** shows that endurance is higher for SiO_x ReRAM, despite the larger V_{stop} in the reset sweep. The larger immunity to stress and the greater endurance can be attributed to the strong covalent bond in SiO_2 and to the inert nature of the graphitic carbon used as bottom electrode in the silicon oxide ReRAM[236] described here. In fact, the negative set that indicates endurance failure is generally due to a breakdown of the bottom electrode interface, resulting in an injection of electrode atoms from the bottom electrode. Therefore, to prevent negative set and improve the cycling endurance in ReRAM technology, it is recommended to adopt inert bottom electrode materials such as carbon[236], Pt[243] and Ru[244].

The higher immunity to voltage stress is also reflected by a greater stability of the SiO_2 ReRAM devices against high temperature annealing. In general, ReRAM devices suffer from resistance changes in both LRS and HRS due to temperature-induced rediffusion of defects, causing disruption of the conductive filament in the LRS, or closure of the depleted gap in the HRS, both resulting in a variation of the resistance[245]. Size dependent retention effects were

demonstrated in unipolar switching NiO ReRAM devices[246] and bipolar switching GdO_x devices[247]. Here, LRS shows decreasing retention time for increasing resistance, as a result of the thinner conductive filament and the consequently weaker stability against atomic diffusion. From this respect, SiO_2 ReRAM shows relatively good stability at elevated temperature, e.g., LRS programmed at various resistance between 10 kΩ and 100 kΩ showed negligible resistance variation up to 260°C for 1 hour, suggesting no significant size-dependent resistance loss[236]. On the other hand, the LRS resistance was shown to increase by about a factor of 5 after 1 hour at 250°C in HfO_2 ReRAM[245]. Also, random variations of resistance can affect HfO_2 ReRAM even at room temperature[248], resulting in distribution broadening and consequent retention loss[249].

Another strong requirement for memory reliability is the switching uniformity against device-to-device and cycle-to-cycle variations, which are known to affect ReRAM and constitute a serious challenge in the development of large size arrays[250]. Cycle-to-cycle variability is generally assessed by the standard deviation of resistance, σ_R, divided by the average value of resistance R, namely σ_R/R[237], which is shown in **Figure 10c** as a function of R for SiO_x ReRAM and HfO_2 ReRAM for both LRS and HRS[236]. Different LRS and HRS states were obtained by changing the programming conditions, e.g., I_C during set process or V_{stop} during the reset process. Data show that resistance variations are comparable for the two ReRAM technologies in LRS, indicating that Ti migration might be responsible for resistance switching in both cases. The variability is controlled by the shape variation of the CF[251]. On the other hand, HRS variation is much lower in SiO_2 ReRAM compared to HfO_2 ReRAM. The lower variability, combined with the higher resistance window of SiO_2 and the better immunity to temperature and voltage stress, makes SiO_2 a promising material for ReRAM compared to conventional ReRAM technologies based on metal oxides.

6. Fabrication, system integration and CMOS compatibility

We now discuss state-of-the-art work on the fabrication of SiO_x resistance switching crossbar arrays.

6.1. Sneak path problem of crossbar devices

One major advantage of resistance switching devices (or memristors) is their high integration density, which is a crucial requirement for high capacity memories and large scale neuromorphic computing units. The high density comes from not only the great two-dimensional (2D) scalability of individual devices, but also from the fact that the devices can be stacked into three-dimensional (3D) crossbar arrays. However, the low resistance state of most silicon oxide based resistance switching devices has a fairly linear current-voltage (IV) relation, which will cause sneak path problems that prevent correct reading and programming in a crossbar. This issue must be eliminated for an integrated array to be useful for various applications. The following sections introduces recent efforts in integrating silicon oxide based devices to 2D and 3D crossbar arrays.

6.2. Schottky diode and pn junction selectors

One solution to suppress the sneak path current is to make the IV characteristic of the device cells in the array highly nonlinear (rectifying). This can be done by either integrating a nonlinear selector device or engineering the nonlinearity in the device cell. Wang et al[252] integrated Schottky diodes as selector devices to build a functional 1 kbit (32×32) SiO_x memristor crossbar array. The memristor is composed of Pd electrodes, and e-beam evaporated SiOx as the switching layer. The Schottky contact in the integrated diode is formed between the deposited Al layer and the p-typed doped Si layer on a silicon-on-insulator (SOI) wafer. The effectiveness of the integrated Schottky diode is experimentally proved by reading a high resistance cell in a 2×2 array, and programming eight ASCII code within the 1 kbit array. Ji et al[253] further employed p-n junction diodes for lower reverse-bias

leakage currents and higher breakdown voltages. The silicon oxide resistive switching layer is deposited on a $p^{++}/n^{+}/n^{++}$ epitaxial Si wafer, which forms the p-n junction diodes. During the measurement, the tungsten probe tip contacting with the nanosphere lithography patterned pillars is used as the top electrode. The individual devices showed good performance, especially in terms of rectifying ratio, which enables a 1 Gbit array from simulation of integrated one-diode-one-resistance switch (1D1R) arrays.

6.3. Room temperature single crystal Si membrane transfer

In order to stack the crossbar three-dimensionally, the fabrication process should be controlled within the thermal budge of back-end-of-line (BEOL) to be compatible with the CMOS fabrication process. However, most silicon based selector devices use silicon from the wafer substrate, and are thus not 3D stackable. Li et al[31] developed a fluid-supported method to stack the single crystalline silicon layers at room temperature to build 3D memristor crossbars. The doped silicon layer is released from an SOI wafer by etching away the buried oxide (BOX) with hydrofluoric (HF) acid through the patterned holes, and transferred to another wafer. The HF etching step also makes the silicon surface hydrophobic, which further facilitates the silicon release process and allows the silicon membrane to float on deionized (DI) water. The processes are at room temperature and the result shows good fabrication yield. **Figure 11** shows a released 0.75 cm × 0.75cm square shaped silicon membrane floating on DI water surface; it may subsequently be picked up.

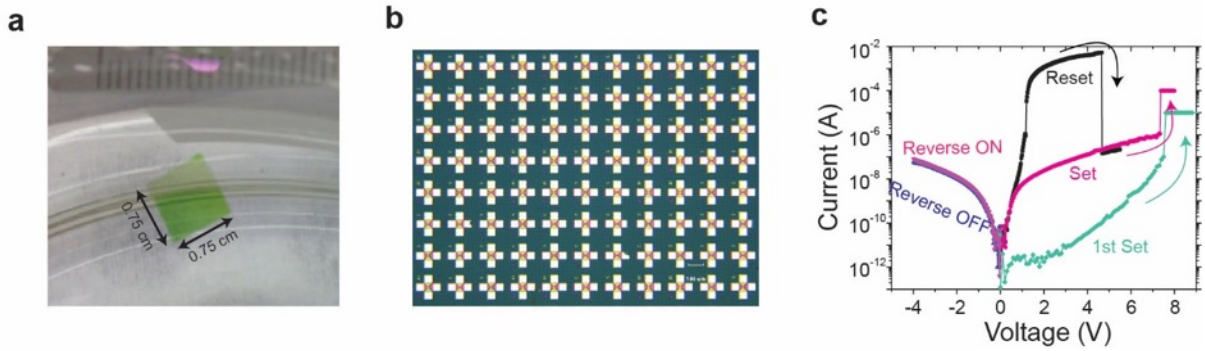

Figure 11. (a) A freestanding 0.75 cm×0.75 cm single-crystalline silicon membrane floating on DI water in a beaker. The membrane is to be transferred to another wafer for use as memristor electrodes. (b) Top view of a 11×8 array of single cross point devices with high fabrication yield. Scale bar, 100 μm. (c) A typical unipolar resistance switching curve with a built-in diode. The set voltage is around 7.5 V while the reset voltage is 4.5 V. The first set voltage is close to that for subsequent sets, suggesting it is forming-free. The reverse current (when negative voltage is applied on the top electrode) is suppressed compared to the forward current. Reproduced with permission[31]. Reproduced under the terms of the CC-BY-4.0 license.[31] Copyright 2018, The Authors.

6.4. p-Si/SiO_2/n-Si devices

The room temperature silicon transfer technique has been used to build 3D memristor crossbar arrays. After transferring the first layer of silicon as the bottom electrode, an approximately 5 nm thick silicon oxide film is produced as the switching layer by chemical (Piranha solution) [254] and plasma (O_2) treatment. The top electrode is fabricated by transferring and patterning another layer of silicon membrane. The fabrication result of one 5 μm × 5 μm Si/SiO_2/Si memristor is shown in **Figure 11b**. By using different types of dopants for the bottom and top electrodes, the device exhibits self-rectifying unipolar switching behaviour, as shown in **Figure 11c**. The reverse biased current is suppressed by the built-in diode regardless of the device resistance state. This self-rectifying characteristic is attributed to a silicon-rich oxygen-deficient conduction channel in the low resistance state that forms a p-i-n like built-in diode with the electrodes. The ON/OFF resistance ratio and self-rectifying ratio is sufficiently large to support large crossbar arrays (e.g. 1024 × 1024 with 1 Ω wire resistance per cell) according to our simulation using a SPICE model based on measured device data. The array performance could be further improved by using thicker silicon wires or incorporating low resistivity metals for electrical conduction only.

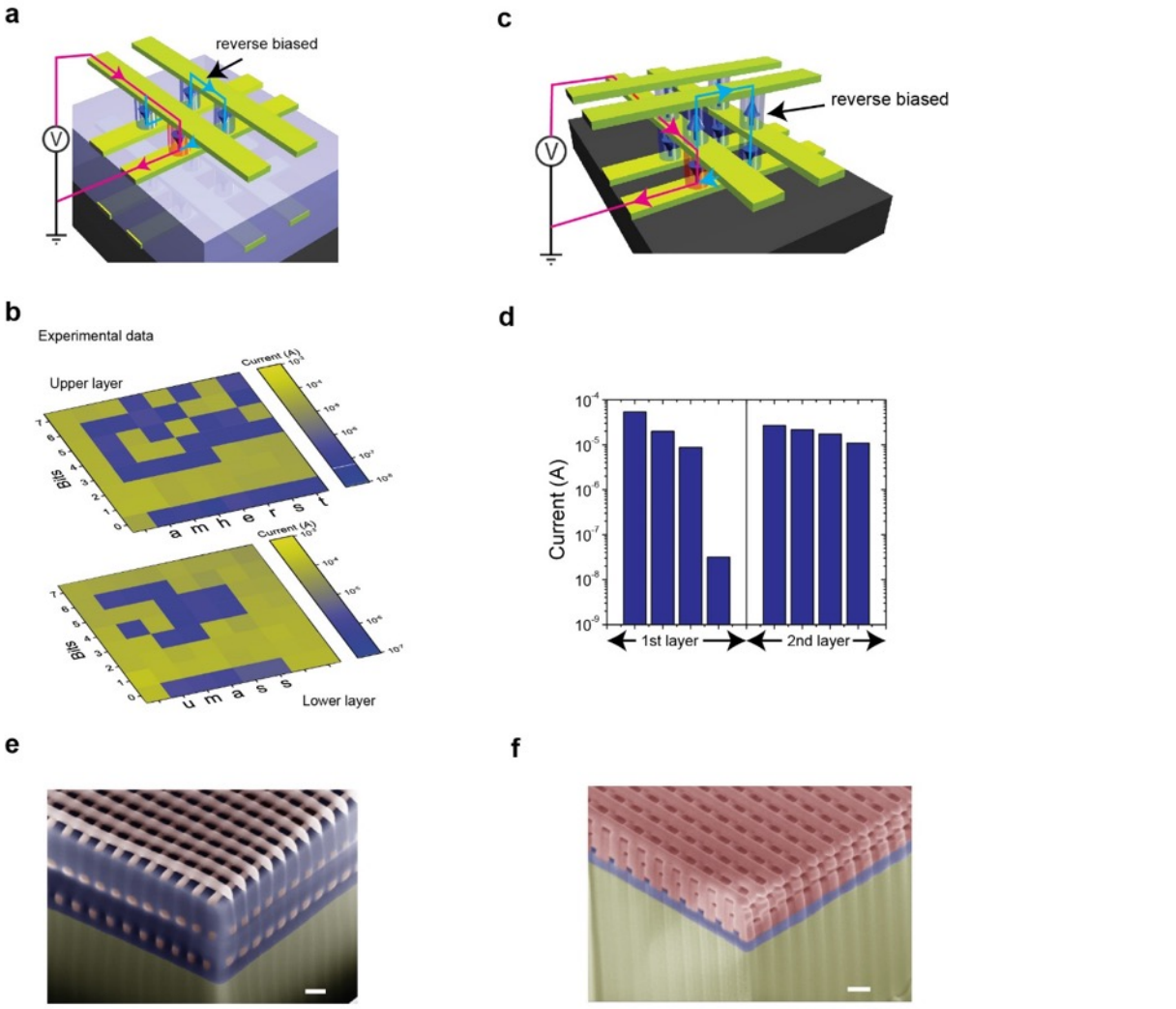

Figure 12. (a) Schematic of the 3D stacked Si/SiO_2/Si memristor crossbar with interlayer dielectric (HSQ) to isolate layers. The built-in diode could block the intralayer sneak path current. (b) The array was programmed to represent the ASCII code for 'umass' and 'amherst', respectively. The unused cells were programmed to the LRS to emulate the worst possible case scenario. The programmed information can be readout successfully, due to the effectiveness of the built-in diode in the device in blocking the sneak path current. (c) Schematic of the 3D stacked Si/SiO_2/Si memristor crossbar with interlayer dielectric (HSQ) to isolate layers. The built-in diode could block the interlayer sneak path current. (d) Experimental results from a 2×2 sub-array show that the only HRS cell in the 1st layer can be read out correctly, even in the worst case scenario of all other cells being in the LRS. This confirms the successful suppression of the inter-layer sneak path current in the array. (e) The six layers of silicon electrode were stacked into three layers of crossbar. Layers of the crossbar are electrically isolated by the spin-on HSQ (shown in blue). Scale bars, 200 nm. Reproduced with permission[31]. Reproduced under the terms of the CC-BY-4.0 license.[31] Copyright 2018, The Authors.

6.5. 3D array stacking

The self-rectifying $Si/SiO_2/Si$ memristors are stacked into two-layer crossbars by repeatedly transferring the silicon layers and electrode patterning, with an HSQ isolation layer in between. A typical sneak path within one layer is illustrated in **Figure 12a** where the cell shown in red is accessed by biasing the corresponding electrode lines and floating all others (the red arrow shows the desired path). With the self-rectifying characteristic from our device, the sneak path current is suppressed by at least one reversed biased built-in diodes along all paths (a typical one is shown in blue). The effectiveness of the suppression is demonstrated by successful reading out of the pre-programmed ASCII codes for 'umass' and 'amherst' from the two layers (**Figure 12b**).

The self-rectifying memristor can also block interlayer sneak paths in a 3D array where the middle electrodes are shared by adjacent layers. **Figure 12c** shows a two-layer crossbar with three layers of electrodes with alternating dopant types (n-p-n). All the memristors in the two-layer crossbar are programmed into the low resistance state except one in the high resistance state. The blue coloured line shows that one interlayer sneak path is blocked by a reverse biased cell, so that the corresponding high resistance state of the device can be correctly read out (**Figure 12d**).

3D crossbars with more layers and nanoscale devices can be fabricated by simply repeating the layer transfer processes and employing advanced patterning techniques. A three-layer stacked crossbar array is fabricated out of six layers transferred silicon membranes with interlayer dielectric isolation (**Figure 12e**). Similarly, a five-layer stacked crossbar array is fabricated out of six layers of transferred membrane with shared electrodes between layers. In this case, the silicon membranes are stacked directly without any interlayer dielectric (**Figure 12f**). Because of the high Young's modulus of the single crystalline silicon, the 70 nm thick silicon nanowires do not bend, and the layers are naturally isolated by the air gap.

7. Summary

Silicon oxide, while being one of the most-studied of all oxides, continues to exhibit novel and rich structural and electrical behaviour under electrical stress. In this review we have summarised recent work that demonstrates the great potential of this most CMOS-compatible of oxides as a resistance switching material. It exhibits a variety of responses – both intrinsic and extrinsic – to electrical stress, which show significant promise for its use in a variety of technologies, from non-volatile memories to neuromorphic devices and systems. Compared to other competing technologies, it offers higher stability, greater resistance contrast, ease of process integration, and the potential to minimise the requirement for cell selector elements. While there remain some challenges ahead to fully realise SiO_x-based ReRAM memory chips or neuromorphic systems, silicon oxide is rapidly emerging as one of, if not the most, suitable contenders in the race to exploit resistance switching technologies.

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Silicon oxide has long played a vital role in semiconductor microelectronics. Recent work, summarised in the review by Mehonic et al, shows how this most CMOS-compatible of oxides is a leading contender in the race to develop resistance switching technologies for non-volatile memories, neuromorphic systems and other exciting applications.

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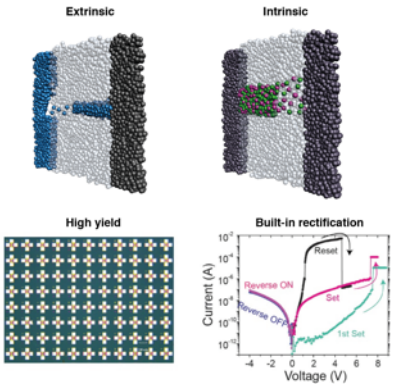
Silicon Oxide (SiO_x) - The Material of Choice for Resistance Switching?



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