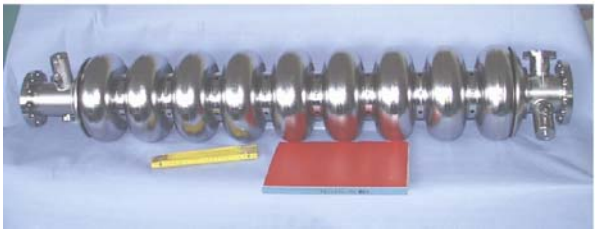

SRF 

# Irradiation Investigations for TESLA and X-FEL experiments at DESY

Dominik Konrad Rybka[a], Arkadiusz Kalicki[a], Krzysztof Pozniak[a], Ryszard Romaniuk[a], Bhaskar Mukherjee[b], Stefan Simrock[c]

[a]*Institute of Electronic Systems, Warsaw Univeristy of Technology*

[b]*Radiation Protection Group, DESY*

[c]*Machine RF Group for Proton Ring Accelerators, DESY*

## Abstract

Electronic components during High Energy Physics experiments are exposed to high level of radiation. Radiation environment causes many problems to electronic devices. This report highlights the major hazards to electronics caused by radiation. Several experiments were done and results are included.

**Keywords:** Irradiation, gamma, neutron, TESLA, X-FEL, LINAC II, DESY, FPGA, TLD, LED, CCD, CMOS

Contribution to the XVIth IEEE-SPIE Wilga Symposium
on Electronics and Photonics for HEP Experiments, May 04, Wilga, Poland

Work supported by the European Community-Research Infrastructure Activity under the FP6 “Structuring the European Research Area” programme (CARE, contract number RII3-CT-2003-506395).

TESLA Report 2004-12

# Irradiation Investigations for TESLA and X-FEL experiments at DESY

Dominik Konrad Rybka[a], Arkadiusz Kalicki[a], Krzysztof Pozniak[a], Ryszard Romaniuk[a], Bhaskar Mukherjee[b], Stefan Simrock[c]

[a]Institute of Electronic Systems, Warsaw Univeristy of Technology
[b]Radiation Protection Group, DESY
[c]Machine RF Group for Proton Ring Accelerators, DESY

## ABSTRACT

Electronic components during High Energy Physics experiments are exposed to high level of radiation. Radiation environment causes many problems to electronic devices.

This report highlights the major hazards to electronics caused by radiation. Several experiments were done and results are included.

**Keywords:** Irradiation, gamma, neutron, TESLA, X-FEL, LINAC II, DESY, FPGA, TLD, LED, CCD, CMOS

## 1. INTRODUCTION

Two new projects TESLA (Tera Electon Volt Superconducting Linear Accelerator) and X-FEL (X-ray Free Electron Laser) are being developed at the DESY (Deutsches Elektronen-Synchrotron) in Hamburg, Germany. These projects are unique because of idea to place control electronic systems in collider tunnel, near superconducting cavities. It may cause many problems in routine work of electronic devices, because of its exposure to a moderate dose of neutron and gamma radiation.

The integrated flux of fast neutrons close to the cryomodule will be of the order of up to $1*10^{12}cm^{-2}/20$ years. The gamma dose rate close to the crymodule cannot exceed 10 rad / hour based on a maximum permitted additional cryo heatload of 0.1 W / $m^2$.

Main problems are due to ionization and displacement damage of semiconductors. This impact of the radiation on the electronic systems could appear as:

- single event upsets
- flipping bits in memory
- total ionizing dose effects
- reduction of life time of electronic components

In this case, there is a need of radiation sensivity investigations of electronic components. These tests should provide the information needed to optimize the design of electronics for TESLA and X-FEL and to minimalize failures during its operation.

For further information:
send correspondence to Dominik Rybka
e-mail: drybka@ntmail.desy.de

The irradiation experiments could be divided into three steps:

1. Radiation level measurements:
   - evaluation of radiation level in LINAC II and to compare with the radiation levels in TESLA and X-FEL
   - undestanding the radiation effects in superconducting linacs and measurements of radiation level in UV-FEL (neutrons, gamma radiation)
2. Investigation of radiation effects on electronic components and circuits - complete systems:
   - determine Single Event Effects (SEEs)
   - determine Total Ionizing Dose (TID) effects
   - determine radiation effects on different types of electronics
   - predict performance and life-time in TESLA and X-FEL tunnels
3. Counter measures:
   - develop radiation mitigation concepts and evaluate their performance in the presence of radiation

## 2. RADIATION EFFECTS ON ELECTRONICS

Radiation causes damages in electronic components. The type and magnitude of these damages depend on irradiation environment. There are three main groups of influence, depending on mechanism and caused effects: [3].

- Total Ionizig Dose (TID):
  Caused by neutrons, protons, heavy particles, gamma. It's degradation and/or failure as a function of ionizing radiation accumulation.
- Single Event Effects (SEE):
  Caused by neutrons. It's relatively instantaneous device upset or destruction (latchup, burnout, gate rupture).
- Displacement damages:
  Caused by heavy and secondary particles. It's the result from particles producing Non Ionizing Energy Loss (NIEL).

### 2.1. Total Ionizing Dose

Ionizing radiation causes electron-hole pairs creation in oxide (see Figure 1). Some of these pairs recombinate, more in the absence of electric field. All remaining electrons, because of their high mobility leave the oxide. Left holes, because of their very low mobility are mostly trapped. As the result there is positive charge trapped in the oxide.

### 2.2. Single Event Effects

Single highly ionizing particle (incident or secondary ion) penetrates through the oxide layer (see Figure 2). It provokes high electron-hole pairs density along its track and transient current across the oxide layer. In the result oxide breakdowns.

There can be different categories of Single Event Effects:

- Non-destructive results:
  - Single Event Upset (SEU) - bit flips in memory

- Single Event Functional Interrupt (SEFI) - SEUs in device control logic (eg. in FPGA: JTAG TAP controller, Select Map interface)
- Single Event Transient (SET) - changes in propagated signal

- Destructive results:
  - Single Event Gate Rupture (SEGR) - gate-to-channel short circuit
  - Single Event Burnout (SEB) - high instantaneous current $->$ junction breakdown
  - Single Event Latch-up (SEL) - Vdd-to-Vss short circuit

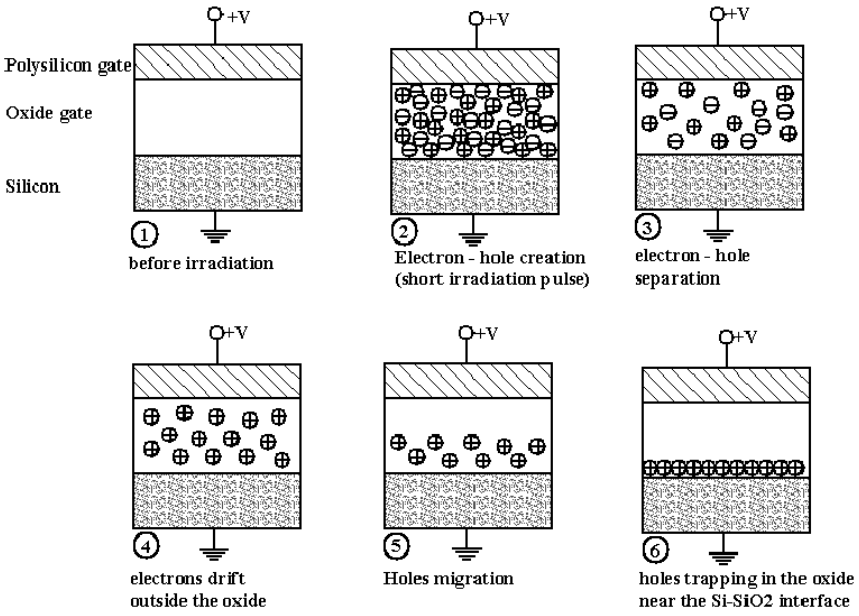



**Figure 1.** Cumulated ionisation example in MOS oxide [3]

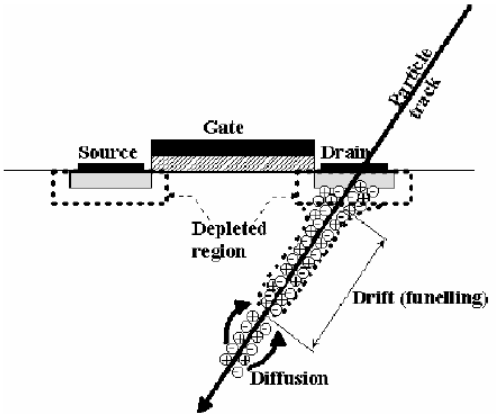



**Figure 2.** Example of Single Event Effect - Single Event Upset [3]

### 2.3. Displacement Damage

Heavy or secondary particle collides with atoms from crystal structure of the semiconductor material. It causes defects in this structure along the track of particle.

The effects of displacement damage could be:

- minority carrier's lifetime decreases
- carrier's mobility decreases
- effective majority carrier's concentration decreases - resistivity increases
- creation of acceptor levels - type inversion (N $->$ P)

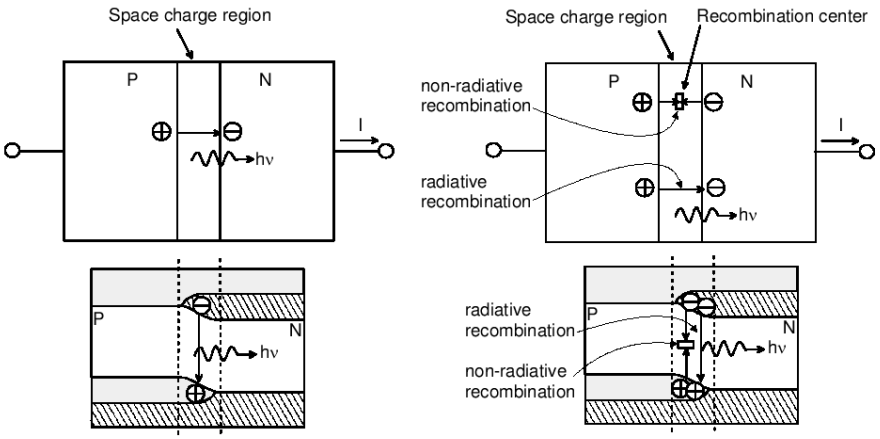



**Figure 3.** Creation of recombination center in P-N junction caused by displacement damage [3]

## 3. IRRADIATION TESTS OF ELECTRONIC COMPONENTS

Because of inaccessibility of TTF-II tunnel, these experiments were carried out in Linac 2 tunnel. The test system and linac itself is described below. It should be mentioned that future tests are planned to be prepared in UV-FEL tunnel.

Some electronic components have been tested:

- Thermo Luminescent Dosimeters (TLD)
- Light Emitting Diodes (LED)
- Charge-Coupled Device (CCD) Cameras
- Field Programmable Gate Array chips (FPGA)

All experiments and the results are presented below.

### 3.1. Linac 2 test system

Linac 2 is DESY's only electron accelerator injecting high energy electrons (450 MeV) to booster synchrotron DESY 2. It consists of two parts (see Figure 4). First one accelerates electrons produced by 150 keV electron source. Electrons with energy about 450 MeV hit the tungsten conversion target and produce electron-positron pairs. There are also neutrons and gamma radiation produced as a parrasitic radiation. The positrons are stored in Positron Intensity Accumulator (PIA), and then delivered to DESY 2, booster synchrotron. [1]

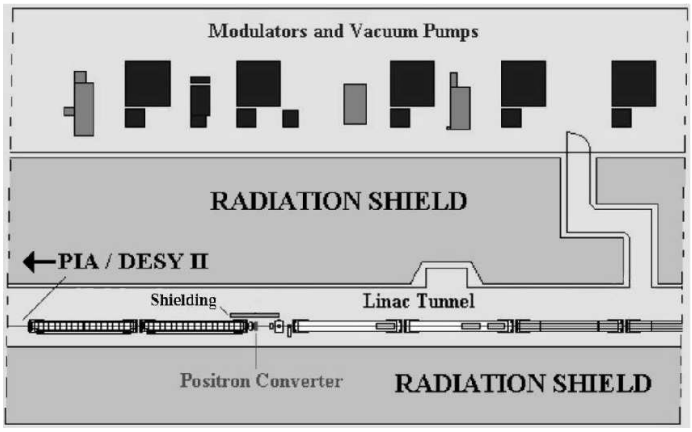



**Figure 4.** Linac 2 tunnel

The radiation environment in Linac 2 tunnel is not well known. The only value which can help quantify it is PIA current. This current coresponds to number of electrons hitting the converter and to parasitic radiation. The accumulated PIA current (PIA charge) corresponds to total neutron and gamma dose.

During the experiments Devices Under Tests (DUT) were placed in various positions along the tunnel (see Figure 4). Changing the distance between the DUT and $e^-/e^+$ converter allows to change radiation level. Its lowest value is near the entry corridor, about 20 meters from the target and the highest near the converter. It should be pointed that electron-positron converter is placed behind the lead shield. This shielding reduces radiation intensity.

### 3.2. Thermo Luminescent Dosimeter irradiation experiments

#### 3.2.1. Introduction

Thermo Luminescent Dosimeter is made of Lithium Fluoride. After exposure, the device is heated to 400 Celssius degrees. This causes them to emit luminescence signal, whereas iths intensity is proportional to radiation exposure. Glow curves of the readout show accummulated radiation dose.

Thermo Luminescent Dosimeter 100 (TLD-100) is mainly sensitive to gamma radiation.

#### 3.2.2. Experiment and results

TLD 100 samples were placed in different positions along the tunnel for 23 hours. The results are shown in the Table 1.

Integrated PIA current during 23 hours of experiment was 76.626 mA.

**Table 1.** TLD results

| Distance from converter [m] | 0 | 0.5 | 1 | 2 | 4 | 8 | 12 | 16 |
|---|---|---|---|---|---|---|---|---|
| Dose [Sv] | 102.3 | 117.9 | 113.0 | 149.0 | 32.5 | 4.9 | 1.9 | 1.2 |

The experiment provides information about irradiation doses along the Linac II tunnel. The doses depend on position of DUT in the accelerator tunnel. The influence of lead shielding is also evident. TLDs placed near the converter (distances: 0, 0.5, 1 meter) but behind the curtain show lower accumulated dose than TLDs placed at 2 meter.

## 3.3. Light Emitting Diodes irradiation experiments

### 3.3.1. Introduction

It's known that neutron flux causes the displacement damage of p-n junction in semiconductors, such as Light Emitting Diodes (LED). Light emitting diodes (LED) suffer irreversible damage after irradiation with fast neutrons. The LEDs exposed to neutrons produce less luminescence light than unexposed (control) LEDs, connected to a constant current source.

### 3.3.2. Experiment

The proposed experiment aims to investigate the radiation damage phenomena of the LED irradiated with accelerator produced neutrons. The chosen LEDs are yellow 3 mm light emitting diodes from Panasonic (LN48YPX). The plan of the experiment is summarized below:

1. Estimation of the light output characteristics of a group of yellow LEDs operated at various input current level.
2. Irradiation of the LEDs with fast neutrons in the available accelerator tunnel at various exposure (dose) levels.
3. Evaluation of the LEDs.
4. Data analysis and estimation of the neutron flux.

Simple instruments including a photometer, constant current power supply, digital multimeter and a custom designed aluminum cup was used in this test (see Figure 5).


**Figure 5.** LEDs test system, consisting of light meter (RS V10860), multimeter (HP 34401A) and power supply (EA-PS 2016-050).

Results for unirradiated LEDs operating various input currents (control reading) shows Figure 6. There were made several irradiation runs. The results - relationship between LEDs relative light attenuation and PIA accumulated current shows Figure 7.

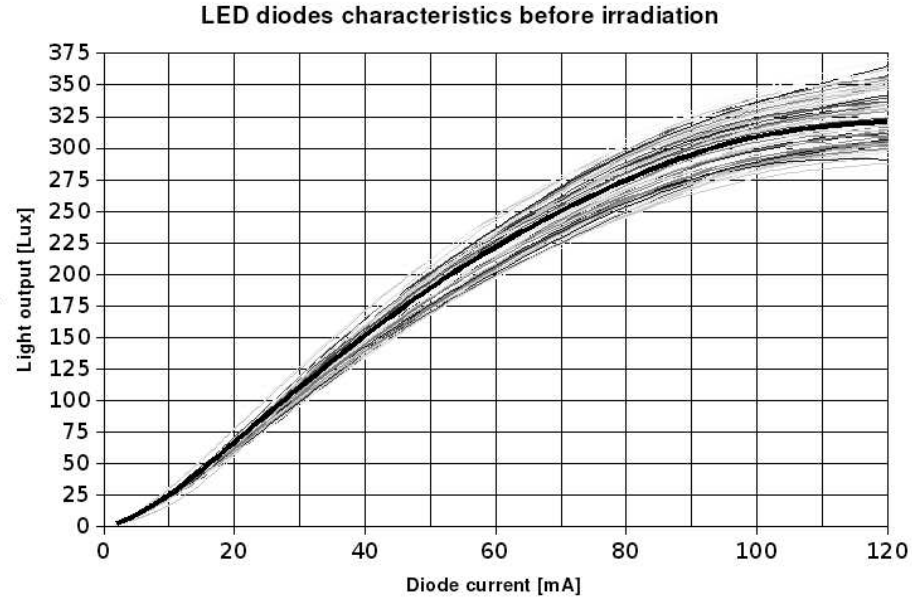



**Figure 6.** LEDs control reading, black bold line shows avarage value

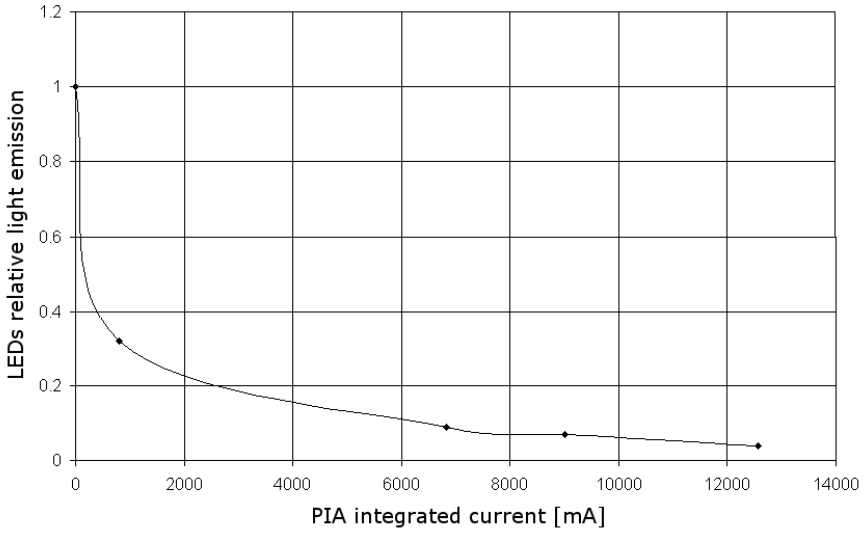



**Figure 7.** LEDs relative light emission as a function of PIA accumulated current, LEDs were evaluated with a forward current of 20 mA

The Figure 7 proves that irradiation destroys p-n junction in light emitting diodes. The light output becomes smaller proportionally to PIA integrated current and to accumulated radiation doses.

### 3.4. CCD sensors irradiation experiments

#### 3.4.1. Introduction

The goal of the experiment was to use Charge Coupled Devices (CCD) sensors as radiation detector. Find dependence between radiation hardness of CCD and total integrated dose and radiation level, also estimate the device lifetime.

CCD was chosen because it is much more sensitive to radiation damage than other types of semiconductor elements. Signal charge packets travel over a much longer path before being registered, and the readout method (moving signal row by row from the image area into the output register, with a subsequent shift in the output register to the output node) increases the time a signal is subject to loss.

Tests took place in Linac II tunnel in DESY Hamburg and show that radiation influence causes two defects: dark current increase and increase of number of hot pixels. Measurements were calibrated with LED diodes tests.

#### 3.4.2. Tests and theory

We tested commercially available CCD and build a model for the radiation damage effects. Structure of a CCD sensor is schematically shown on Figure 8. The epitaxial layer of $\sim 20\mu m$ thick is the sensitive region.

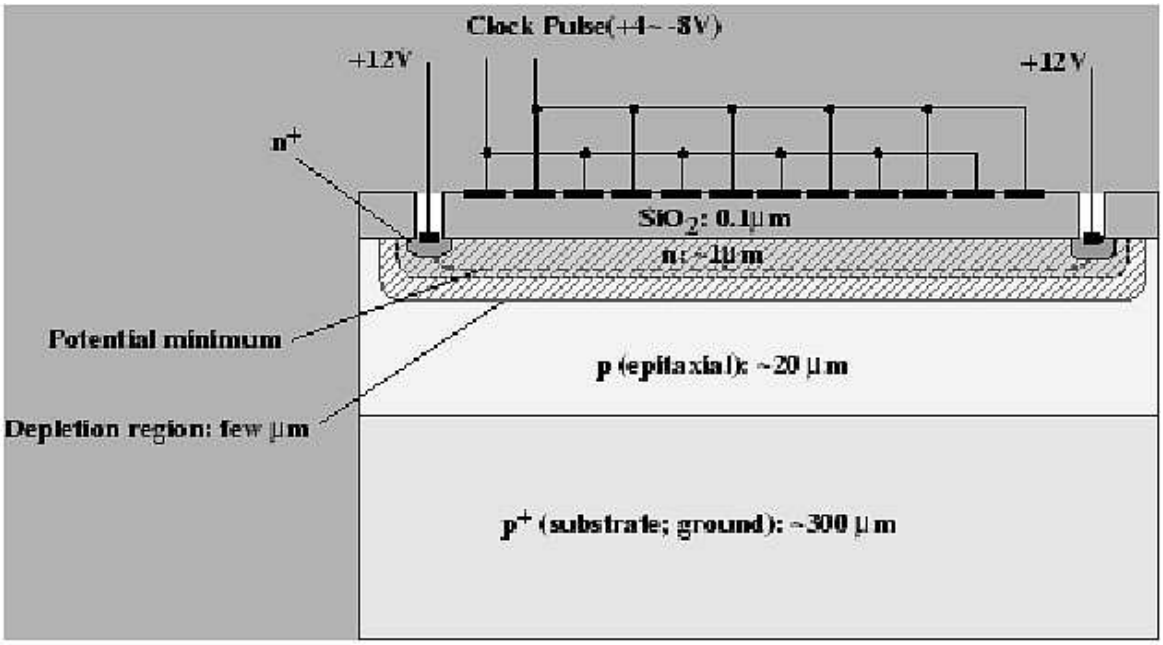



**Figure 8.** Structure of a CCD sensor [7].

Because of the type and the energy spectrum of the radiation, surface and bulk damage effects happen in the CCD sensors. Ionizing radiation creates electron-hole pairs in silicon dioxide, which is used as gate and field dielectric in CCDs. Charge carriers drift in the electric field (externally applied or built-in) to the corresponding electrode. Electrons quickly reach the positive electrode, but some of the holes remain trapped in the oxide and give rise to radiation-induced trapped positive oxide charge, which can be stable for long time. This **surface damage** is dominant source of dark current in CCDs.

High energy radiation can displace Si atoms from their lattice positions, creating displacement damage (**bulk damage**). Low energy electrons and X-rays can deliver only small energy to the Si atom and isolated displacements, or point defects, can be created. But heavier particles, like protons and neutrons can knock out

silicon atoms which can displace other atoms in the crystal. This bulk defects also cause dark current to increase. Irradiation with heavy particles (e.g. protons, neutrons) creates "dark current spikes", also known as "hot pixels" – pixels with much higher dark current than the average value for the CCD (see Figure 9 and Figure 10). Their presence is connected with the high electric fields caused by the device architecture and field-enhanced emission, the cluster nature of the radiation damage and crystal strains in the silicon material [7].

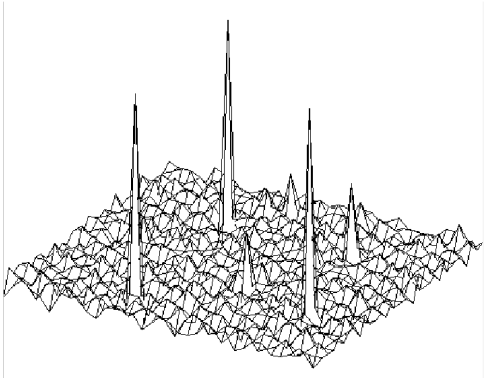


**Figure 9.** Hot pixels 3D.

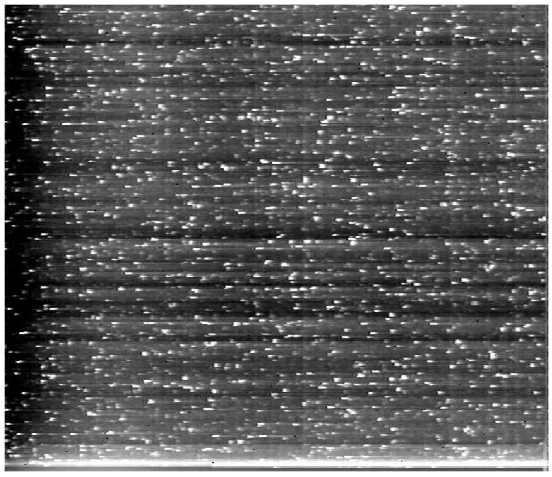


**Figure 10.** Hot pixels image.

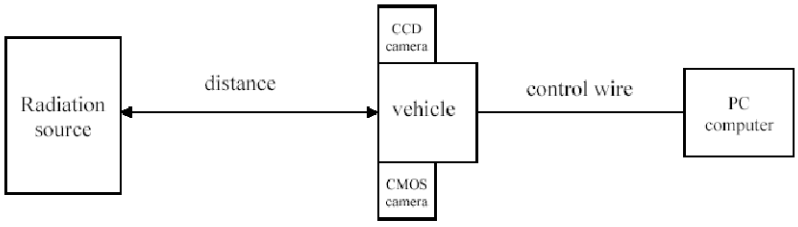



**Figure 11.** Test system.

### 3.4.3. Test system

The test system was build with CCD and CMOS cameras connected to PC with coaxial cable (see Figure 11). Images were taken and processed by PC, radiation level controlled by changing distance to radiation source. The system was remote controlled by TCP/IP network.

Online monitoring software was based on Linux operating system, language C/C++ and TCL/TK, Perl scripts. It used **bttv** module image grabber (**V4L** interface). Algorithm consisted in grabbing image, count and store number of hot pixels:

- grab image (**V4L** interface, **bttv** module image grabber),
- find and count hot pixels (see Figure 9 and 10)
  - multiply image by upper transmit filter (to reduce background) and find local maxims,
  - count hot pixels,
- store the number of hot pixels in database (save selected images),
- switch on, switch off cameras power supply to check if hot pixels are permanent defects,
- finally calculate data in and draw diagrams in **octave**.

### 3.4.4. Experiment and results

- **Number of hot pixels during the experiment**

  One of effects happened by irradiation CCD sensors are hot pixels. To check what dependence is between number of hot pixels and total integrated dose we draw number of hot pixels and integral of PIA current on one Figure 12 and 13. Number of hot pixels rises when there is PIA current – integral of PIA current rise (see Figure 12).

  To check nature of hot pixels we switch on and switch off power supply of CCD sensors (0 hot pixels - camera switched off, Figure 12). The number of hot pixels quickly increases after switch on and stops on permanent level (see Figure 13). This is example of theoretically predicted **bulk damage** and shows that hot pixels are permanent effects.

- **Image histogram, "dark current" during the experiment**

  Other effect happened during irradiation of the CCD sensor is the "dark current" increase. During the experiment we observe that "dark current" increase, maximum of the shape of histogram moves to left and staying wider (see Figure 14 and Figure 15). It confirms theoretically predicted **surface damage**.

- **Number of hot pixels in function of total integrated dose**

  To use CCD sensor as radiation sensor we need to estimate number of hot pixels in function of total integrated dose. We count deltas of number of hot pixels, and then count integral and draw diagram in function of integral PIA current (see Figure 16).

  It seems to be a linear dependence, hence approximated with a first degree polynomial (see Figure 16).

  $$pix = 0.000119 \cdot pia + 0.0332$$

  where: pix - integral deltas of number of hot pixels [percents], pia - integral PIA current

  Calibration with LED diodes shows total integrated dose was:

  $$1.81 \cdot 10^{11} \frac{neutrons}{cm^2}$$

  We can count that dose $0.4 \cdot 10^{11} \frac{neutrons}{cm^2}$ cause increase 0.1 percent of hot pixels.

The measurements show that neutron irradiation of CCD-s with a dose of $2 \cdot 10^{11} \frac{neutrons}{cm^2}$ creates noticeable effects on the CCD. The increase of number of hot pixels can be approximated as linear function of integrated dose. It allows use CCD sensors as low-cost radiation detector.

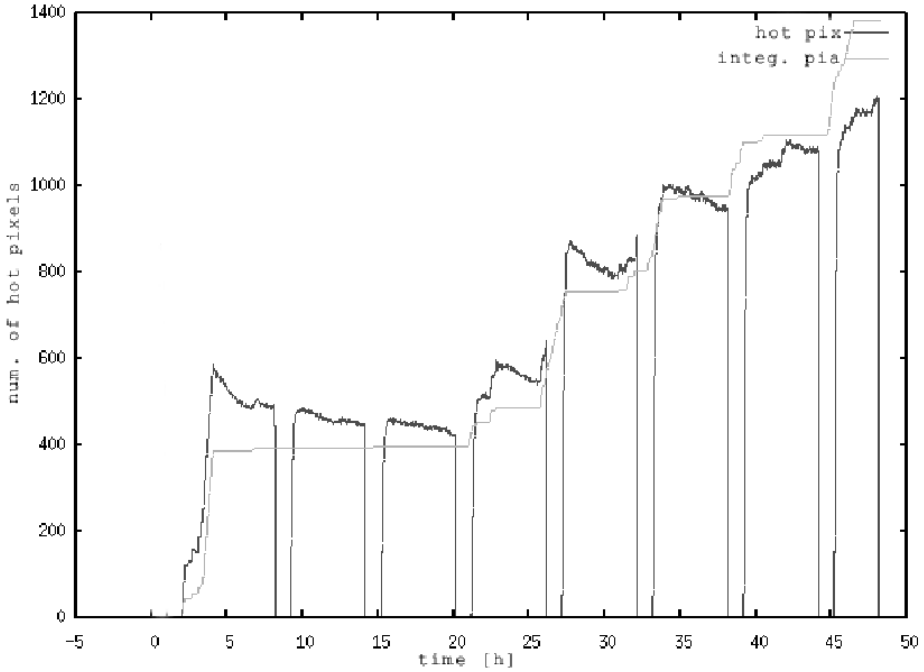



**Figure 12.** Number of hot pixels on CCD camera and integral of PIA current.

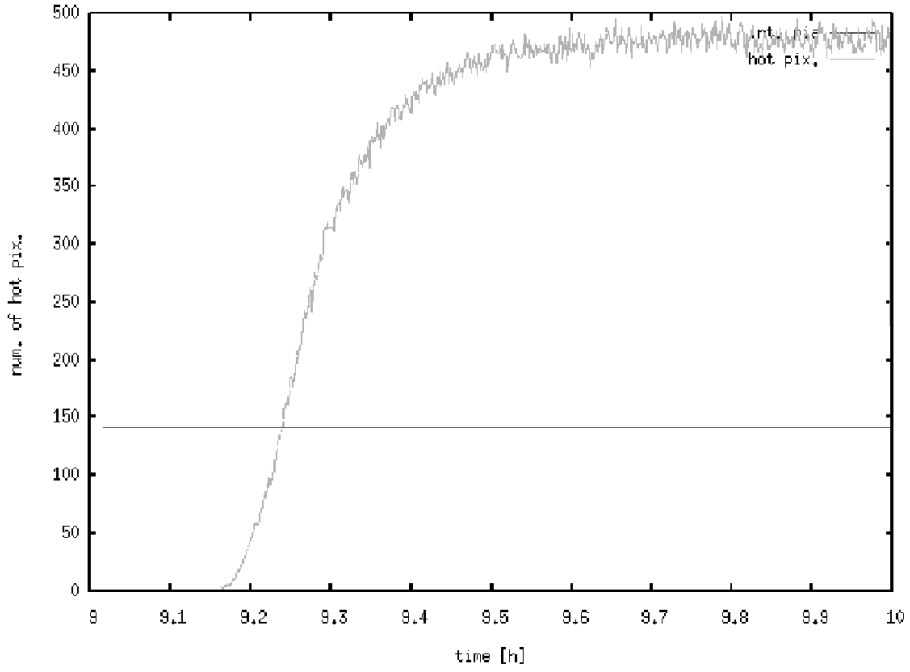



**Figure 13.** Number of hot pixels on CCD camera after "power on", no PIA current.

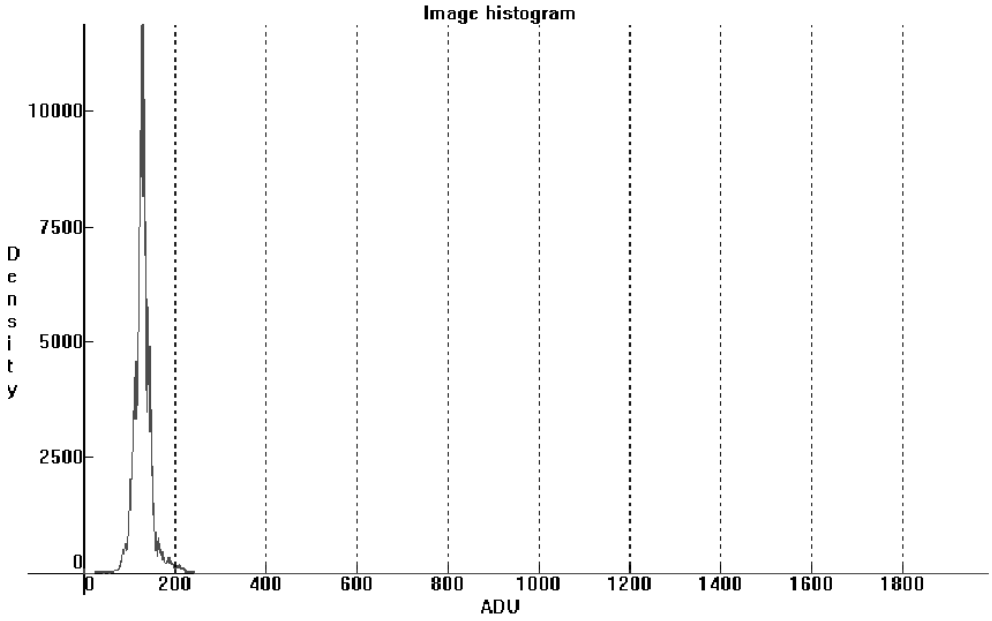



**Figure 14.** Histogram of CCD signal output after 3.5 hours.

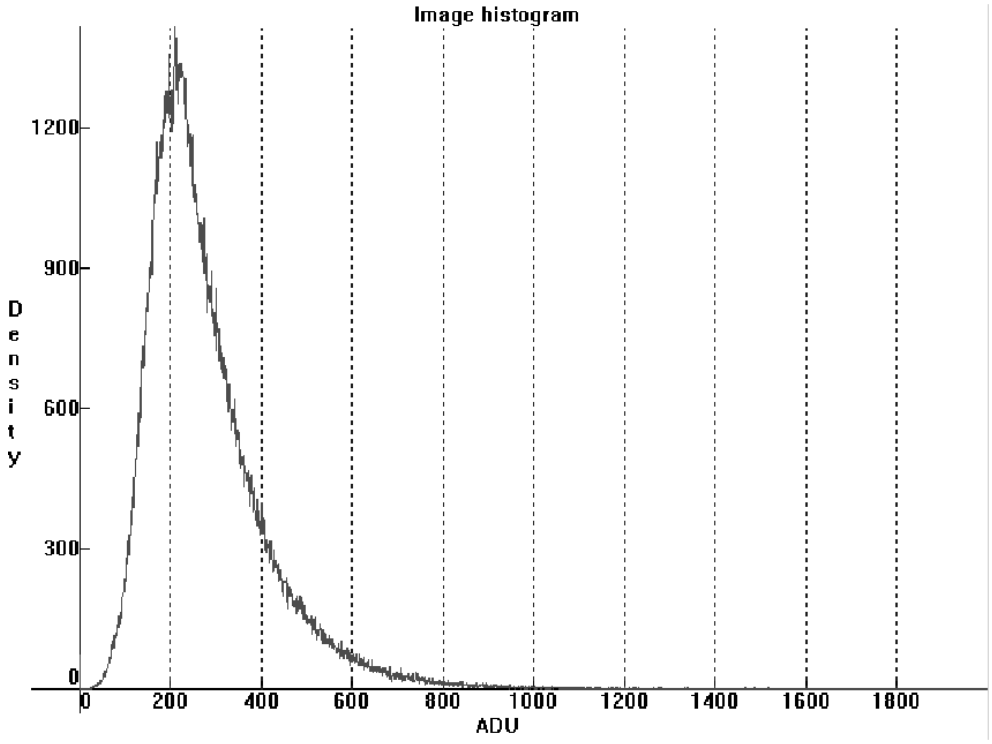



**Figure 15.** Histogram of CCD signal output after 9 days.

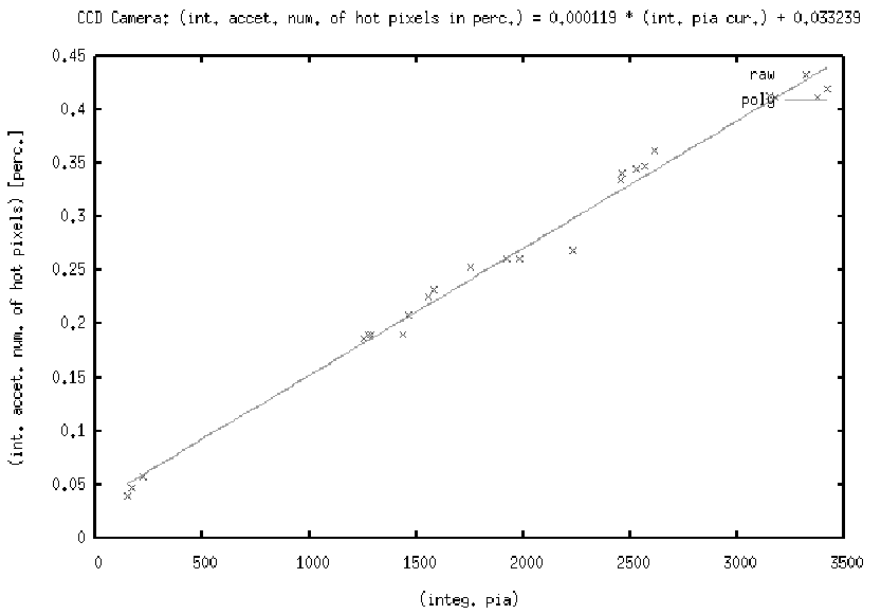



**Figure 16.** Integral deltas of number of hot pixels as a function of integral PIA current.

## 3.5. Field Programmable Gate Arrays irradiation experiments

### 3.5.1. Field Programmable Gate Array technology

Field Programmable Gate Array chips (FPGAs) are type of programmable circuits, which are programmed by user to perform the designed functionallity. Project must be written in one of Hardware Description Language (HDL), e.g. VHDL, Verilog. It's compiled, synthesized and implemented in FPGA chip. The configuration bits can be stored in a chip using different techniques depending on technology:

- Antifuse technology - programmable only once,
- Flash memory - programmable several times,
- SRAM memory - programmable dynamically.

The last possibility is dominating technology. It allows very fast, almost unlimited in system reprogramming.

Architecture of FPGA chips from different vendors may differ but the main idea is almost the same. It consists of some main blocks (description based on Xilinx Spartan-IIE chip, see Figure 17):

- Flexible, programmable Configurable Logic Blocks (CLB), which provide the functional elements for constructing logic. The basic block of the CLB is Logic Cell (LC). Two LCs form slice and two slices form CLB. Each LC includes a function generator, carry logic and a storage element. The function generator is implemented as look-up table (LUT). The storage element can be configured either as edge-triggered D-type flip-flop or as level-sensitive latch.
- Programmable Input/Output Blocks (IOB), which provide the interface between the package pins and the internal logic. The IOB features inputs and outputs that support a wide variety of I/O signalling standards. Each input and output can be configured to conform to any of the low-voltage signalling standards.

- Delay-Locked Loops (DLL) for clock distribution. This block eliminates skew between the clock input pad and internal clock-input pins throughout the device. Additionaly delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input.
- Dedicated internal memory (Block RAM). That's internal memory that can be used to storage data inside the chip. The word length and type of memeory can be configured by system designer.
- Versatile multi-level interconnection structure. Local routing resources provide three types of connections:
  - interconnections among the LUTs, flip-flops,
  - internal CLB feedback paths, between LUTs in the same CLB,
  - direct paths providing high-speed connections between horizontally adjecent CLBs.

  The software automatically uses the best available routing based on user timing requirements.

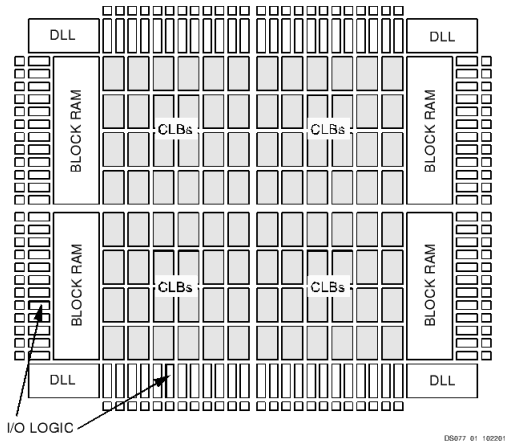



**Figure 17.** Basic Spartan-IIE Family FPGA Block Diagram [9]

Values stored in static memory cells control all the configurable logic elements and interconnection resources. These values must be loaded into the memory cells on power-up and can be reloaded to change function of the device, almost any time.

### 3.5.2. Radiation induceed errors in FPGA chips

The two most important components of a FPGA chip where radiation failures occur are SRAM (Static Random Access Memory) cells and flip-flops. The most probable errors are related to Single Event Effects, particularly Single Event Upsets.

Single Event Upset (SEU) is a change of a logic state of an element storing one bit caused by radiation. Two types of SEUs may be distinguished:

- static SEUs - changes in the configuration bits
- dynamic (or transient) SEUs - changes the logic state of the bits, which are supposed to change during normal operation (for example flip-flops)

SEUs affect the performance of FPGA in different ways. Changing the state of one flip-flop working as a latch results in false value of one bit during one clock period only, while changing the state of one SRAM cell in look-up table results in a permanent wrong answer for one combination of input bits. Changing the state of one SRAM that programs the interconnection between logic blocks can seriously modify the performance of whole circuit. [4]

### 3.5.3. Test board and system

For the irradiation experiments the SRAM-based FPGA chip from Xilinx company - Xilinx XC2V1000 was used. Chip was mounted on Virtex-II LC 1000 Memec Development Kit (see Figure 18). This board also utilizes:

- serial interface (RS-232 C)
- voltage regulators
- DDR and PROM memories
- oscillators
- LED display

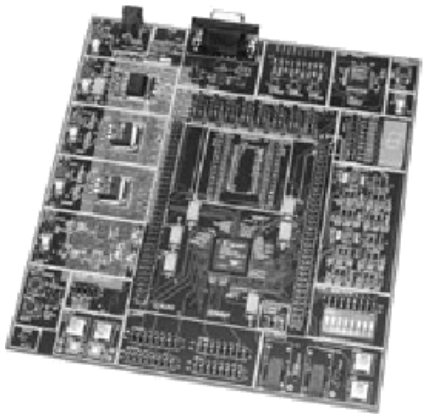


**Figure 18.** Virtex-II LC 1000 Memec Development Kit [9]

The test board was connected with computer placed outside the irradiated area. Connection provides configuring and verifying of FPGA chip by JTAG interface. There was appropriate software running on computer, performing test routine (see Figure 19) automatically.

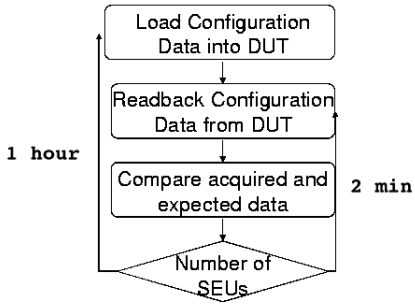



**Figure 19.** FPGA test routine

Test routine (see Figure 19) allows to verify FPGA configuration memory. Programming DUT with dummy project was performed every 1 hour. The reading back configuration was done every 2 minutes. The result was compared with bitstream with which DUT was programmed. The number of different bits shows number of static errors in configuration memory of FPGA.

### 3.5.4. Results of the experiment

The results of tests are shown in Figure 20. Picture presents total number of SEUs in configuration memory and integrated PIA current during each day of experiment. There is strong relationship between these values.

On the other hand there were only SEUs observed, no permanent destruction of FPGA chip. Also there were no problems with voltage regulators and JTAG interface. These elements worked correctly.

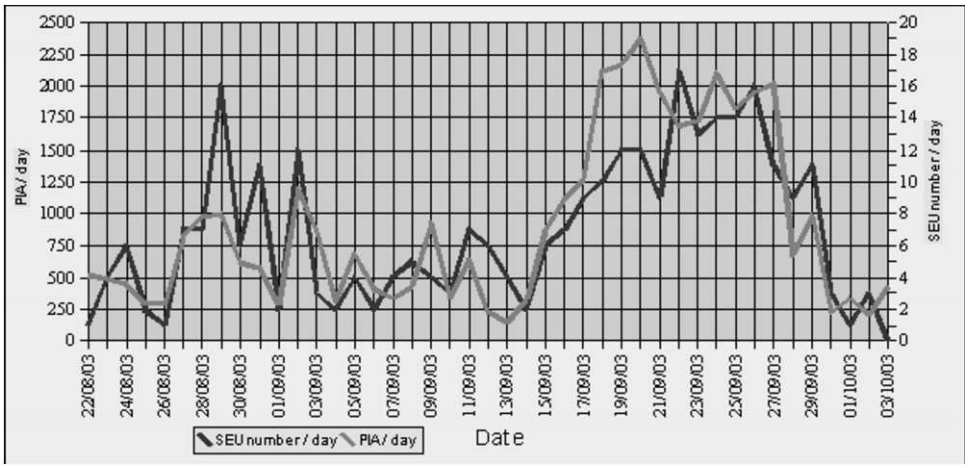



**Figure 20.** SEUs in FPGA configuration memory

## 4. COUNTER MEASURES METHODS

Irradiation experiments show that special methods of mitigation of radiation effects are needed. There are several ways to perform it:

- Conventional shieldings
- Chips dedicated to work in irradiation environment
- Appropriate system design (eg. Triple Module Redundancy)

### 4.1. Conventional shieldings

Estimated maximum value of gamma radiation is about 10 rad / h = about $10^6$ rad / 20 years. The maximum Total Ionizing Dose for electronic devices is about a few krads. In this case gamma field should be reduced to 0.1 % to secure in-tunnel electronics. The best substance for this purpose is concrete. This material has HVL factor about 100 mm, for gamma radiation energy 5 MeV. Half-Value Layer (HVL) is the thickness of material to reduce gamma radiation to half [6]. To reduce gamma to 0.1 % there should be used $10 * 100mm = 1m$ of concrete wall.

Neutrons for electronic devices is not a critical problem. They cause only not-permanent errors [4]. Shielding againt neutron radiation is less important.

### 4.2. Dedicated electronics for radiation environment

Some companies produce chips designed to work in high radiation environment. For example it could be XQR family of Xilinx FPGA chips. It has bigger (200 krads instead of tens krad) Total Ionizing Dose. This chips have longer lifetime exposed to high radiation.

There are also whole electronic systems dedicated to radiation environment. Maxwell company produces SCS750 board wich includes 3 PowerPC on it. In comparison to commercial PowerPC it can withstand a dose in excess of 100 krad. It has also incredible high SEU rate ($< 9 * 10^{-6}$ upset per day on GEO orbit).

The main disadvantage of such rad-hard devices is high cost. It is many times higher than price of normal, commercial devices.

### 4.3. Appropriate system design

There are some methods to mitigate irradiation problems with electronic devices by designing appropriate system schematic. For example it could be (in the brackets there is name of the effect against which method protects):

- Current Limiting (SEL, SEB)
- Software and hardware error detection and correction (SEU)
- Constant refreshing (SEU)
- Redundancy triple voting - TMR (SEU):

These ideas are presented in other publications, eg. [3].

## 5. CONCLUSIONS

All experiments show that irradiation of electronic devices causes damages. Depending on that information there is a possibility of buidling systems to measure radiation using Light Emitting Diodes and Charge Coupled Devices as radiation detectors. Although control and calibration experiments should be performed.

Next point is that errors in Field Programmable Gate Arary chips are Single Event Upsets. There are caused mainly by neutrons. Gamma radiation only limits lifetime of devices but does not causes improper work.

The results of experiments show some radiation mitigation methods should be used to ensure electronic system will work properly in the tunnel. Previous chapter of this article presented several new concepts. We are planning to conduct thorough experiments in order to investigate the function of complex electronic systems in various radiation environments of interest. A suitable counter measures could be selected from the above experimental results.

## REFERENCES


1. H. Weise, *Introduction to Linac 2 / PIA and Linac 3*, 2003
2. L. Dusseau, *Introduction to Radiation Issues of Commercial-Off-The-Shelf (COTS) Components*, CERN Training 2000
3. M. Dentan, *Radiation Effects on Electronic Components and Circuits*, CERN Training 2000
4. K. Bunkowski, I. Kassamakov, K. Kierzkowski, M. Kudla, T. Maenpaa, K. Pozniak, D. Rybka, E. Tuominen, D. Ungaro, W. Zabolotny, *Irradiation Effects in Electronic Components of the RPC Trigger for the CMS Experiments*, SPIE Proceedings, Volume 5484
5. F. Gusmao, *Single Event Upset Mitigation Techniques for Programmable Devices*
6. J. Burnham, *Radiation Protection ("Green Book")*
7. Particle Physics Experiments at JLC ACFA Linear Collider Working Group Report.
8. Investigation of radiation damage effects in neutron irradiated CCD. Physics Department, University of Oregon.
9. Datasheets of used devices, chips and parts



Paper presented during the XVIth IEEE-SPIE Conference on Electronics and Photonics for High Energy Physics Experiments, WILGA 26-30 May, Published in Proc. SPIE,