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Characterisation of an ATLAS Forward-SCT Prototype Silicon Microstrip Module

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Abstract

A prototype silicon microstrip detector module for the forward-region of the ATLAS Semiconductor Tracker (SCT), has been constructed and evaluated. Results are presented from laboratory work with the full 11.955cm-long module along with earlier test-beam studies with the module at *'half-length'* (6.3778cm long strips). The detectors incorporate radial n^+-type strips which would measure ϕ-coordinate in the ATLAS collider geometry. The isolation technique is that of individual p-stops and the pitch varies from 70μm at the narrow end to 90μm at the broad end. The module was equipped with CAFE and CDP binary readout electronics offering 40MHz sampling. The CAFE chips were found to exhibit an excessive degree of pedestal variation, however by correcting for this effect in order to isolate the detector properties, the beam test study indicates a minimum-ionising particle detection efficiency consistent with 99% or above up to a threshold of 1.9fC at 300V reverse bias. The noise occupancy for the full length module is less than 10^{-3} for thesholds above 0.8fC giving a useful threshold '*headroom*' of 1.1fC, pre-irradiation. Figures for the intrinsic spatial resolution within this threshold operation range are found to be consistent with $\frac{\text{strip pitch}}{\sqrt{12}}$.

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Introduction

Following the decision to adopt silicon for microstrip-based tracking in the forward regions of the ATLAS Inner Detector, prototype detectors with a radial strip geometry were designed in the UK in early 1996 and manufactured by Hamamatsu Photonics[1] during that year. These detectors comprised n^+ strips in n^- bulk material, the chosen isolation method being that of individual p-stops. Two separate wafer fabrications were required to form 11.955cm strip-length modules, each wafer containing either a 6.3778cm-long, full-width narrow wedge-shaped detector or its 5.5772cm strip-length broader partner. Upon delivery of the first batch of wafers, (which incorporated the narrow-end wedge plaquettes only), a half-length module with binary readout was constructed and installed in the H8 test-beam at CERN for evaluation in September 1996. This note gives an account of the analysis of the data collected from the module during that run along with some results from tests conducted in the laboratory at Liverpool with the full-length device.

Detector design features

In Figure 1 the layout of the wafers is shown. The readout pitch varies from 70μm at the narrow end to 90μm at the broad end, the number of channels being 770. In operation the outer two channels would not be instrumented but would however be tied to the same potential as the others. In this way, readout strips with asymmetric electric field profiles at the detector edges are avoided. During the SCT detector review in December 1995,

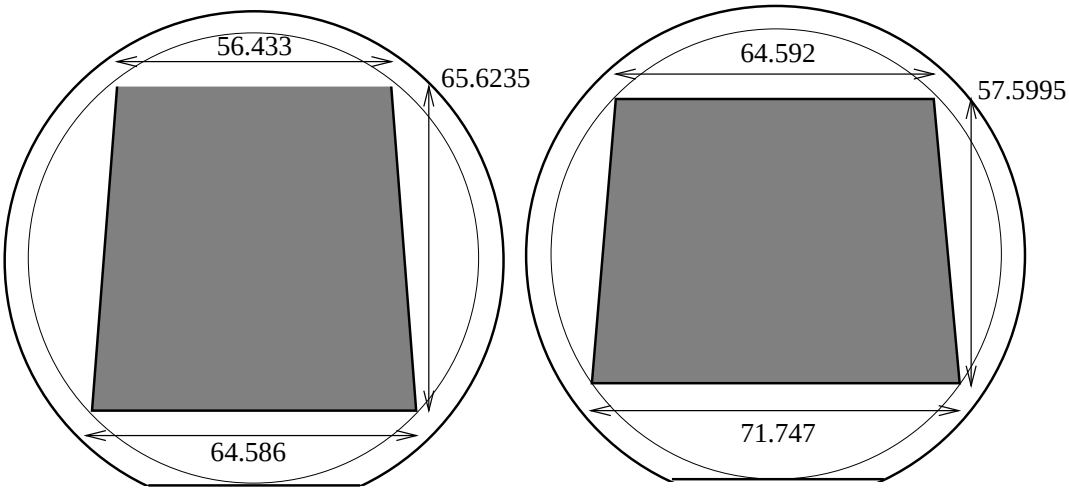

Figure 1: *Forward prototype detectors: wafer layouts.*

the detector design philosophy based on n^+ strips in n^- bulk material was established as the baseline choice for reasons of radiation tolerance. In this design the n^+-type readout strips are electrically isolated from each other by means of surrounding implanted p^+-type rings (*individual p-stops*)[2].

The detectors were also designed to be compatible with the binary readout scheme which was adopted as the baseline choice during the SCT electronics review. For optimal efficiency, charge division between readout strips must be minimised therefore no intermediate diodes were included in these designs. With individual p-stops however, the non-implanted regions between adjacent p-type implants, where electrons accumulate beneath the silicon dioxide interface, have the potential to act as intermediate strips. With this in mind the p-stop gap was chosen to be as narrow as possible, (10μm), and priority was given to an investigation of this effect.

Figure 2 shows a magnified view of one corner of a narrow wedge device. Each n^+ strip is connected to a common bias bus via a polysilicon resistor (these are the meandering structures observed in the photograph). In this way the implant strips may be AC-coupled to the readout electronics via integrated capacitors. Below and to the right of the strips, the compound guard-ring structure is visible. Comprising alternating n^+ and p^+ rings, this serves to enhance the high voltage performance by gradually ramping down the potential towards the cut edge of the detector (thus suppressing the onset of breakdown). On the reverse side of the crystal, (the junction-side), a mirror of this guard structure, which is composed of p^+ implants only, is present. The active area on the junction-side has a uniform covering of p^+ implant which is directly coupled to an even coating of aluminium, forming the backplane. A detailed view of the polysilicon structures and the p-stops is seen in figure 4.

Figure 3 shows a conceptual longitudinal cross section through the forward ATLAS Semiconductor Tracker (SCT)[3]. In this layout, keystone-geometry silicon microstrip detectors are present on 9 discs [3]. The radial coverage spans from 320mm to 560mm with the exception of the outer 3 discs which extend down to the radius defined by[4] $|\eta|$ =2.5. Each disc contains two rings of wedge-shaped modules, a module having an active length of 12cm. Each module would comprise two detector layers, one providing the ϕ-coordinate and the other rotated by a 40mrad stereo angle.

[2]Detailed beam-test studies of an SCT-barrel prototype detector incorporating the alternative scheme of a common p-stop network [2] indicated that this choice was not optimised for charge collection efficiency. Seperate pulse height spectra were produced for tracks which had intercepted this detector within $\frac{\text{pitch}}{4}$ distance of a readout strip and those which extrapolated to a position outside these zones. In the former case, the peak of the Landau distribution was notably higher than in the latter. Plots of mean signal to noise versus the distance from a track extrapolation point to a readout strip showed that some charge was present in channels which were not directly next to the hits.

[3]a conceptual mounting scheme is described in [4]

[4]where η = pseudo-rapidity

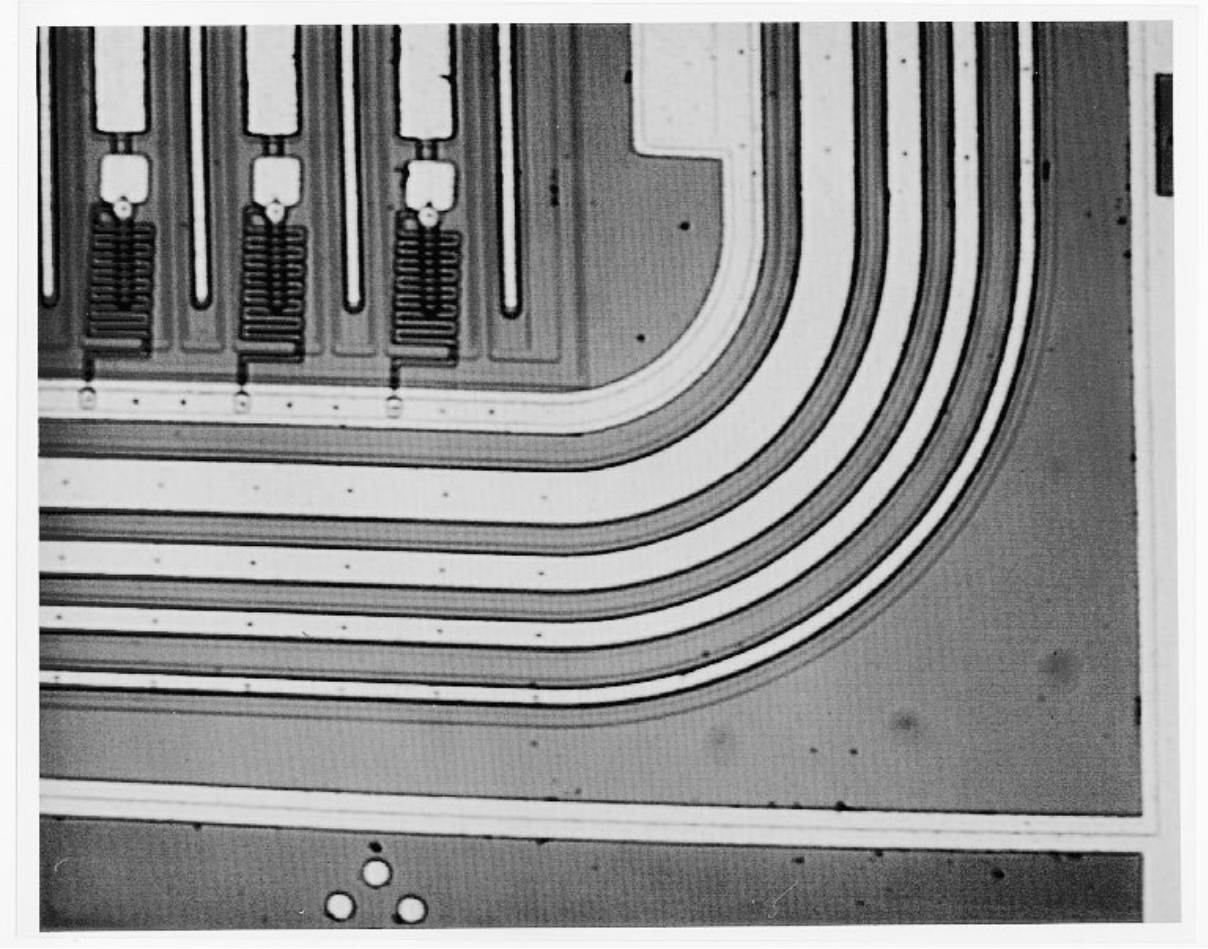

Figure 2: *Photograph of one corner of a narrow wedge detector.*

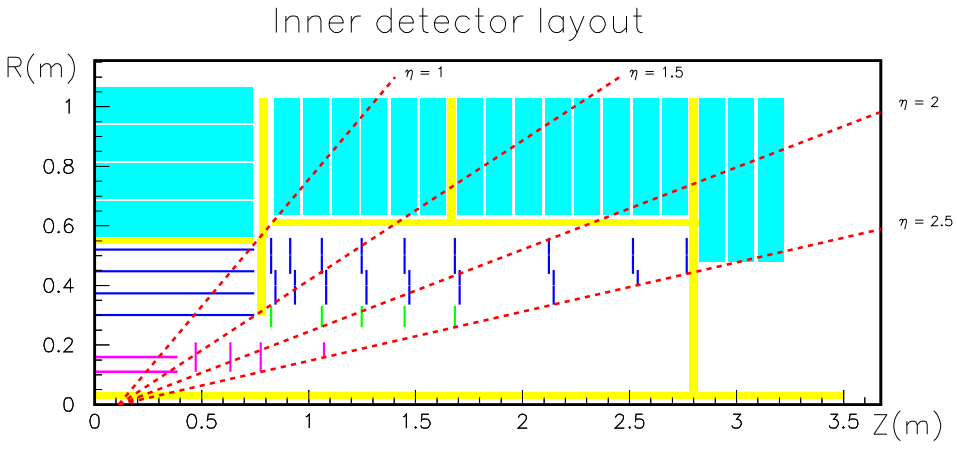

Figure 3: *Cross section through the Inner Detector.*

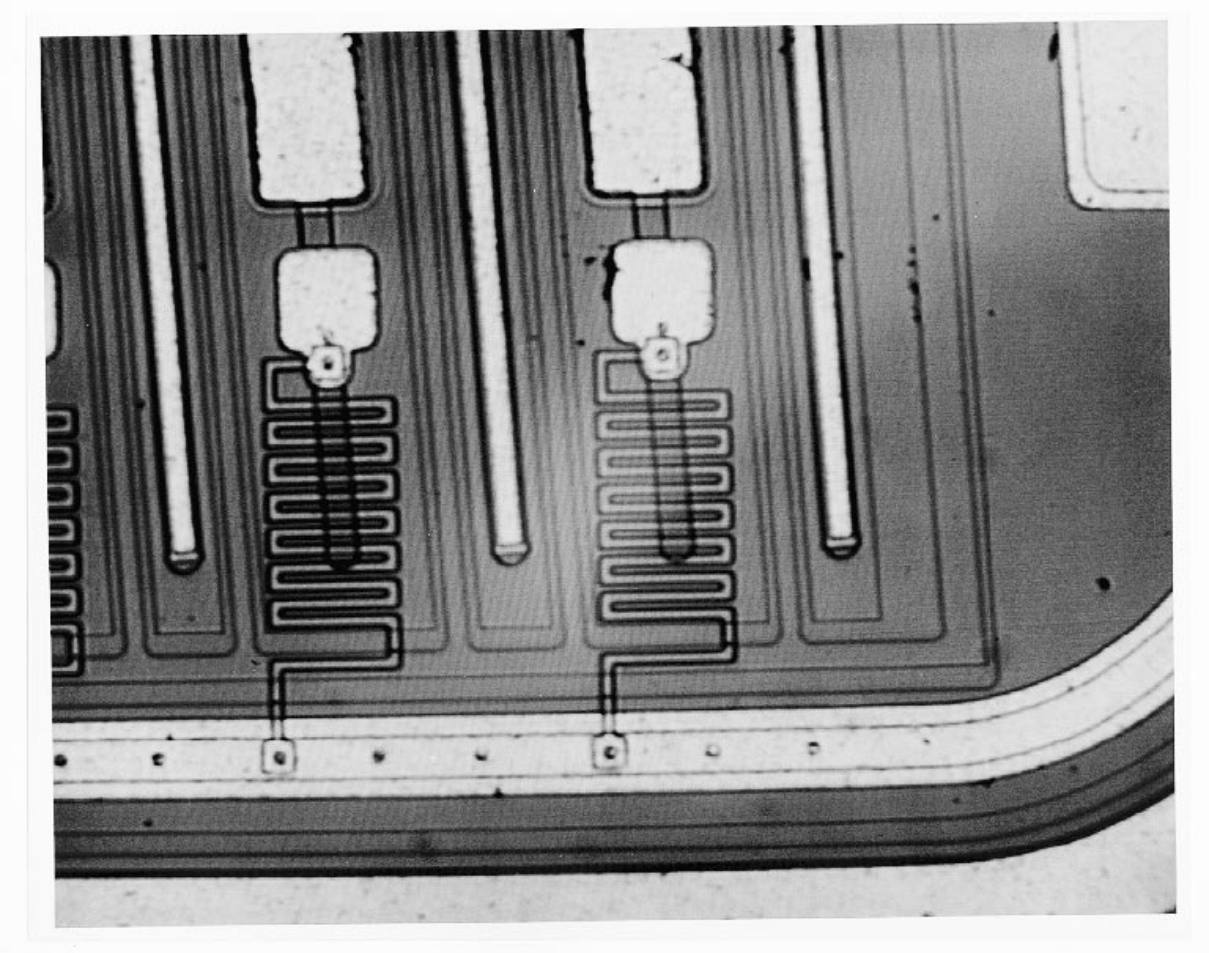

Figure 4: *Detailed view of detector corner showing polysilicon resistors and individual p-stops.*

Detector electrical properties

Measurements of leakage current performed as a function of reverse-bias voltage on a batch of the detectors showed that they were all within the pre-irradiation specification of 6μA at 150V. These results are depicted in figure 5. The interstrip capacitance from an individual readout strip to its two nearest neighbours and to the next nearest pair was determined. Figures 6 and 7 show that for the narrow wedge detector the nearest neighbour capacitance converges to a value of 5.0pF beyond depletion for a range of frequencies whilst that of the secondary neighbours is 1.4pF. For the broader device the corresponding figures are 3.8pF and 1.2pF. While the nearest neighbour capacitance measurement was being performed, the next to nearest strips were held at the same potential as those taking part in the measurement and vice versa. In figure 8 the total dynamic capacitance from the strip side to the backplane is shown for both types of detector at 300kHz. The sum total of this capacitance is 287pF beyond depletion giving 0.37pF per channel, a figure which includes the capacitance of the guard rings and is thus an upper limit. The total capacitive load per channel is therefore estimated to be less than 11.77pF corresponding to 0.98pF/cm. Along with the load capacitance, the noise of

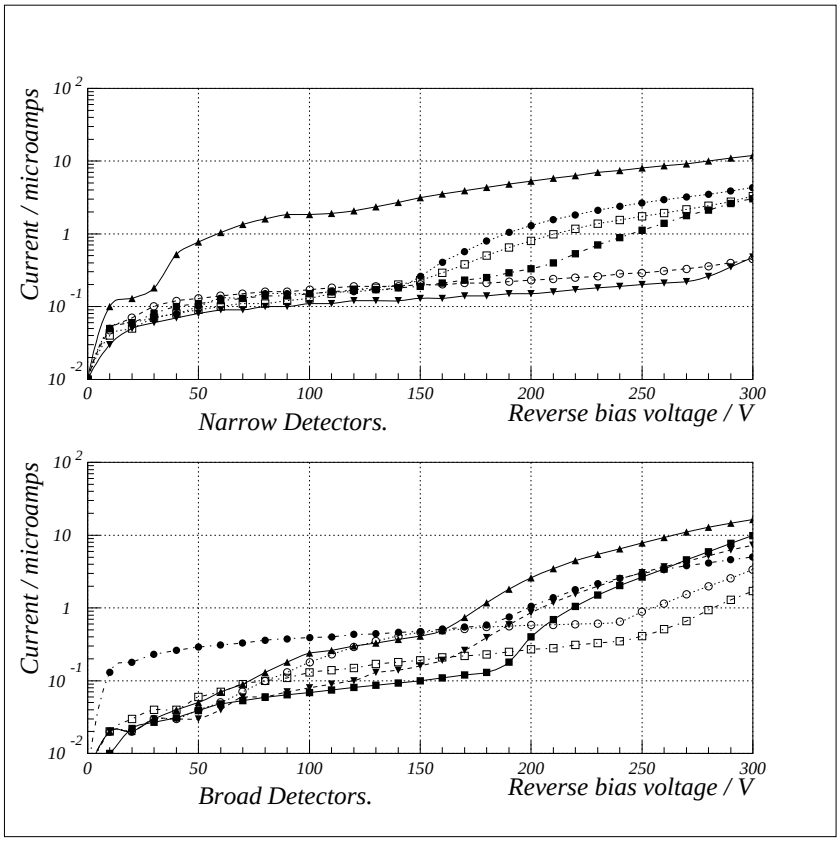

Figure 5: *IV Characteristics for both types of Hamamatsu forward detectors.*

a detector channel is also dependent upon the aluminium strip resistance due to Johnson noise generation. Figure 9 shows the values obtained from measurements performed on a batch of the detectors. The figures are within the specified value of R<20Ω/cm.

The module composition

The half-length module which was installed into the H8 beam in September comprised a narrow wedge detector which was read out via a flat-back barrel $r\phi$-type ceramic hybrid designed at the Lawrence Berkeley National Laboratory, (see figure 10). This hybrid was populated with 6 *bn-flavour*[5] bipolar front-end CAFE[5] chips manufactured by AT&T in the US and 6 CMOS CDP[6] back-end chips. The CDP operation and data readout were controlled via a HAC[7] sequence manager chip. Only two of the CAFE chips were fully working devices so only these two were bonded to the detector channels. The detector and hybrid were each glued to a flat rectangular piece of ceramic, avoiding the junction-side guard region, using slow-cure Araldite. No evidence of detector degradation in terms of its leakage current was observed post-gluing and bonding. The backplane contact was achieved by means of connecting a fine wire to the large unpassivated region with

[5]i.e. binary n-type

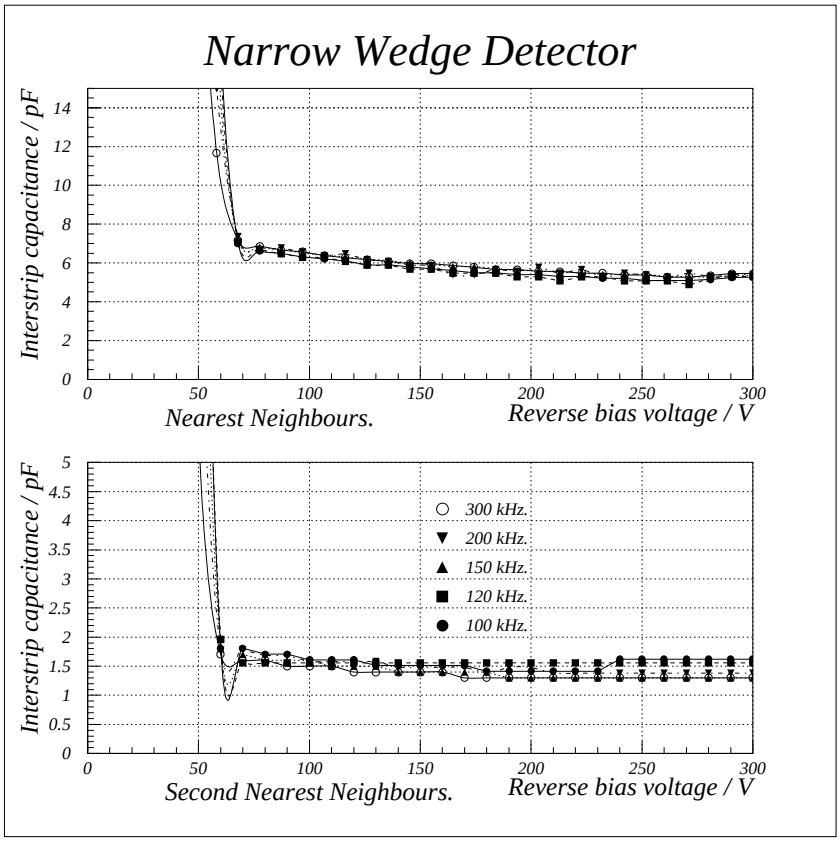

Figure 6: *Interstrip capacitance measurements for a narrow wedge detector.*

conductive epoxy. The broad detector was added to the module after the beam test and this was studied in the laboratory, see figure 11

Test beam studies

The H8 assembly

Figure 12 shows a schematic of the arrangement within the H8 test beam area. Silicon strip modules are mounted on a granite block which is supported on the second trolley in the diagram. During the September 1996 period of running, track definitions were provided by a system of three hodoscope cross-planes (at z-positions of 0cm, 74cm and 77cm) of 50μm pitch silicon detectors instrumented with VIKING[8] readout chips. Data was taken for the forward module with applied reverse bias voltages of 80V, 150V and 300V and the orientation was vertical, (measuring x), for the 80V period and horizontal for the remainder of the run, (see figure 10).The z-position was 25cm. The beam composition varied throughout the run period as the tile calorimeter group were the main users, however for most of the data presented here the beam comprised either pions or muons at energies of $100GeV$ or above.

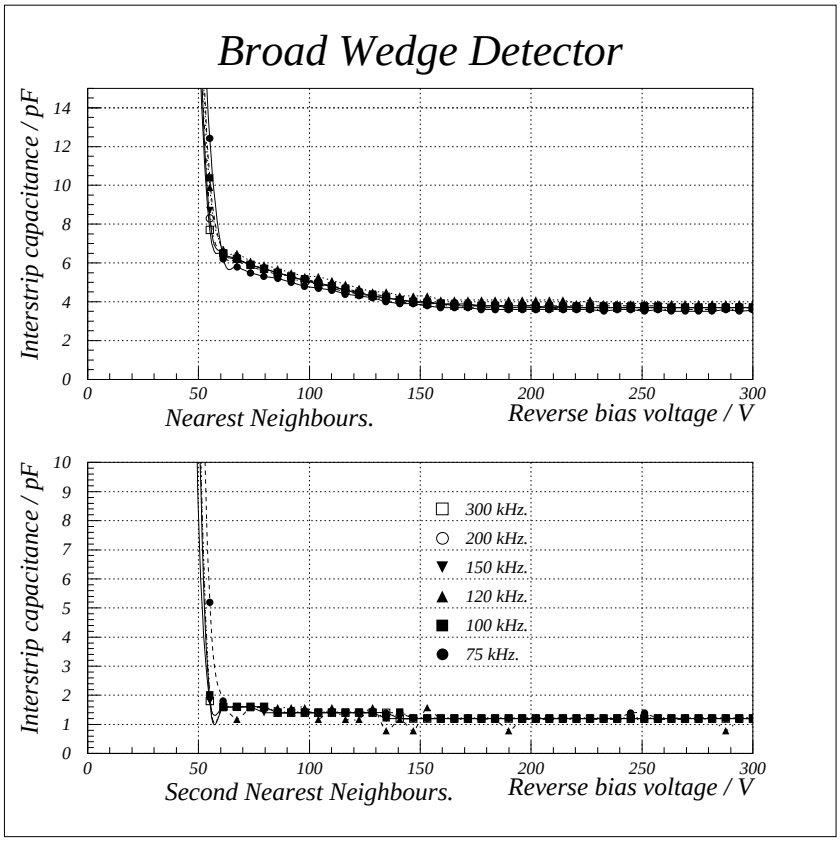

Figure 7: *Interstrip capacitance measurements for a broad wedge detector.*

First iteration data analysis

For each applied bias, a broad range of threshold was scanned, recording 20,000 triggers per threshold setting. By performing chi-squared straight-line fits in 2 dimensions to space points located in the hodoscope cross-planes, the particle tracks were reconstructed and extrapolated to the z-position of the forward module. Incidents of more than one space point in any hodoscope plane were rejected in order to eliminate 2-track ambiguities. Figure 13 shows the variation in efficiency of the module with the applied threshold (in fC equivalent charge) for a reverse bias voltage of 80V. An efficient event is defined as one in which a track, which extrapolates to the active window of the module, registers a hit on one or both of the two closest strips.

The lower plot in figure 13 shows the rate of fake hit incidence (or *noise occupancy*) as a function of threshold. Channels which lay within 500μm of the projected hit positions were discounted during the calculations in order to reject true hits. The analysis was performed on a single CAFE chip only and in these plots 21 channels are rejected on the basis of being particularly inefficient. A further 20 channels are also rejected for having an uncharacteristically high occupancy. This degree of channel exclusion is worrying and despite the measure only one position in the scan is in accordance with the ATLAS specifications of efficiency$\geq$99% and fake occupancy$\leq 10^{-3}$. An investigation was made into the source of this problem.

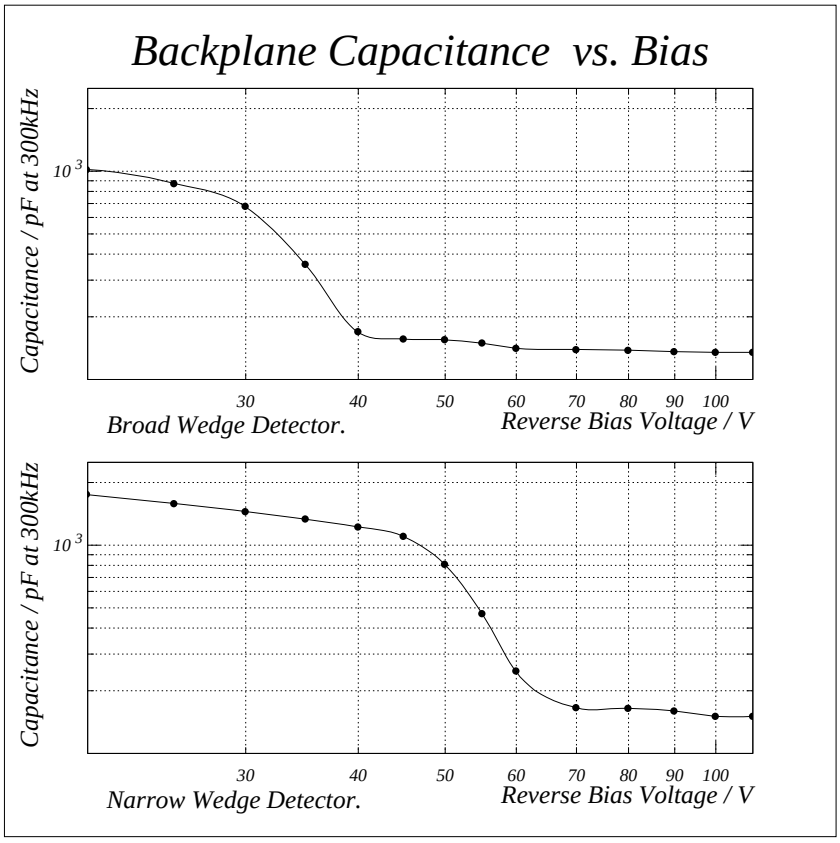

Figure 8: *Backplane capacitances at 300kHz for both types of wedge detector.*

Diagnosis

Calibration data taken in the laboratory was analysed in detail and large variations in response were observed across the readout channels. Figure 14 depicts the extent of this variation for the chip which was involved in the test beam analysis. The upper plot shows the 50% efficiency points taken from a threshold scan with no charge injection, i.e. the *pedestal* value, for each channel. The projection, as seen in the lower plot, is Gaussian with σ equal to 0.28fC. It was noted that the channels which had been rejected in the test beam study tended to populate the fringes of this distribution.

Second iteration analysis

For every channel the pedestal offset relative to the mean of the distribution was recorded in a database. The test beam data was analysed again and for each applied threshold, plots of efficiency and noise occupancy versus true[6] threshold were produced. In the case of efficiency the offset corresponding to the channel closest to the extrapolation was taken into account. Figure 15 shows the graphs which are obtained by combining the individual plots from the whole scan at 80V bias. In this case only 3 of the 128 channels are

[6]i.e. corrected for the offset relative to the applied threshold

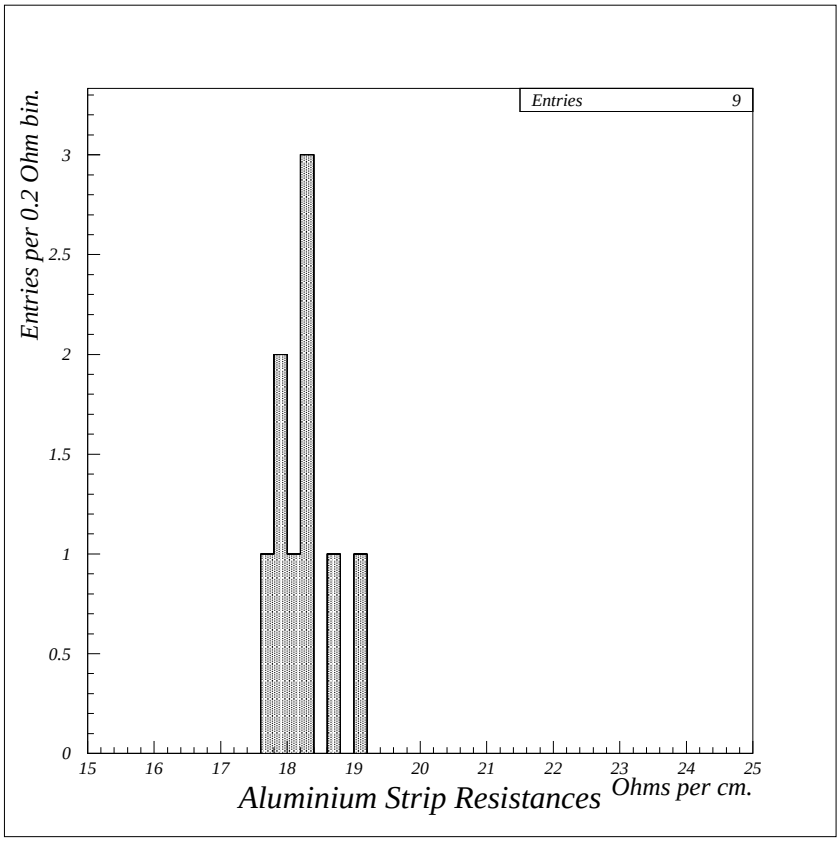

Figure 9: *Aluminium strip resistances in* Ω/cm. *Measurements of the average of 24 strips are shown for 9 detectors.*

rejected and the efficiency is statistically consistent with 99% or above up to a threshold of 1.35fC. The noise occupancy diminishes to a value of 10^{-3} at 0.7fC threshold giving a 0.65fC *'headroom'* of operation. The long tail present in the occupancy plot is due to cases where a particle track has intersected the active region of the forward module but has missed the 3×3cm sensitive window of each hodoscope plane, (thus escaping the track multiplicity veto).

Intrinsic spatial resolution

Figure 16 shows two distributions of the difference in track extrapolation position and hit position in the forward module at an applied threshold corresponding to an input charge of 1.15fC and a reverse-bias voltage of 80V. In the upper plot the cases where only a single strip was found to fire are recorded. The lower plot corresponds to those cases where two adjacent strips in the proximity of the track extrapolation register a hit, the mid-point of those channels taken to be the measured hit position. The r.m.s. values obtained are 20μm and 14μm for the single-strip and double-hit cases respectively and the track extrapolation error is insignificant at the 1μm level when subtracted in quadrature. At this beam position the mean pitch was estimated to be 72μm. The upper plot in figure 17 shows the variation in resolution with threshold. For the data taken at 300V

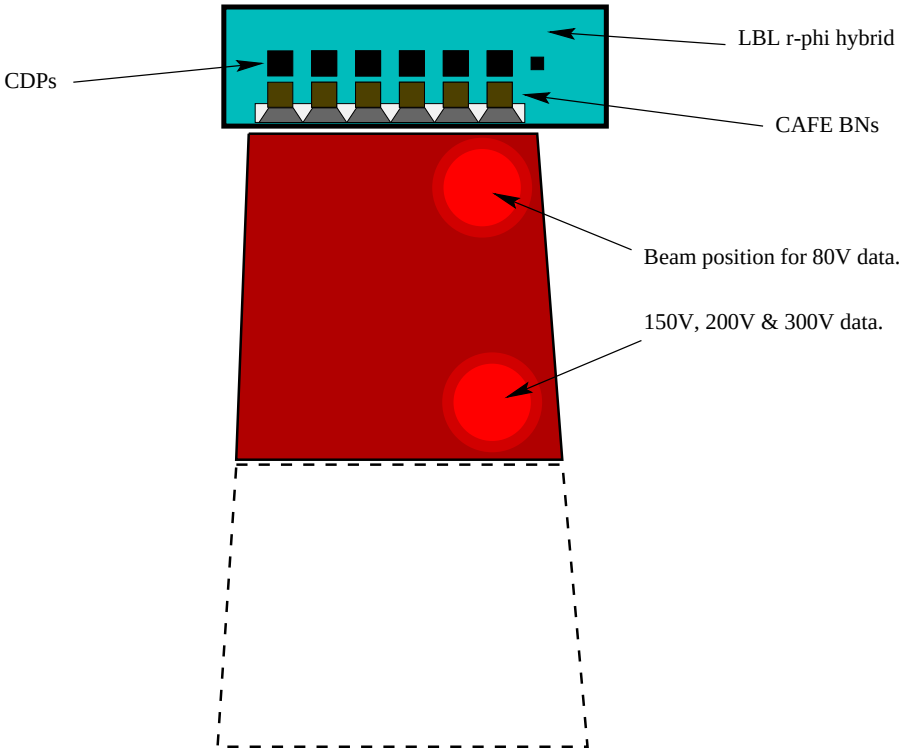

Figure 10: *Forward CAFE module composition.*

the resolution was measured to be 22μm which is also in agreement with $\frac{\text{pitch}}{\sqrt{12}}$ at an approximate mean pitch of 78μm.

Charge division

As mentioned earlier one of the key issues with this detector design is the extent to which the deposited charge is divided between strips. With binary readout electronics the goal is to have all of the charge appearing on one strip only as often as possible in order that the efficiency is maximised. Concern was expressed that the accumulation electrons which reside in the gap between individual p-stops effectively mimic the presence of an extra n-type implant strip thus enhancing charge division by capacitive coupling. The ratio of single to double-channel clusters observed in figure 16 shows that charge division is only occurring at an appreciable level in below 10% of cases at this threshold. In figure 17 the proportion of double-channel clusters is plotted as a function of applied threshold. At 0.8fC this proportion is around 11% and the figure falls with increasing threshold as the front-end comparator becomes less sensitive in the channel which collects the minor portion of the liberated charge.

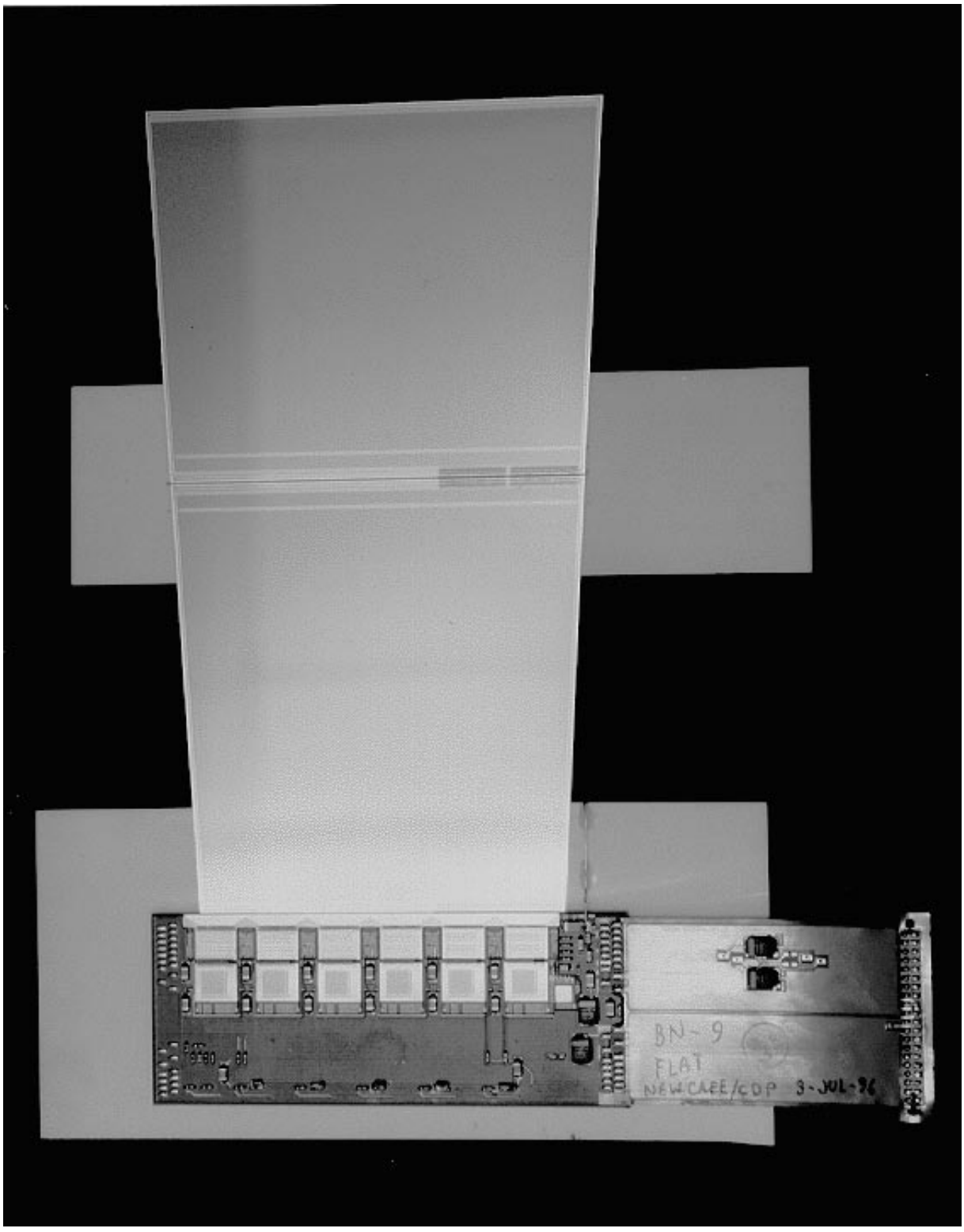

Figure 11: *Photograph of the full 11.955cm strip-length forward module.*

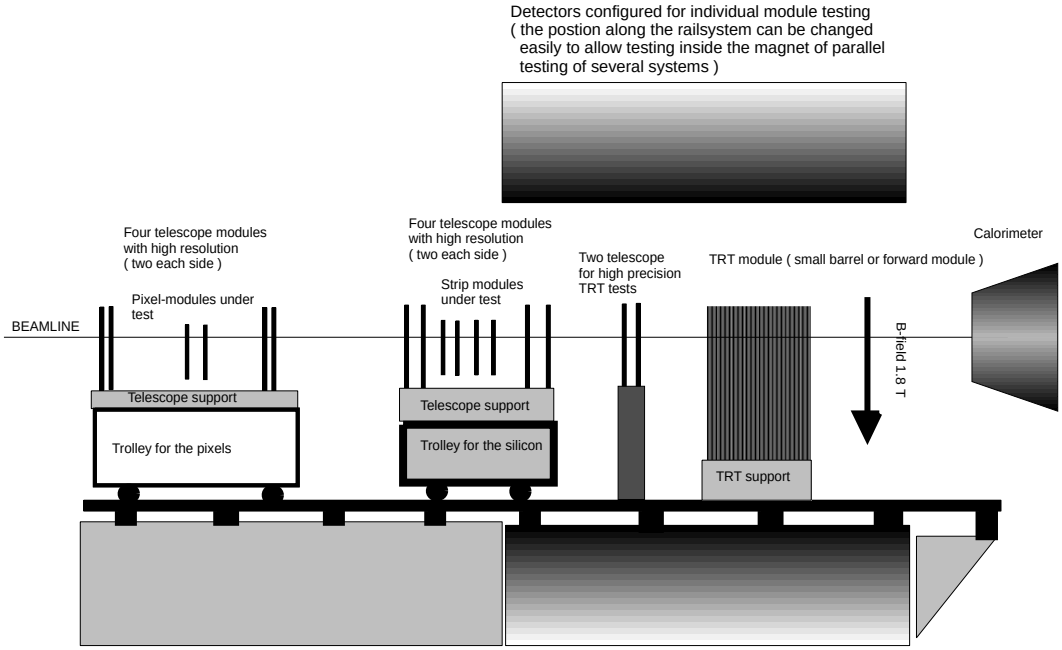

Figure 12: *The H8 assembly.*

Bias voltage scan

Figure 18 shows the figures for efficiency versus corrected threshold for 3 cases of applied reverse bias voltage. At 80V the 50% efficiency point, (i.e. the median of the pulse height spectrum), occurs at 2.90fC. At 200V this value is 3.10fC and at 300V a median charge deposition of 3.25fC is measured. The efficiency at 300V remains at the 99% or above level up to an applied threshold of 1.9fC thus increasing the operation headroom to 1.2fC.

Laboratory studies

Figure 19 shows the noise values obtained by fitting error functions to the efficiency versus threshold curves and correcting for the absolute calibration for a range of charge magnitude injected into the front-end calibration circuitry. With the module at 6.3778cm strip-length a horizontal straight-line fit to the data yields an equivalent noise charge of 1112e$^-$ and at 11.955cm the figure is 1513e$^-$.

In figure 20 the noise occupancy as a function of threshold for the full-length module is plotted. At a threshold value corresponding to $4\times\sigma_{noise}$ (=0.97fC) the occupancy is approximately 10^{-4}. In the absence of beam there is no tail present at high thresholds.

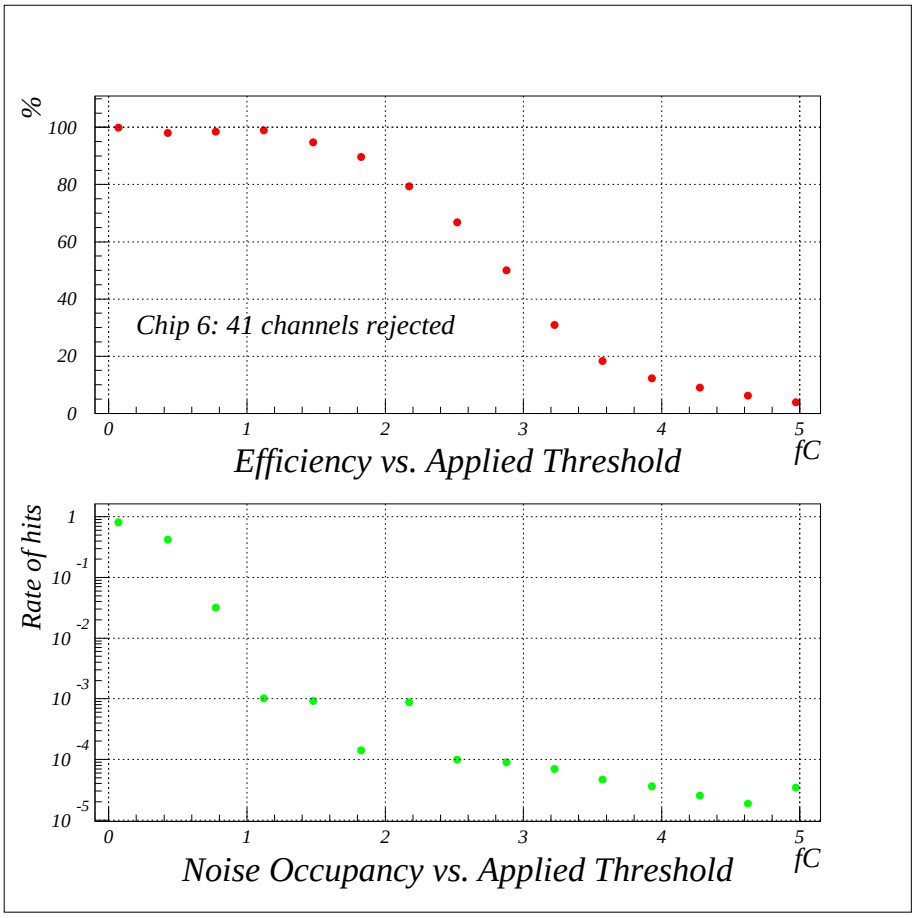

Figure 13: *Efficiency and noise occupancy as a function of applied threshold for a reverse bias of 80V. Forty-one channels from this single chip are rejected.*

Conclusions

An ATLAS forward-SCT prototype silicon microstrip module with baseline n^+ strip in n^- bulk detectors and binary readout was constructed and evaluated in the H8 test beam. Studies of resolution, efficiency and noise occupancy, having corrected for the channel-to-channel pedestal non-uniformity in the front-end CAFE chips, indicate that the detectors perform well and within the ATLAS specifications pre-irradiation. Leakage currents are below the 6μA specification at 150V bias and load capacitance values are well below the 1.2pF/cm specification also. Values measured for the aluminium strip resistance are below the requirement of 20Ω/cm. The individual p-stop isolation structures fulfill their function and by choosing a gap of 10μm between adjacent p-implants, charge liberated by the passage of a MIP divides between 2 readout strips in $<10\%$ of cases over a broad range of hit selection threshold.

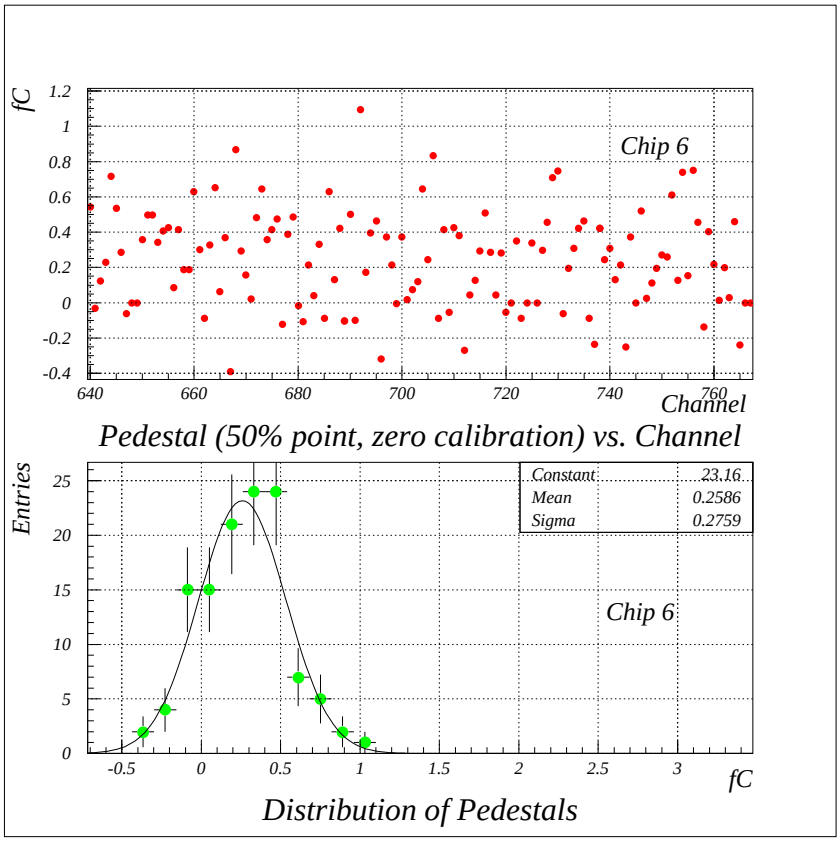

Figure 14: *Pedestal variation.*

Acknowledgements

We would like to express gratitude to Helmuth Spieler, Carl Haber, Sandra Ciocio, Jim Siegrest and Julio Lozano at LBNL and to Tim Dubbs and Hartmut Sadrozinski at Santa Cruz for putting the hybrid together and offering lots of invaluable help and advice. Thanks to Allan Clark, Bertrand Vuaridel, Roberto Bonino and Christian Couyoumtzelis at Geneva for access to the binary system at CERN and help with the test beam mechanics. We also wish to acknowledge the efforts of Ogmundur Runolfsson at CERN who was involved in the construction of this module.

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[3] Detailed information regarding the SCT may be found in:
The ATLAS Collaboration, *ATLAS: Technical Proposal for a General-Purpose pp*

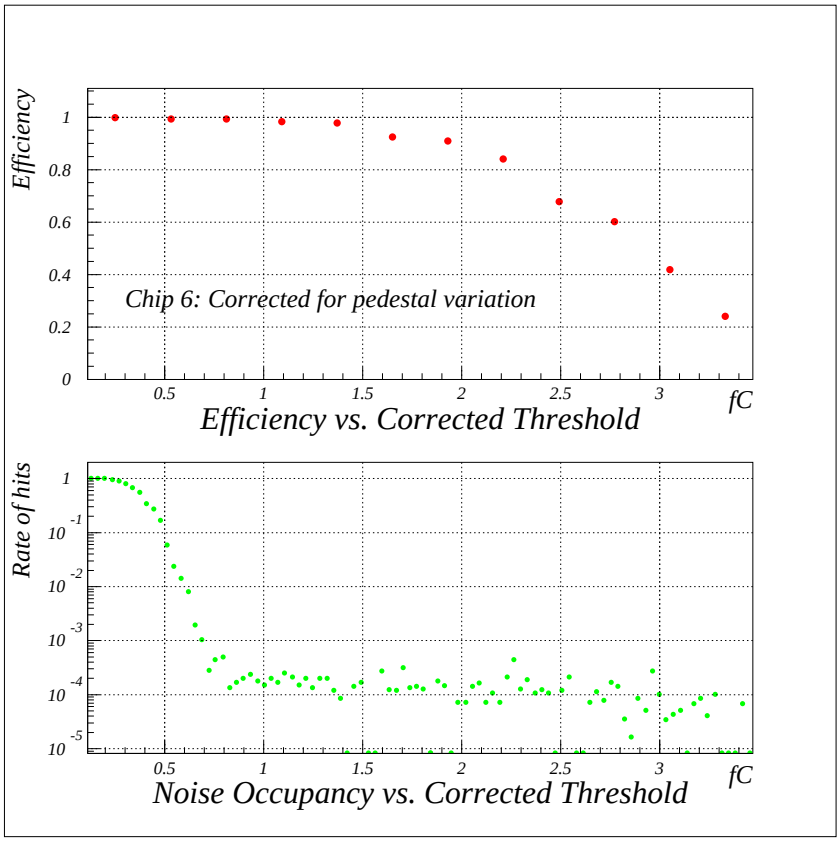

Figure 15: *Efficiency and noise occupancy as a function of threshold plots obtained when the data is corrected for individual channel offsets in pedestal.*

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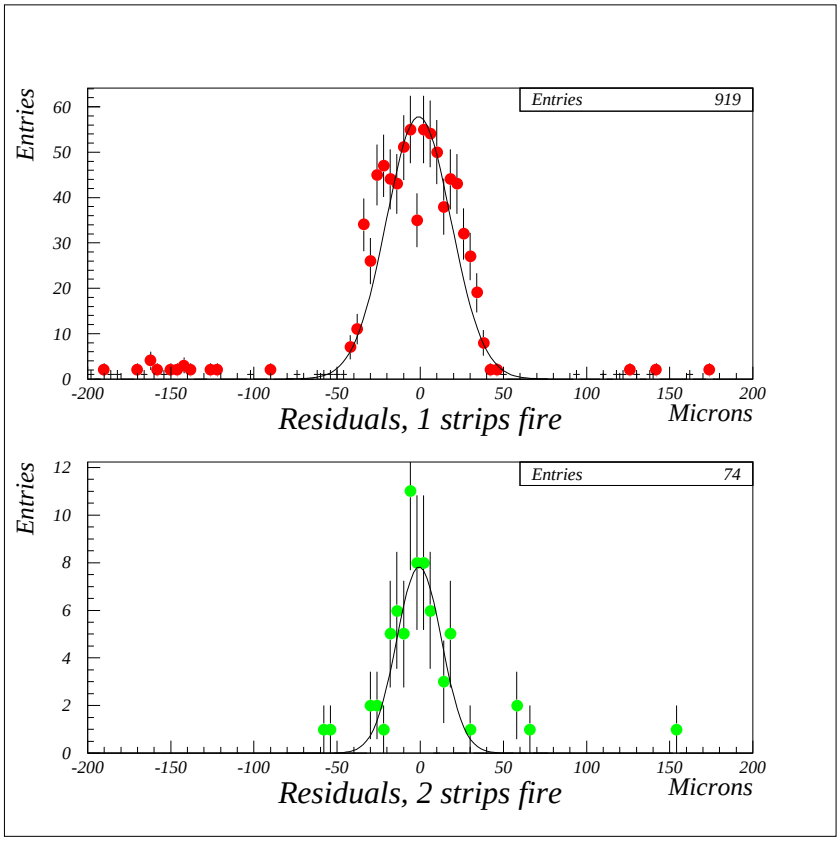

Figure 16: *Distributions of residuals for single-channel clusters (upper plot) and double-channel clusters at 80V reverse bias.*

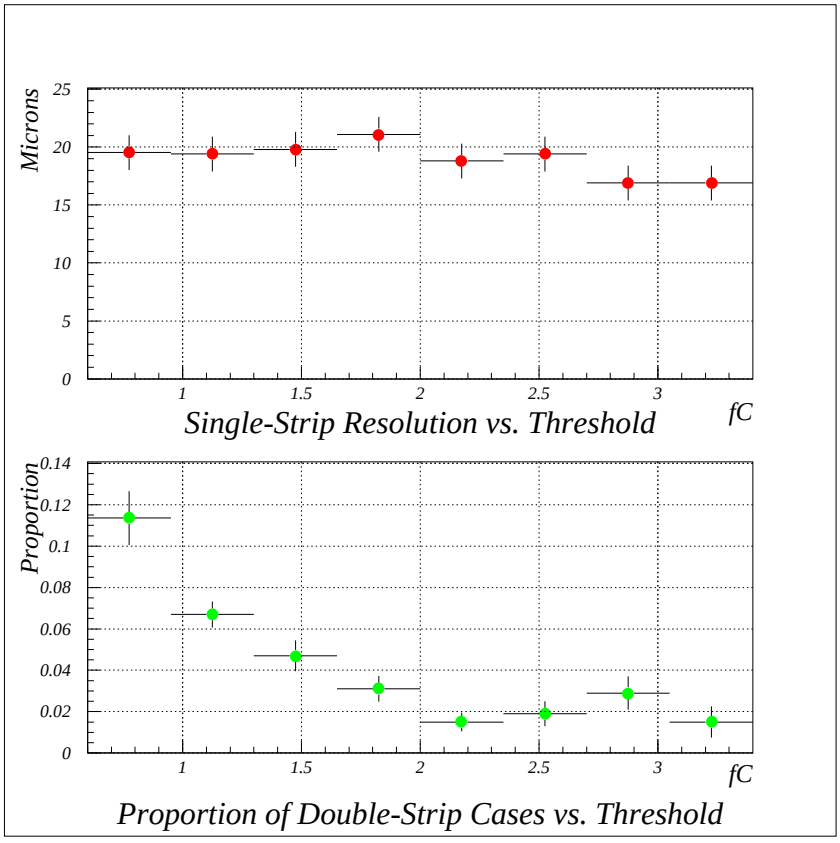

Figure 17: *Variation in spatial resolution with threshold at 80V bias (upper) and proportion of double channel clusters (lower).*

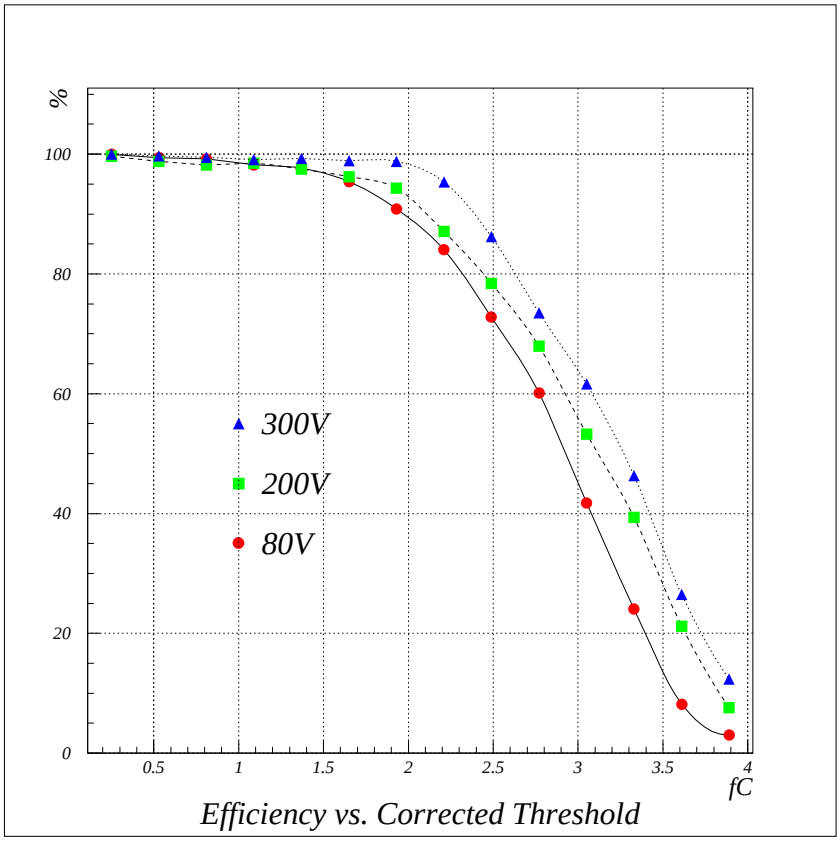

Figure 18: *Comparison of efficiency versus threshold for reverse bias voltages of 80V, 200V and 300V.*

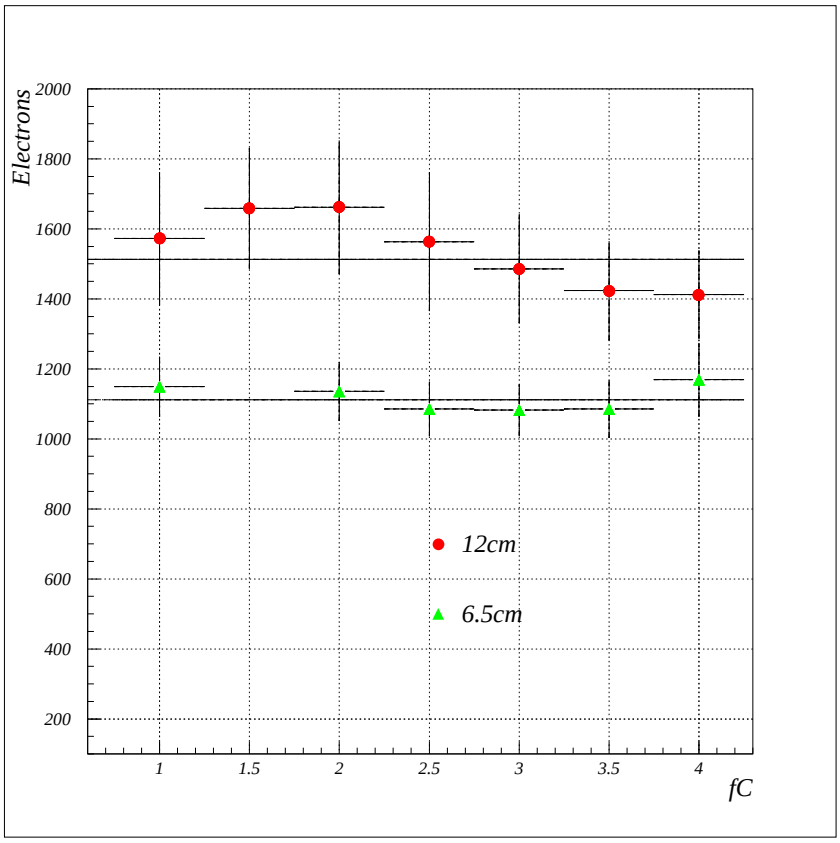

Figure 19: *Noise versus input calibration charge for the module at 6.3778cm and at 11.955cm for an applied bias of 300V*

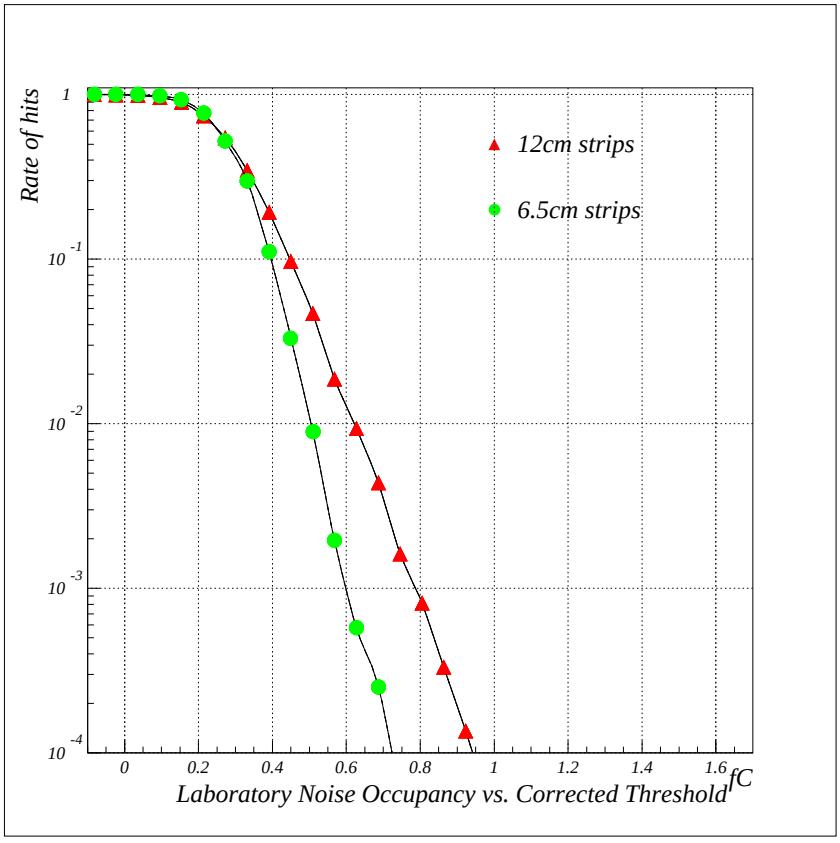

Figure 20: *Noise occupancy measured in the laboratory (V_{bias}=300V).*