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# Development of Control and Monitoring for Silicon Microstrip Detector Modules in ATLAS

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**Abstract**

The silicon detector proposed for ATLAS apparatus at LHC is more than an order of magnitude bigger than the silicon vertex detectors currently in use. This fact combined with the severe radiation and high data rates at LHC imply that high requirements have to be put on the control and monitoring. The scheme we propose is based on circuits located on the detector modules which we intend to pursue in a development programme that comprises design, simulation and fabrication of control and monitoring chip prototypes to be operated and evaluated with ATLAS silicon microstrip detector module prototypes in test beams.

# 1. Introduction

A Control and Monitoring (CM) circuit will be developed for the Barrel Sector Prototype (BSP)[1] project within the ATLAS project which is one of the two proposed large experiments at the Large Hadron Collider (LHC)[2]. The CM circuit proposed here will be developed for the pulse-height readout solution represented by the FELIX front-end chip. The development is planned to take about 3 years. The first year will be dedicated to develop the CM scheme in a prototype circuit. The work includes specification of the requirements for the CM, design of a simple CM and implementation of the CM in gate-array. In parallel the design of a Printed Circuit Board (PCB) for testing the CM with a ATLAS type Silicon Strip Detector (SSD) module will be made. The module will be tested in the ATLAS test beam in fall 1995. In the next design to be made the complexity of the circuit will be increased to meet the needs of the ATLAS Silicon Inner Tracker (SIT). This circuit will be implemented in IC technology. In a third step the circuit design will be further adapted to the needs of ATLAS and implemented in radiation hard IC technology.

# 2. Control and monitoring

The control and monitoring of a SemiConductor Tracker (SCT) detector module can be seen as a set of functions operating the module. The functions are of two kinds: control of the data when data is sent to the module and monitoring of the data when data is received from the module. A control function can be e.g. a bias setting of a front-end chip or a masking pattern of bad channels. A monitoring function can be e.g. a reading of a bias current or a temperature reading. The changes in the operating conditions of a detector module can be split in two types: global and local. The global changes are generally slow and caused by radiation or heat. If a global change proceeds too far then the physics data from the whole tracker may be degraded. A global change may damage the tracker completely. A local change is fast and typically limited to a single channel, a front-end chip or a detector module. Such a failure is local and will only partly degrade the data. A CM circuit which can check the module at regular interval is sufficient to avoid global problems. On the other hand, as the number of CM functions needed will be considerable each single function need to be fast in order for the intervals to be sufficiently short. A minimum set of functions necessary for a reliable operation of an SCT module are stable biasing, thresholds for discriminators, masking of bad channels and calibration and test of the front-end.

In the current LEP experiments the CM circuits are located in the control room with separate wires connecting the experiment for each function. In the LHC environment the material budget and the complexity of the experiment will limit the amount of cables that connect the control room to each detector module. The CM functions can be integrated on the detector module either in a separate CM IC-chip or integrated in the front-end chip. Some control functions such as chip biasing and thresholds are probably better to implement in each front-end chip. Functions such as bias and temperature monitoring are preferably made only once on every hybrid. We propose a CM scheme in which the CM functions are distributed between the front-end circuits and a dedicated CM-chip. The CM-chip serves as a master to the CM-functions distributed on the hybrid or in the CM-chip. The CM-functions are called slaves.

## 2.1 Controlling and Monitoring of the detector module

The hybrid of the detector module, shown in figure 1, will be connected to the control room by a single optical fiber handling data traffic in both directions. A circuit controlling the optical link will split the CM data from the Beam Cross Over (BCO) and Level 1 triggers. The same circuit will also control if data from the CM chip can be sent to the control room.

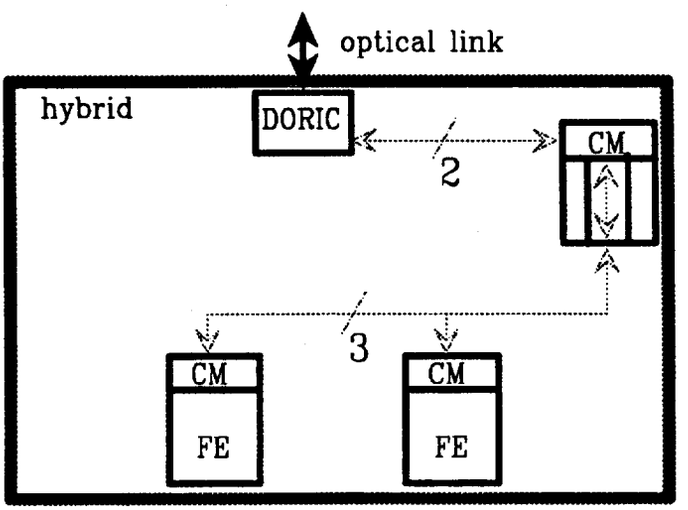


**Figure 1** A schematic layout for a hybrid showing the serial bus between the CM part in the Front End chips and the CM chip.

The CM circuit, shown in figure 2, is built with a serial bus which serves both the slave circuits on the CM chip and the distributed slave circuits on the front-end chips. A Bus Handler (BH) is controlling the traffic on the CM bus and the communication with the control room. The slave circuits performing specific control or monitoring functions are placed on the CM serial bus. Each slave circuit has an address that can be recognized in the data protocol. The modular structure of the CM concept allows extensions to satisfy future needs.
The slave circuits are specialized either for control or monitoring tasks. The aim is to minimize the amount of data that must be sent on the optical link during data taking. This can be achieved by using two protocols. The minimal communication that is needed during data taking will follow a "short" protocol allowing transmission of warnings and important control commands. The circuit will continuously monitoring biasing and temperature conditions on the detector module and send warnings to the control room only when a value is outside a predefined range following the "short" protocol. On request from the control room all biases and temperatures monitored by the CM chip can be transmitted following a "long" protocol[2].

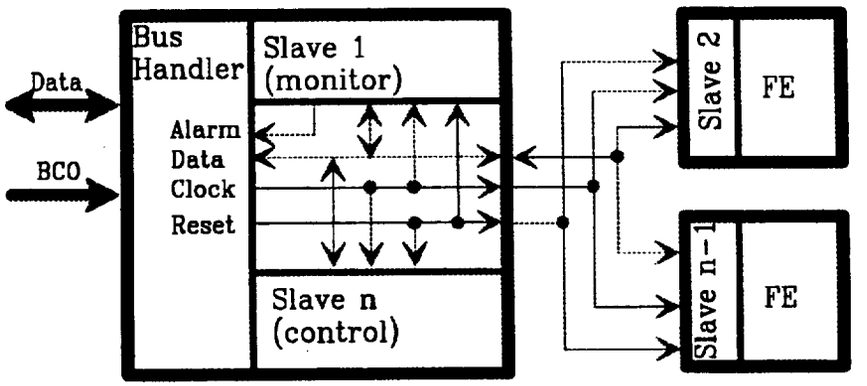


**Figure 2** A schematic layout of the distributed CM circuit.

## 2.2 Protocol for the CM

Each SCT detector module will have a single optical link to control room. The CM data will be folded with the 40 MHz BCO clock. The communication between the control room and the CM chip will always follow a pattern with a request sent from the control room and a reply returned from the CM circuit.
The "short" protocol can easily be sent between triggers. The "long" protocol is needed when the bias settings are transmitted to the front-end DAC and when the monitoring data is transmitted to the control room. The amount of data to be transmitted following the long protocol is usually big and the transmission is preferably done outside data taking. Low priority data is always sent by the "long" protocol.

The "short" protocol consists of:

5 bits preamble , 11101
1 bit header (data type identifier) ,1
4 bits subheader
4 bits command
4 bits counter
9 bits trailer , 100000000

During data taking the CM circuit is regularly receiving data from the control room a few times every minute. The commands sent from and to the control room may be any of the commands listed in appendix A except for the long protocol header. After data is received from the control room the CM circuit will return high priority data. If the High Priority Buffer (HPB) is empty the idle command is returned to the control room. A typical state during data taking is that no actions are requested from the control room in which case an idle command is sent. If the detector module is running well there is no high priority data and an idle command is returned to the control room.

The "long" protocol consist of:

5 bits preamble , 11101
1 bit header (data type identifier) ,1
4 bits subheader
4 bits command
4 bits counter
4 bits address
unlimited bits data
9 bits trailer , 100000000

With the "long" protocol all the tuning of the detector module can be done. The "long" protocol is flexible and allows very long strings of data to be sent to the detector module. This is needed for setting up bias voltages and currents and masking bad channels. When a request or a setting is sent to the CM circuit high priority data is returned to the control room as default. If no high priority data is present then low priority data is returned. If there is no low priority data either then an idle command is returned. It will typically take some microseconds for the CM circuit to process low priority data after a request from the control room. Some requests may need less time for execution than others and to keep track of the sequence every request from the control room has a book keeping number. The request will be cleared when a reply arrives from the CM circuit with the same book keeping number.

## 2.3 Subelements in the CM

Bus Handler (BH)

A functional layout of the BH is shown in figure 3. The BH is the master controlling the communication between the control room and slave circuits on the CM bus. The data coming from the control room is put into a buffer and is forwarded to a subelement in the CM circuit when the serial CM bus is free. Warnings and error messages coming from monitoring functions will be sent to the control room on the first transmission available. When the detector module is working properly no error messages will be issued, hence no data will be sent to the control room unless data is explicitly requested.

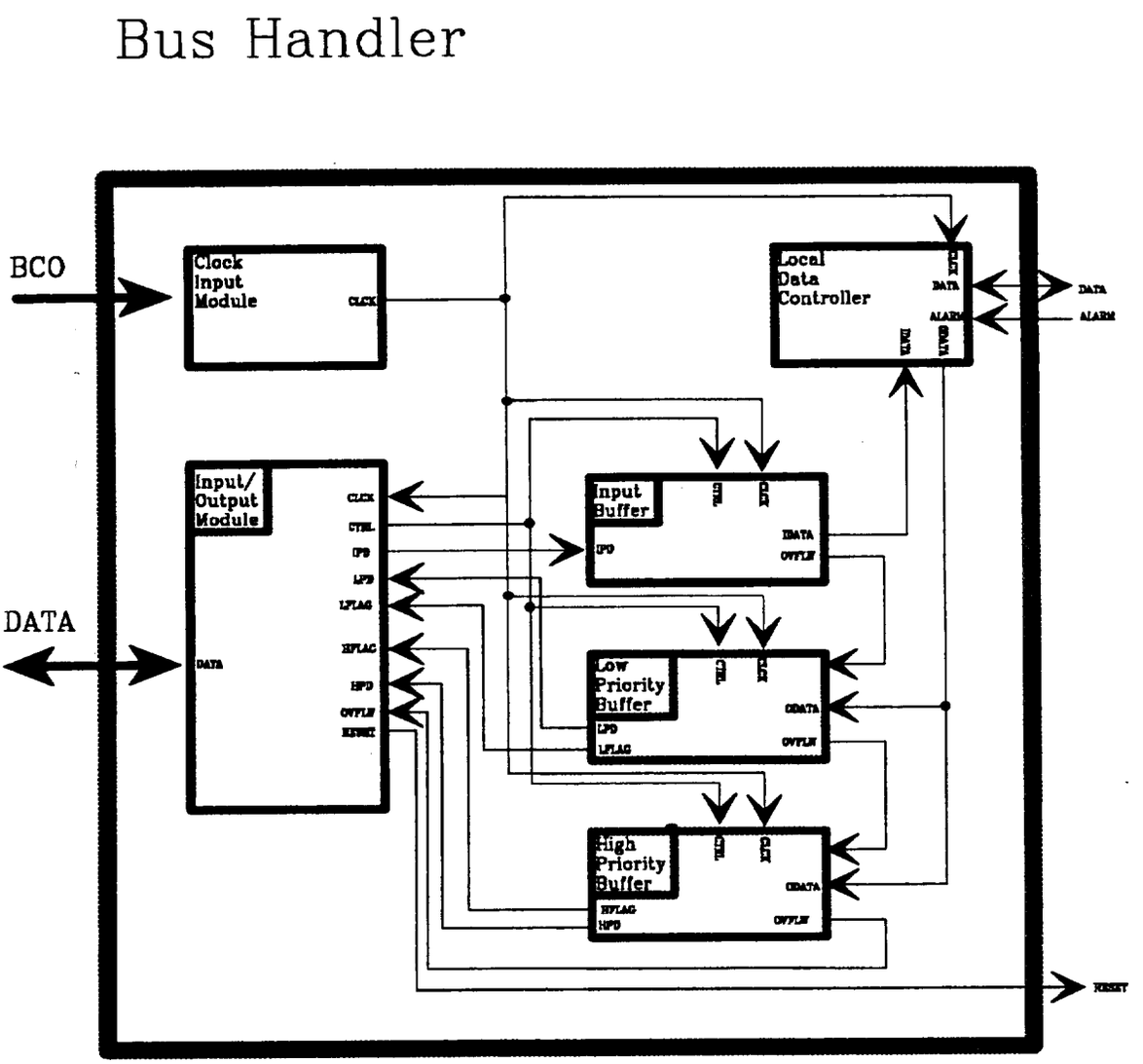


**Figure 3** A functional layout of the Bus Handler (BH).

Clock Input Module, CIM

This subcircuit inside the CM chip receives the BCO clock from the receiver chip for the optical link. The signal is transformed to a frequency suitable for the CM circuit and delivered to the other subcircuits in the CM chip. The signal is labeled CLCK.

Input/Output Module, IOM

The CM data traffic inside the BH is controlled by the IOM. The data sent from the control room is sent to the Input Buffer. If the High Priority Buffer, HPB, has data, High Priority Data, HPD, will be sent to the control room. If "long" protocol is allowed and the High Priority Buffer is empty Low Priority Data, LPD, from the Low Priority Buffer, LPB, will be sent to the control room. The highest priority is given to the High Priority Buffer overflow that will be transmitted before any HPD or LPD. The output buffers, HPB and LPB, sets a flag in the IOM if data present. The IOM controls the buffers by a local a control bus.

Local Data Controller, LDC

The bidirectional data traffic on the CM serial bus is handled by this subcircuit. Data from the input buffer is sent to the slaves and the LDC will wait for a return signal from the requested slave before any other actions are taken. Data arriving from the slaves are put into appropriate buffers.

Input Buffer, IB

The data is kept in the IB until the LDC is ready for transmission. If the IB is overflowed a OVFLW signal is sent to the LPB.

Low Priority Buffer, LPB

The output data from a monitoring slave will be stored in the LPB until the "long" protocol allows the data to be transmitted to the control room. If the LPB is overflowed a OVFLW signal is sent to the HPB.

High Priority Buffer, HPB

The important monitoring data are stored in the HPB awaiting transmission to the control room. This buffer will be constantly read by the IOM. However if this buffer overflows a OVFLW signal is generated and sent to the control room before any other messages.

Internal Bus (IB)

The internal bus consists of essentially two lines, one transmitting the serial data to the slave circuits and one transmitting a reset and other control signals. The clock is taken from the common clock on the detector module.

Slave modules

The slave modules are specialized to a single function. Every slave has a genuine hardwired address. The slave elements can provide biasing, functionality tests, monitoring of voltages, thresholds etc. Table 1 lists the different CM functions with an suggestion where on the detector module the function is implemented.

| Function | Place |
|---|---|
| Setting front-end bias | FE |
| Setting discriminator threshold | FE |
| Masking of bad channels | FE |
| Monitoring front-end bias | CM |
| Monitoring temperatures | CM |
| Alarm generator | CM |
| Functionality test | CM and FE |

**Table 1** The implementation of CM functions on the detector module. FE= front-end, CM= control and monitoring chip

The slave module performing control functions, shown in figure 4, will typically be placed in the front-end chip. The control function generator will be a DAC or a register for channel masking and generation of logical signals for the front-end.

The slave module for monitoring functions, shown in figure 5, will typically be implemented on the CM master chip. The slave module performs analog-to-digital conversion of bias settings and temperature. The internal CM logic signals are listed in appendix B.

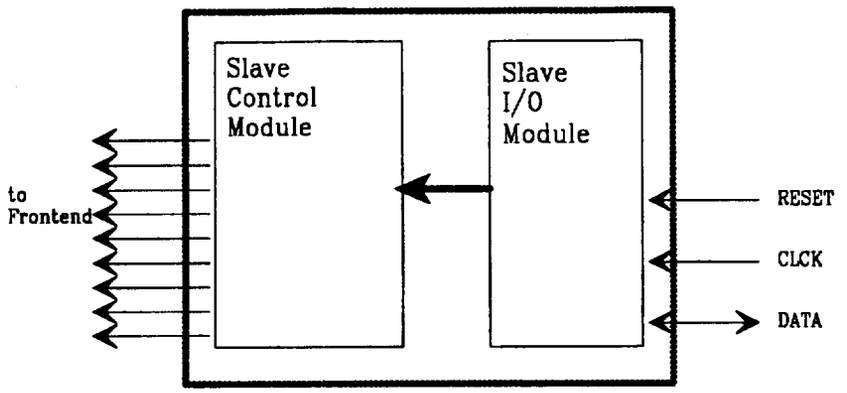


**Figure 4** A schematic layout of a controlling slave module.

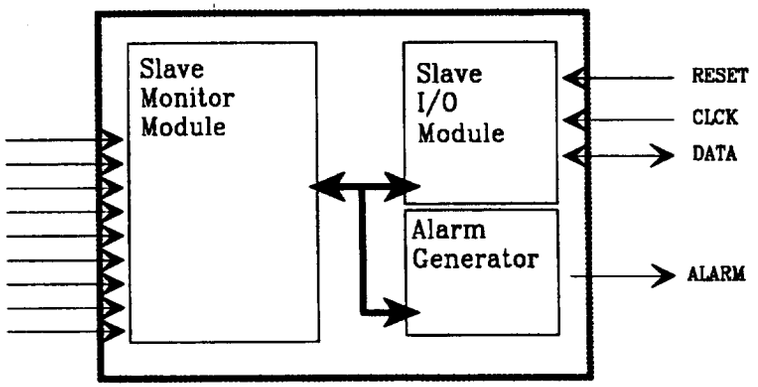


**Figure 5** A schematic layout of a monitoring slave module.

## 3. Development of a prototype Control and Monitoring circuit

A Silicon Strip Detector (SSD) module for ATLAS prototyping in the BSP project is shown in figure 6. The two SSD's are mechanically connected to a hybrid which is equipped with FELIX 128 channel front-end chips and a 128 channel fast **MU**ltiple**X**er (MUX)[3]. The prototype of the FELIX chip was tested 1993[4][5] and a first test of the full FELIX was done in summer 1994. A fan-in plate of quarts with aluminum print glued on top of the SSD connects the readout strips to the denser FELIX inputs.

## 3.1 Control signal levels required by the SSD module

The detector module equipped with FELIX and MUX chips and SSDs have so far been operated by logical signals supplied from the control room in several wires. The voltages and currents are generated with potentiometers placed on the PCB unaccessible for tuning during the test beam. The CM we plan to develop will supply the module with all the necessary control signal for reliable operation except for high voltage polarization of the SSD. The requirements are given in appendix C.

## 3.2 Timing of logical signals

The logical signals are provided in ECL logic by the control room. The signals are the master BCO clock, master RESET and a trigger. All the logic signals needed for the FELIX and MUX will be generated from these inputs. The pattern will be programmed into the CM circuit and the levels needed for the circuits will be generated on the PCB utilizing DACs in the CM circuit. The general timing for the logical signals are showed in figure 7 but the programmable nature of the CM will make it possible to make variations of the timing.

## 3.3 The prototype module

The designs of the components on the hybrid already exist but the module is lacking control and monitoring. The plan is to develop a prototype CM circuit which will be placed on a separate PCB board connected to the hybrid with Kapton cables. The circuit will be implemented in gate-arrays .
Since there is no need for a distributed CM scheme for the BSP all the functions will be contained on a single chip. The primary configuration is: one BH, two slave modules for control and one slave module for monitoring. The specifications for the prototype chip are:

**Input (from control room)**

| | |
|---|---|
| +/- 2V | Power input |
| BCO | 40 MHz continuous clock |
| Trigger | Maximum rate 1 KHz |
| Information Data | Data for programming the CM circuit |

**Output (to control room)**

| | |
|---|---|
| Information Data | Data from the CM circuit |

**Control**

Slave 1

7 currents

8 voltages

Slave 2

| | |
|---|---|
| RESET | Master reset |
| FELIX(T1) | Programmable width (n*BCO) period and delay to trigger |
| MUX(BHOLD) | Programmable delay to T1 |
| MUX(BCLCK) | 20 MHz clock in periods of (m*128) periods started by BHOLD |
| MUX(RBITIN) | Read bit for shift register on the first BCLCK pulse |

**Monitoring**

Slave 1

2-4 voltages

**Precision of components**

Resolution of DACs: 7 bit

Resolution of ADCs: 7 bit

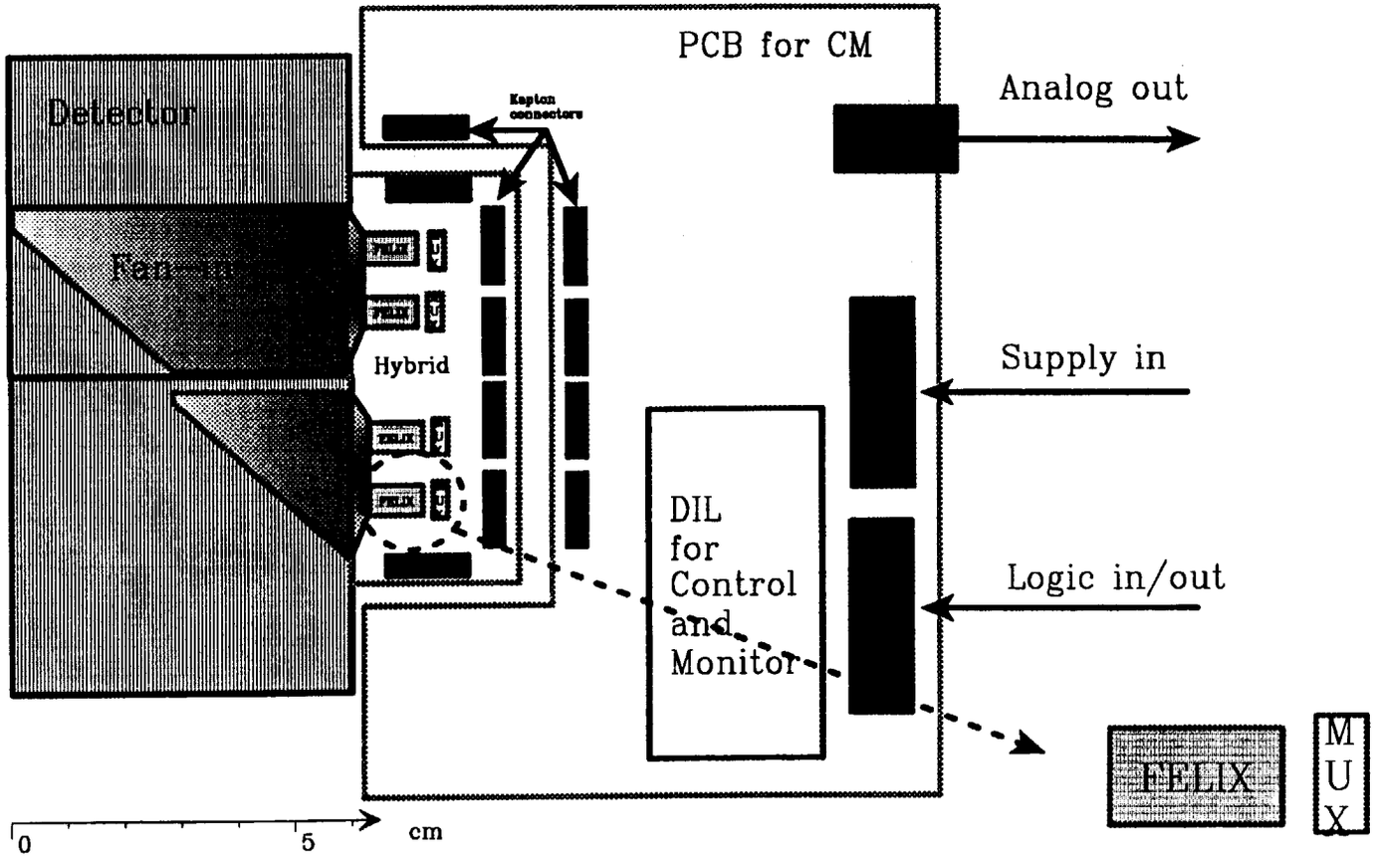


**Figure 6** The ATLAS-type module with a hybrid and a separate PCB for CM.

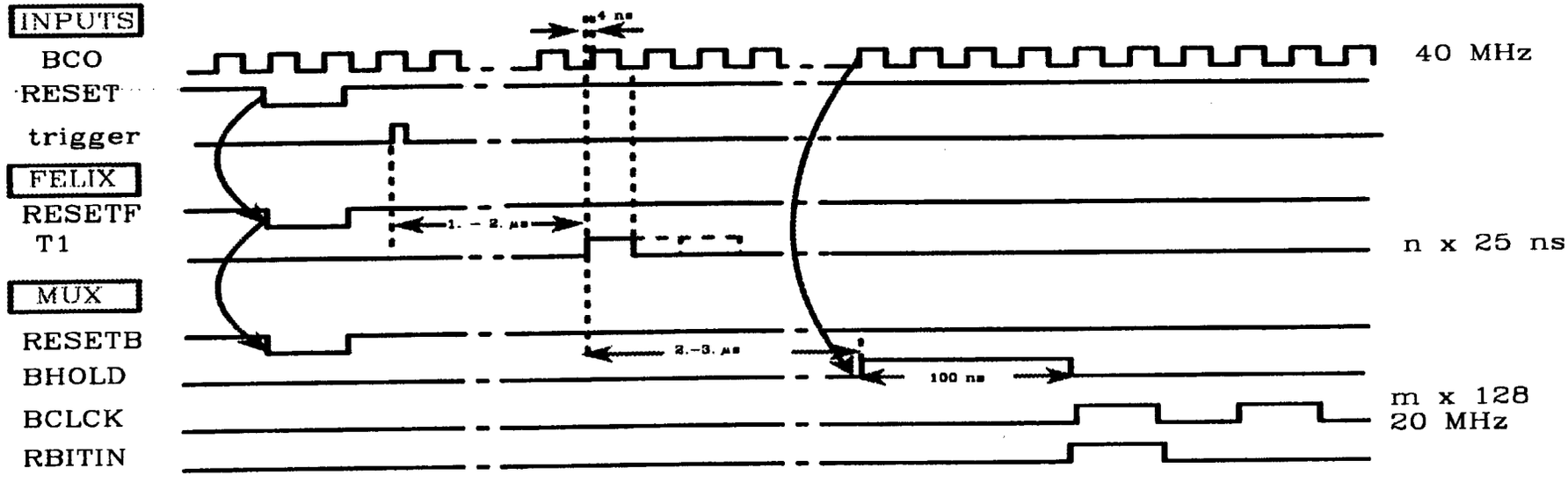


**Figure 7** Timing for logic signals.

### 3.4 The Printed Circuit Board, PCB

The mother board for the CM circuit and the hybrid will be a PCB. The board will have one signal layer on each face and one ground plane in the center. The PCB will carry the encased CM circuit, several discrete components for decoupling and level adaption and an amplifier with linedriver for boosting the analog signal from the MUX on its way to the control room. The PCB will receive power, logic data and output analog and logic data.

## 4. Future development of the control and monitoring scheme

The future development of the CM scheme will continue in close collaboration with the front-end design. A likely option is that the CM will be distributed with slave functions placed in separate chips next to the front-end chip and a separate master chip on the hybrid.
The last step in the development is to implement the control functions in the front-end chip and to manufacture the master CM chip in a radiation hard process

## 5. Acknowledgements

R. Brenner wants to acknowledge NorFA for financial support.

## References

[1] Proposal to Develop a Barrel Sector Prototype of the ATLAS Inner Tracker, June 2, 1994
Draft on WWW:
http://atlasinfo.cern.ch/Atlas/GROUPS/INNER_DETECTOR/BSP/BSPproposal.ps/

[2] ATLAS Technical Proposal, CERN/LHCC/94-43/LHCC/P2, 15 December 1994

[3] J. Kaplon, CERN/RD20-TN31

[4] R. Brenner et al., Nucl. Instr. and Meth. A339 (1994) 477-484

[5] R. Brenner et al., Nucl. Instr. and Meth. A339 (1994) 564-569

# Appendix A

| Command | dec | hex |
|---|---|---|
| Idle | 0 | 0000 |
| Reset | 1 | 0001 |
| ... | 2 | 0010 |
| ... | 3 | 0011 |
| ... | 4 | 0100 |
| ... | 5 | 0101 |
| ... | 6 | 0110 |
| ... | 7 | 0111 |
| ... | 8 | 1000 |
| ... | 9 | 1001 |
| ... | 10 | 1010 |
| ... | 11 | 1011 |
| ... | 12 | 1100 |
| Long protocol from CM disabled | 13 | 1101 |
| Long protocol from CM enabled | 14 | 1110 |
| Long protocol follows | 15 | 1111 |

**Table I** Broadcast command sent from the control room

| Command | dec | bin |
|---|---|---|
| Idle | 0 | 0000 |
| High temperature | 1 | 0001 |
| High Priority Buffer overflow | 2 | 0010 |
| ... | 3 | 0011 |
| ... | 4 | 0100 |
| ... | 5 | 0101 |
| ... | 6 | 0110 |
| ... | 7 | 0111 |
| ... | 8 | 1000 |
| ... | 9 | 1001 |
| ... | 10 | 1010 |
| ... | 11 | 1011 |
| ... | 12 | 1100 |
| ... | 13 | 1101 |
| Low priority data waiting | 14 | 1110 |
| Long protocol follows | 15 | 1111 |

**Table II** Short protocol command received by the control room

# Appendix B

Control signals

| Signal | From | To | Description |
|---|---|---|---|
| CLCK | CIM | IOM, LDC, IB, LPB, HPB | internal clock in the CM circuit |
| OVFLW | IB, LPB | HPB | buffer overflow signal |
| OVFLW | HPB | IOM | buffer overflow signal |
| IPD | IOM | IB | CM data from |
| LPD | LPB | IOM | low priority data from monitoring slaves |
| HPB | HPB | IOM | high priority data, essentially warnings for fast transmission to control room |
| RESET | IOM | Slaves | fast reset of CM circuit |
| LFLAG | LPB | IOM | low priority data present |
| HFLAG | HPB | IOM | high priority data present |
| ECTRL | IOM | IB, LPB, HPB | control signal for writing data to/from buffers to control room |
| ICTRL | LDC | IB, LPB, HPB | control signal for writing data to/from buffers to the slaves |

**Table I** Internal control signals

# Appendix C

| Supply | Value | Description |
|---|---|---|
| AVDD | +2V | analog part of chip |
| AVSS | -2V | analog part of chip |
| DVDD | +2V | digital part of chip |
| DVSS | -2V | digital part of chip |
| VDC | -2V - 0V | back-plane voltage of memory cell |
| VFP | 0V - +2V | feed-back resistance of preamplifier |
| VFS | 0V - +2V | shaping time adjustment |
| DCL | -2V - 0V | source-voltage for APSP amplifier |
| VBP | -2V - 0V | back-plane voltage for weight-capacitors |
| pre_bias | 600 $\mu A$ | current in preamplifier, derived from AVDD |
| sha_bias | 120 $\mu A$ | current in shaper, derived from AVDD |
| lev_bias | 30 $\mu A$ | current for levelshifter, derived from AVSS |
| buf_bias | 80 $\mu A$ | current in buffer, derived from AVSS |
| APSP_bias | 20 $\mu A$ | current in APSP amplifier, derived from AVSS |

**Table I** The supply values for one FELIX chip

| Signal | Level in V | Description |
|---|---|---|
| BCO | 0.2 - 0.5 | clock for pipeline, 40MHz |
| T1 | 0.2 - 0.5 | trigger, active high |
| RESET | 0.5 - 2.0 | reset of pointers in pipeline, active high |
| BUSY | 0.5 | active high |

**Table II** The levels for the logic signals to a FELIX chip, the inverted signals have are the same but with opposite polarity

| Supply | Value | Description |
|---|---|---|
| AVDD | +2V | analog part of chip |
| AVSS | -2V | analog part of chip |
| DVDD | +2V | digital part of chip |
| DVSS | -2V | digital part of chip |
| MPUL | +1V | bias voltage pull-up resistor |
| SFBIAS | 20 $\mu A$ | bias for sample and hold buffer |
| BIASBUF | 150 $\mu A$ | bias for output buffer |

**Table III** The levels for the MUX.

| Signal | Level in V | Description |
|---|---|---|
| BUFCKL | 2.0 | clock , 20 MHz |
| RESETB | 2.0 | reset of shiftregister, active low |
| RBITIN | 2.0 | read bit shifted through the shiftregister, active high |
| BUFHOLD | 2.0 | hold signal to select output from FELIX, active low |

**Table IV** The logic levels for a MUX chip

| Supply | Value | Description |
|---|---|---|
| BKPL | 50V - 200V | detector backplane |
| BIAS | 0.V - 2.0V | detector junction side bias |

**Table V** Supply for the SSD