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Pixel detector back-up Document to support the ATLAS Technical Proposal

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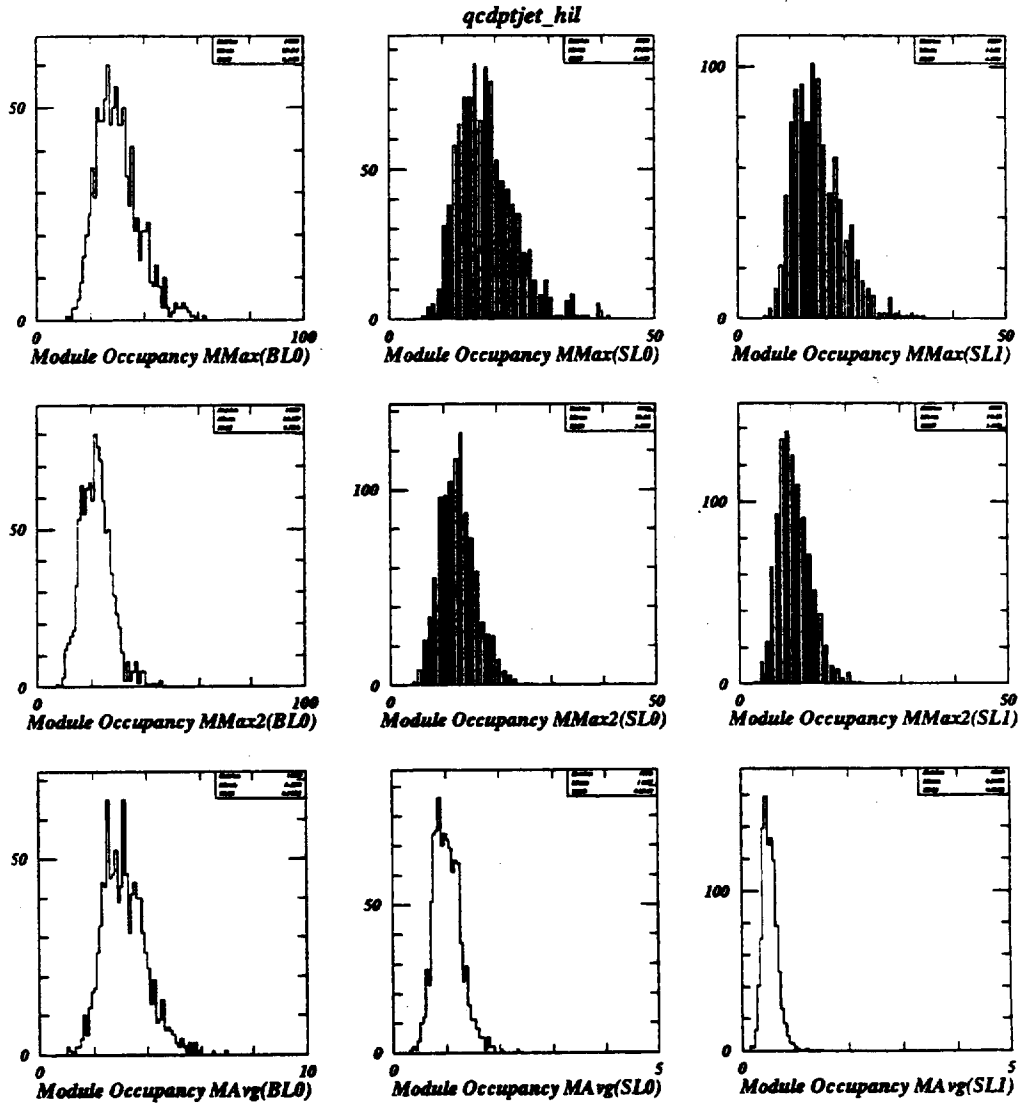


Figure 133: A series of plots for the three Barrel layers of the expected average (AVG) and worst-case (MAX = highest, MAX2 = second highest) module occupancies for 1 TeV Dijet events at a luminosity of 10^{34} .

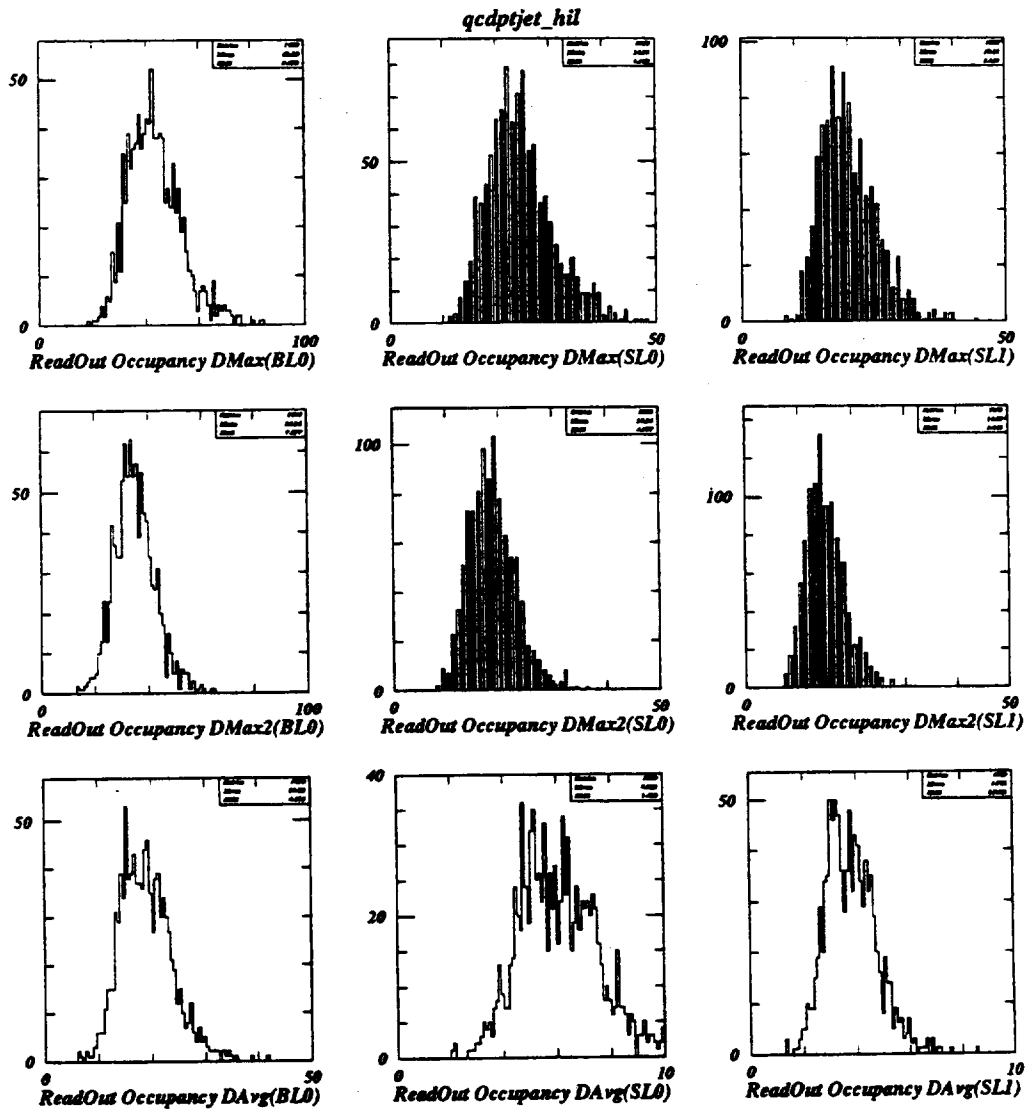


Figure 134: A series of plots for the three Barrel layers of the expected average (AVG) and worst-case (MAX = highest, MAX2 = second highest) readout unit occupancies for 1 TeV Dijet events at a luminosity of 10^{34} .

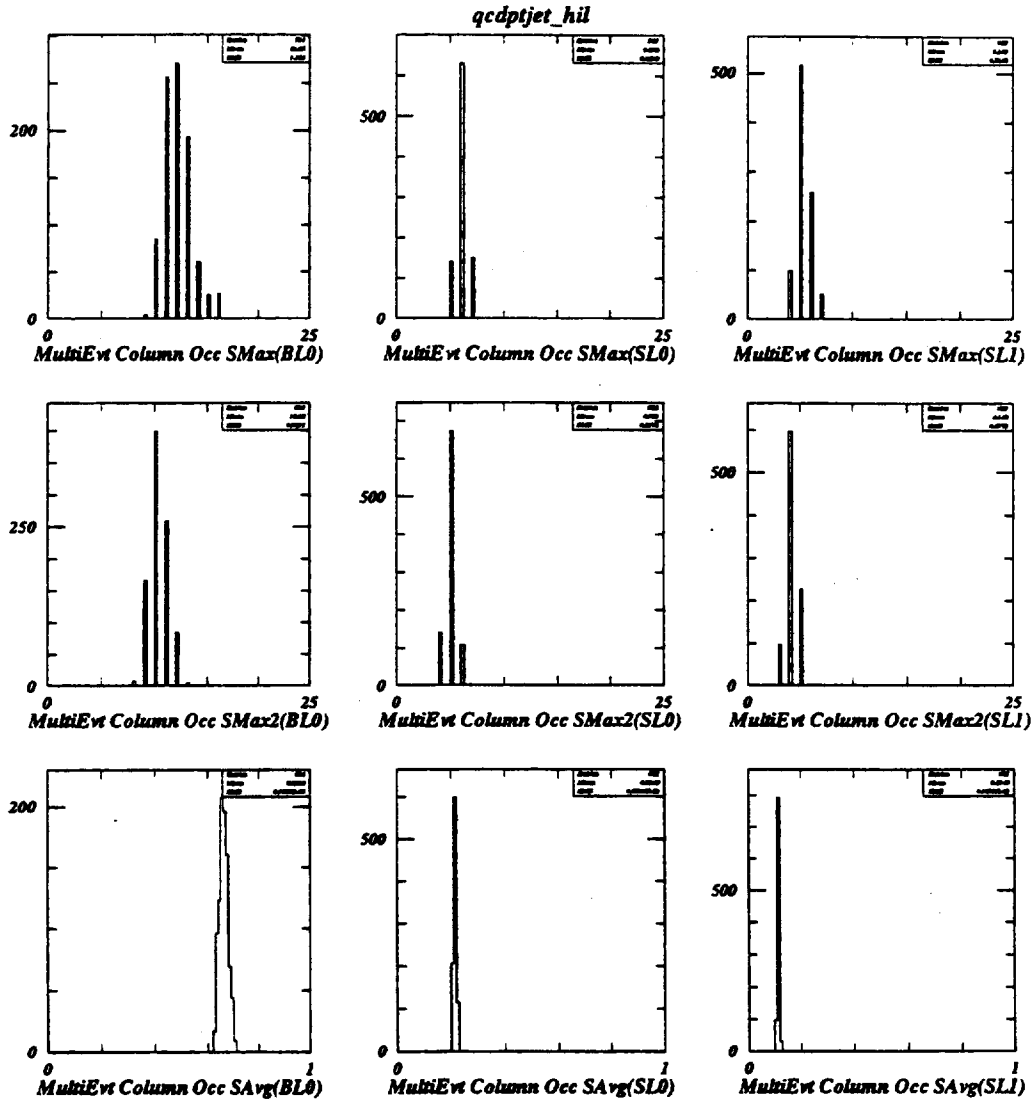


Figure 135: A series of plots for the three Barrel layers of the expected average (AVG) and worst-case (MAX = highest, MAX2 = second highest) column occupancies accumulated over the Level 1 latency period of 80 beam-crossings for 1 TeV Dijet events at a luminosity of 10^{34} .

Table 21: A summary of the probabilities for observing greater than or equal to a certain number of hits in a given pixel detector element at each level in the DAQ system for the different event samples under study. All occupancies are quoted as the number of charged tracks per crossing, where a crossing will include the relevant number of MinBias pileup events for the specified luminosity. The total probability was normalized using only those detector elements in the event which were hit by at least one track, in order to understand the tails of the occupancy distribution for the low occupancies relevant to the pixel detector. For each element, two entries n and p are given, specifying a probability of the form $P(x \geq n) = p$. For most cases, the first n for which $p \leq 10^{-3}$ is given. Note for the barrels, the readout unit is a stave, whereas for the disks, it is a set of four wedges.

| Layer | Column | | | | Chip | | Module | | Readout Unit | |
|-------|----------------------|---------|---|---------|------|---------|--------|---------|--------------|--------|
| | MinBias at 10^{33} | | | | | | | | | |
| BL0 | 2 | 0.001 | 4 | 0.0 | 4 | 0.00008 | 7 | 0.0009 | 15 | 0.0006 |
| SL0 | 2 | 0.0002 | 4 | 0.0 | 3 | 0.00004 | 4 | 0.0009 | 7 | 0.001 |
| SL1 | 2 | 0.00007 | 4 | 0.0 | 3 | 0.00008 | 4 | 0.00008 | 6 | 0.0004 |
| EC0 | 2 | 0.0001 | 4 | 0.0 | 3 | 0.0 | 3 | 0.0 | 5 | 0.0007 |
| EC1 | 2 | 0.00006 | 4 | 0.0 | 3 | 0.0 | 3 | 0.00006 | 5 | 0.0008 |
| EC2 | 2 | 0.00006 | 4 | 0.0 | 3 | 0.0 | 3 | 0.00006 | 5 | 0.0008 |
| | MinBias at 10^{34} | | | | | | | | | |
| BL0 | 2 | 0.005 | 4 | 0.00002 | 5 | 0.0003 | 16 | 0.0006 | 39 | 0.0006 |
| SL0 | 2 | 0.001 | 4 | 0.0 | 4 | 0.00004 | 7 | 0.0004 | 16 | 0.0005 |
| SL1 | 2 | 0.0006 | 4 | 0.0 | 3 | 0.0003 | 5 | 0.0007 | 12 | 0.0004 |
| EC0 | 2 | 0.0007 | 4 | 0.0 | 3 | 0.0003 | 5 | 0.0004 | 9 | 0.0005 |
| EC1 | 2 | 0.0006 | 4 | 0.0 | 3 | 0.0004 | 5 | 0.0005 | 9 | 0.0006 |
| EC2 | 2 | 0.0008 | 4 | 0.0 | 3 | 0.0003 | 5 | 0.0005 | 9 | 0.0005 |

Table 22: A summary of the probabilities for observing greater than or equal to a certain number of hits in a given pixel detector element at each level in the DAQ system for the different event samples under study. All occupancies are quoted as the number of charged tracks per crossing, where a crossing will include the relevant number of MinBias pileup events for the specified luminosity. The total probability was normalized using only those detector elements in the event which were hit by at least one track, in order to understand the tails of the occupancy distribution for the low occupancies relevant to the pixel detector. For each element, two entries n and p are given, specifying a probability of the form $P(x \geq n) = p$. For most cases, the first n for which $p \leq 10^{-3}$ is given. Note for the barrels, the readout unit is a stave, whereas for the disks, it is a set of four wedges.

| Layer | Column | | Chip | | Module | | Readout Unit | | | |
|-------|--|-------|------|---------|--------|--------|--------------|--------|----|--------|
| | Dijets with $P_t(jet) \geq 1 \text{ TeV}$ at 10^{34} | | | | | | | | | |
| BL0 | 2 | 0.021 | 4 | 0.002 | 17 | 0.0008 | 39 | 0.001 | 66 | 0.0009 |
| SL0 | 2 | 0.012 | 4 | 0.0004 | 12 | 0.0008 | 23 | 0.0008 | 36 | 0.0008 |
| SL1 | 2 | 0.009 | 4 | 0.0001 | 10 | 0.0009 | 19 | 0.0008 | 28 | 0.0009 |
| EC0 | 2 | 0.001 | 4 | 0.0 | 4 | 0.0008 | 7 | 0.0005 | 13 | 0.0008 |
| EC1 | 2 | 0.001 | 4 | 0.0 | 4 | 0.0004 | 6 | 0.0006 | 12 | 0.0007 |
| EC2 | 2 | 0.001 | 4 | 0.0 | 4 | 0.001 | 6 | 0.0003 | 10 | 0.0009 |
| | Dijets with $P_t(jet) \geq 0.5 \text{ TeV}$ at 10^{34} | | | | | | | | | |
| BL0 | 2 | 0.012 | 4 | 0.0003 | 11 | 0.001 | 28 | 0.001 | 59 | 0.001 |
| SL0 | 2 | 0.005 | 4 | 0.00007 | 8 | 0.0008 | 16 | 0.0009 | 30 | 0.0009 |
| SL1 | 2 | 0.003 | 4 | 0.00004 | 7 | 0.0006 | 13 | 0.0008 | 22 | 0.001 |
| EC0 | 2 | 0.006 | 4 | 0.00005 | 8 | 0.0008 | 11 | 0.0009 | 21 | 0.001 |
| EC1 | 2 | 0.006 | 4 | 0.00007 | 8 | 0.0007 | 11 | 0.0008 | 22 | 0.0008 |
| EC2 | 2 | 0.005 | 4 | 0.00002 | 7 | 0.0009 | 10 | 0.001 | 20 | 0.0006 |

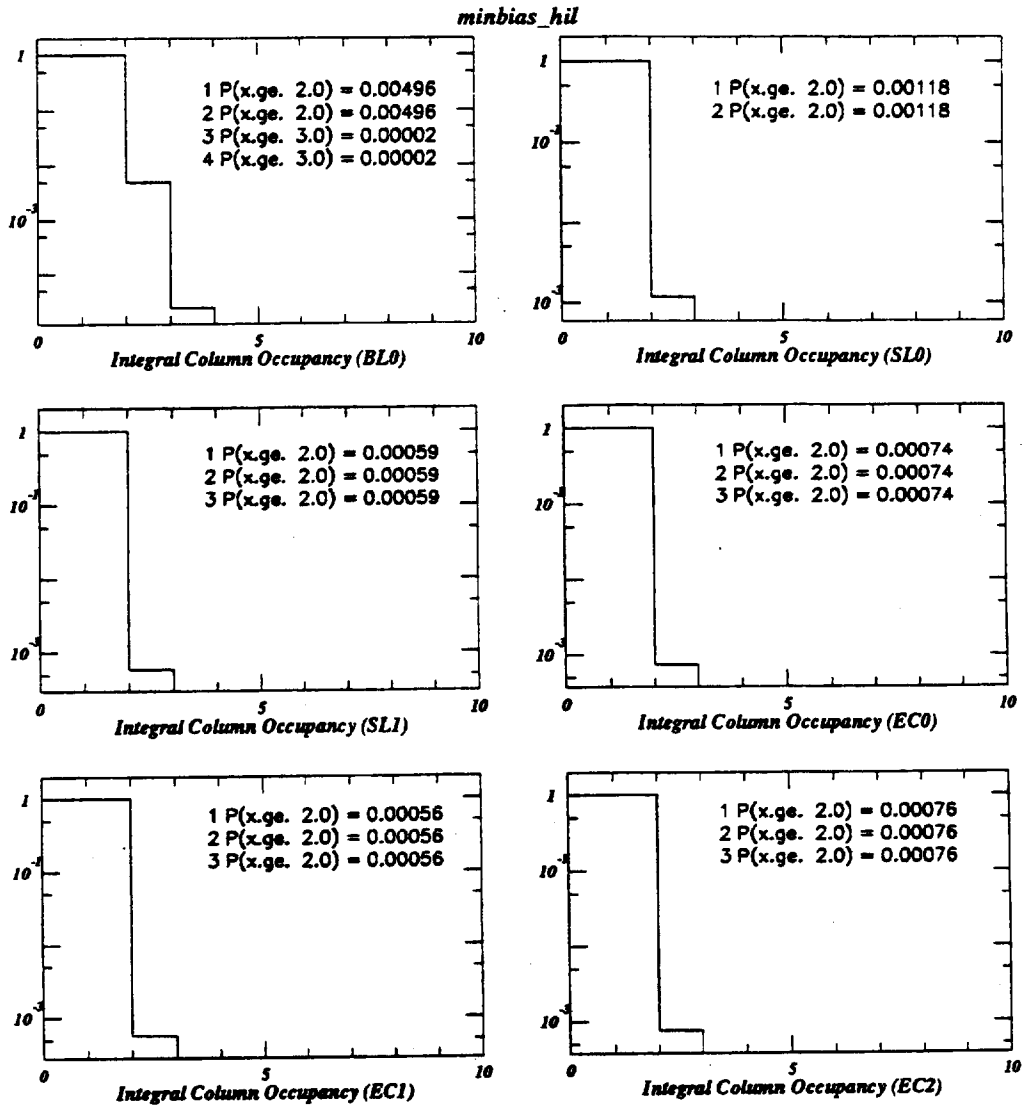


Figure 136: A series of plots for the various elements of the pixel system showing the integral of the column occupancy. The integral is performed from right to left, so that each bin indicates the fraction of detector elements in the sample which were traversed by greater than or equal to the number of charged tracks indicated on the horizontal scale within the Level 1 latency period. The generated event sample was MinBias events at a luminosity of 10^{34} .

minbias_hil

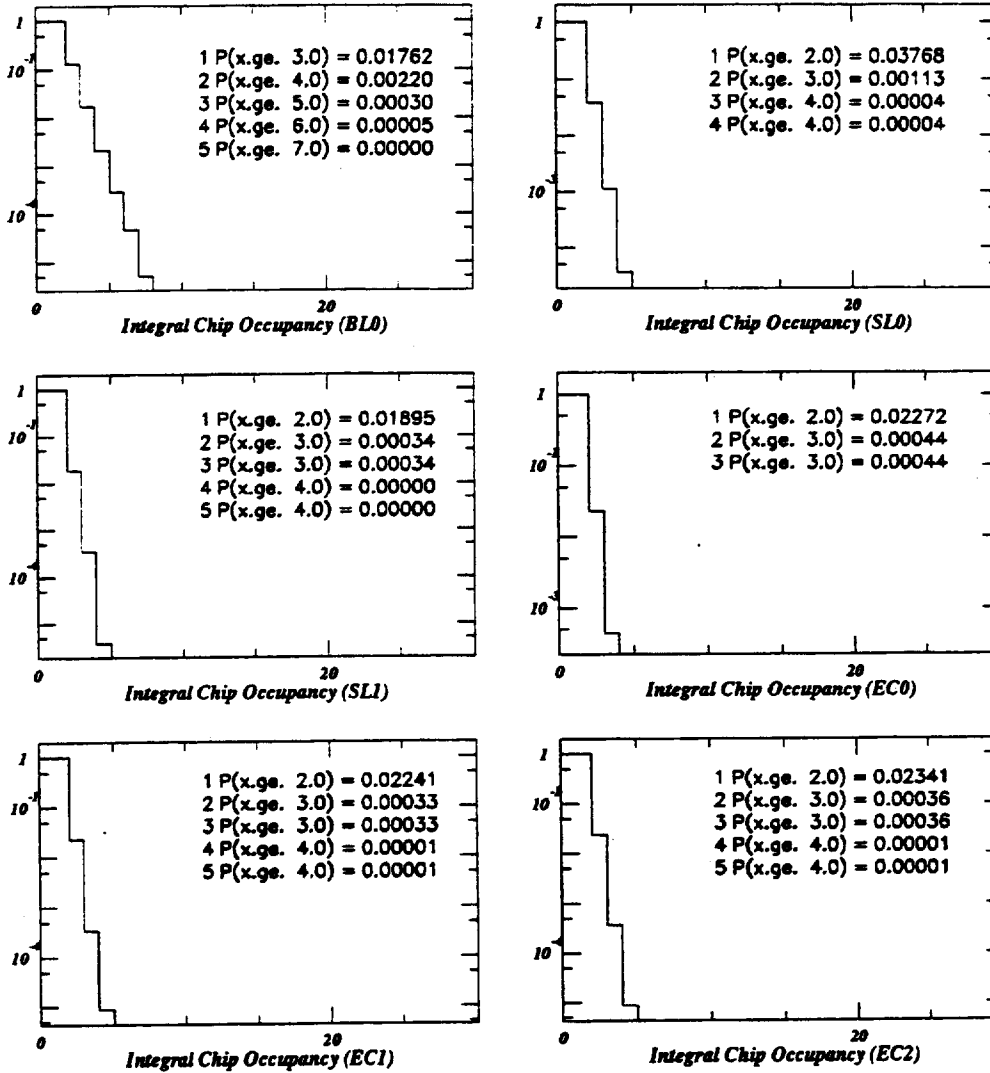


Figure 137: A series of plots for the various elements of the pixel system showing the integral of the chip occupancy. The integral is performed from right to left, so that each bin indicates the fraction of detector elements in the sample which were traversed by greater than or equal to the number of charged tracks indicated on the horizontal scale within the Level 1 latency period. The generated event sample was MinBias events at a luminosity of 10^{34} .

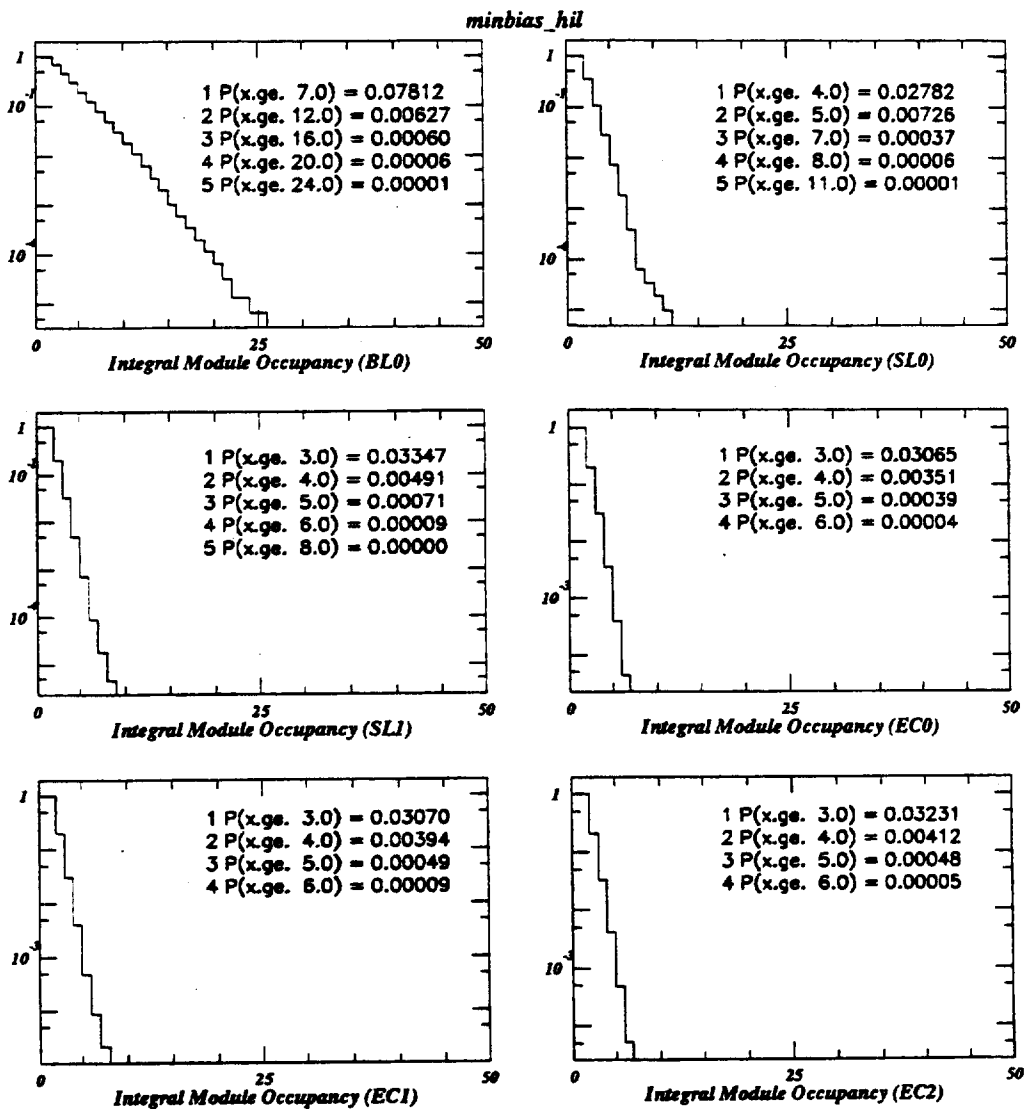


Figure 138: A series of plots for the various elements of the pixel system showing the integral of the module occupancy. The integral is performed from right to left, so that each bin indicates the fraction of detector elements in the sample which were traversed by greater than or equal to the number of charged tracks indicated on the horizontal scale within the Level 1 latency period. The generated event sample was MinBias events at a luminosity of 10^{34} .

minbias_hil

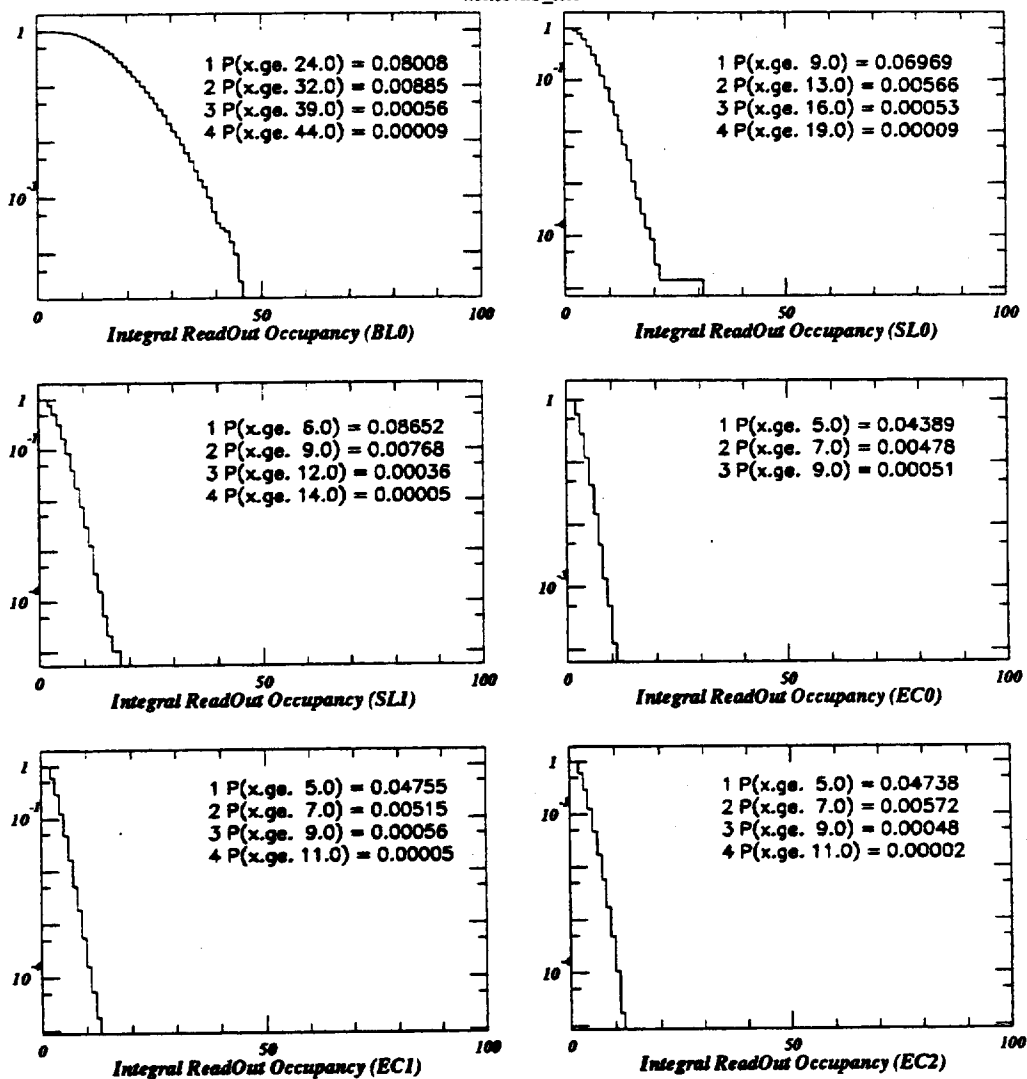


Figure 139: A series of plots for the various elements of the pixel system showing the integral of the readout unit occupancy. The integral is performed from right to left, so that each bin indicates the fraction of detector elements in the sample which were traversed by greater than or equal to the number of charged tracks indicated on the horizontal scale within the Level 1 latency period. The generated event sample was MinBias events at a luminosity of 10^{34} .

minbias_hil

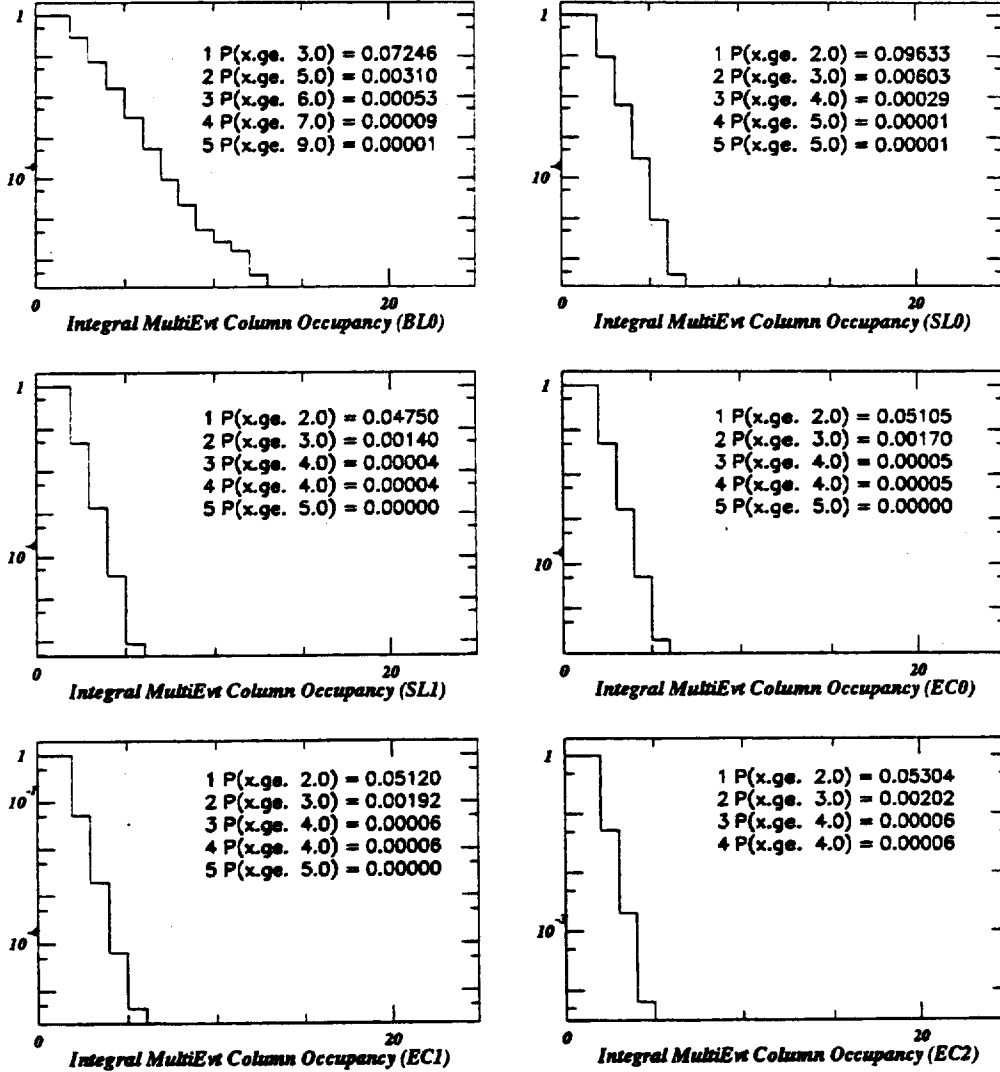


Figure 140: A series of plots for the various elements of the pixel system showing the integral of the accumulated column occupancy for a Level 1 latency period of 80 crossings. The integral is performed from right to left, so that each bin indicates the fraction of detector elements in the sample which were traversed by greater than or equal to the number of charged tracks indicated on the horizontal scale within the Level 1 latency period. The generated event sample was MinBias events at a luminosity of 10^{34} .

3.9.4 Noise Rates

Using a standard formula for noise rates, one expects the following rate:

$$Rate = e^{-Q_{th}^2/2Q_{noise}^2}/4\sqrt{3}\tau$$

where Q_{th} is the threshold charge to fire the discriminator, Q_{noise} is the noise charge, and τ is the shaping time. If one uses the value of $\tau = 20$ nsec, and a threshold of about 1600 electrons (1/16 of a mip for 300 μ thickness silicon), then a noise value of about 400 electrons gives a counting rate of about 10 KHz per pixel. The expected performance of the pixel system after radiation damage is roughly a noise charge of 250 electrons, which gives a completely negligible noise rate of less than 1 Hz per pixel. Hence, in the following discussion, we assume that such electronic noise is completely negligible. Should various kinds of pick-up be worse than expected, the noise performance could deteriorate quickly. Note for reference, if one takes the expected occupancy from MinBias at 10^{34} , and corrects by the estimated factor of ten, then one predicts roughly 1 pixel hit per chip per beam-crossing (see Table 19). This corresponds to a pixel hit rate of roughly 5 KHz when assuming the nominal 40 MHz rate of LHC collisions.

3.9.5 Dataflow Rates

Finally, using the simulation results presented in Section 3.9.3, and applying the estimated factor of ten to convert charged tracks rates to pixel rates, one can make some simple statements about data flows from the ATLAS pixel detector. In making these statements, we have assumed that the hit information from a given pixel requires 32 bits of information: 8 bits of pulse height and 24 bits of address. The large address field is required already at the chip level to transfer the basic information: 8-bit row address, 6-bit column address, and an 8-bit beam-crossing number. Note that it is very difficult to save substantially on this data format by designing a more hierarchical data structure using headers and pointers because of the very low expected occupancy of the system.

A first comment to emphasize is that the optional *b*-layer, which has been assumed to use the same architecture as the remainder of the system, suffers from serious data rate problems at luminosities of 10^{34} (where of course it doesn't survive that long in any case...). The occupancy is substantially higher (roughly by a factor of three) than the rest of the system, leading to special problems in the End of Column buffering, and much higher data transmission rates.

At the Column Level:

1. The average occupancy, in terms of hit pixels, at the column level is 1-2% for the SL and EC layers. It rises to 6-8% for the BL layer at a luminosity of 10^{34} .

At the Chip level:

1. The average data flow from MinBias events at 10^{34} is then roughly 2 pixels per beam-crossing from a BL0 chip, and about 0.5 pixels per beam-crossing from a SL or EC chip.

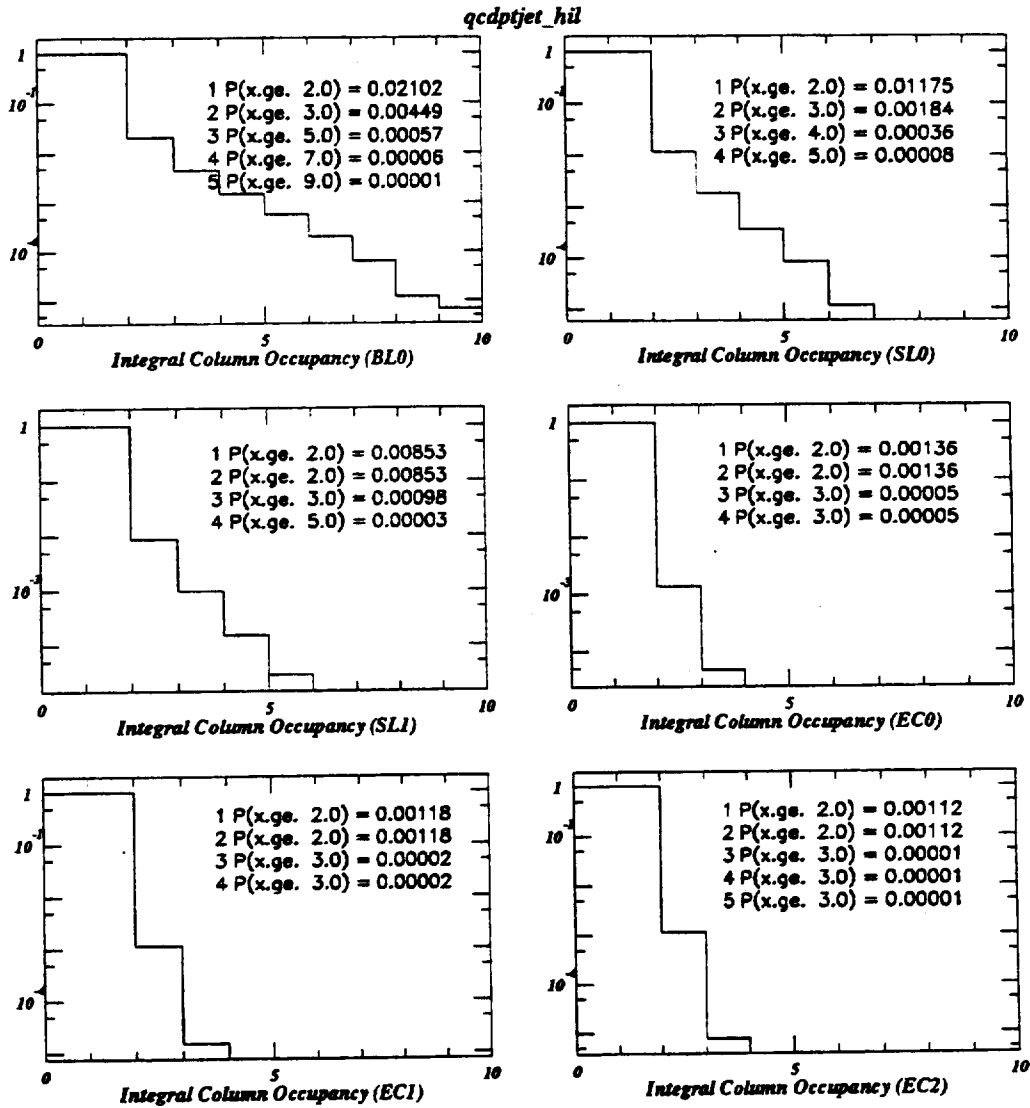


Figure 141: A series of plots for the various elements of the pixel system showing the integral of the column occupancy. The integral is performed from right to left, so that each bin indicates the fraction of detector elements in the sample which were traversed by greater than or equal to the number of charged tracks indicated on the horizontal scale within the Level 1 latency period. The generated event sample was 1 TeV Dijet events at a luminosity of 10^{34} .

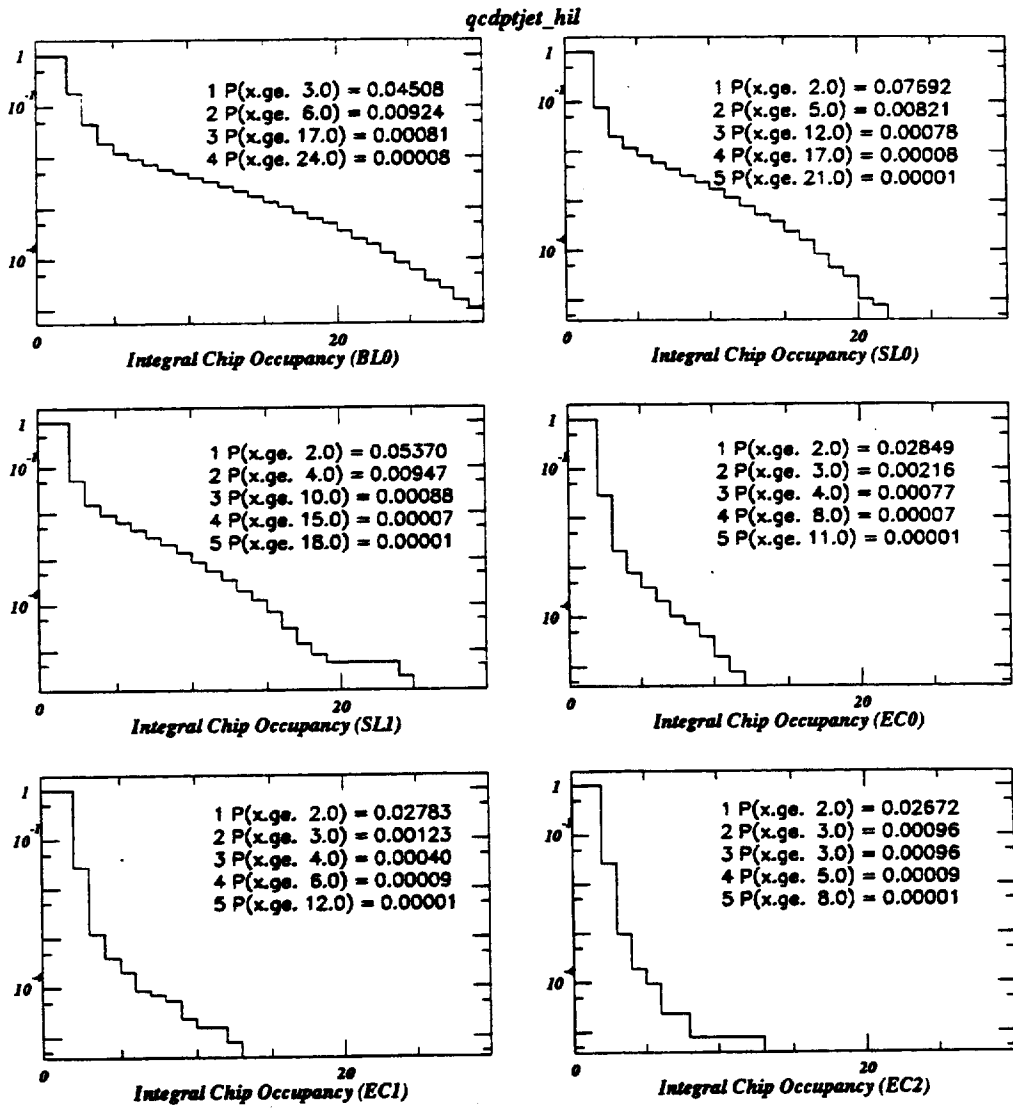


Figure 142: A series of plots for the various elements of the pixel system showing the integral of the chip occupancy. The integral is performed from right to left, so that each bin indicates the fraction of detector elements in the sample which were traversed by greater than or equal to the number of charged tracks indicated on the horizontal scale within the Level 1 latency period. The generated event sample was 1 TeV Dijet events at a luminosity of 10^{34} .

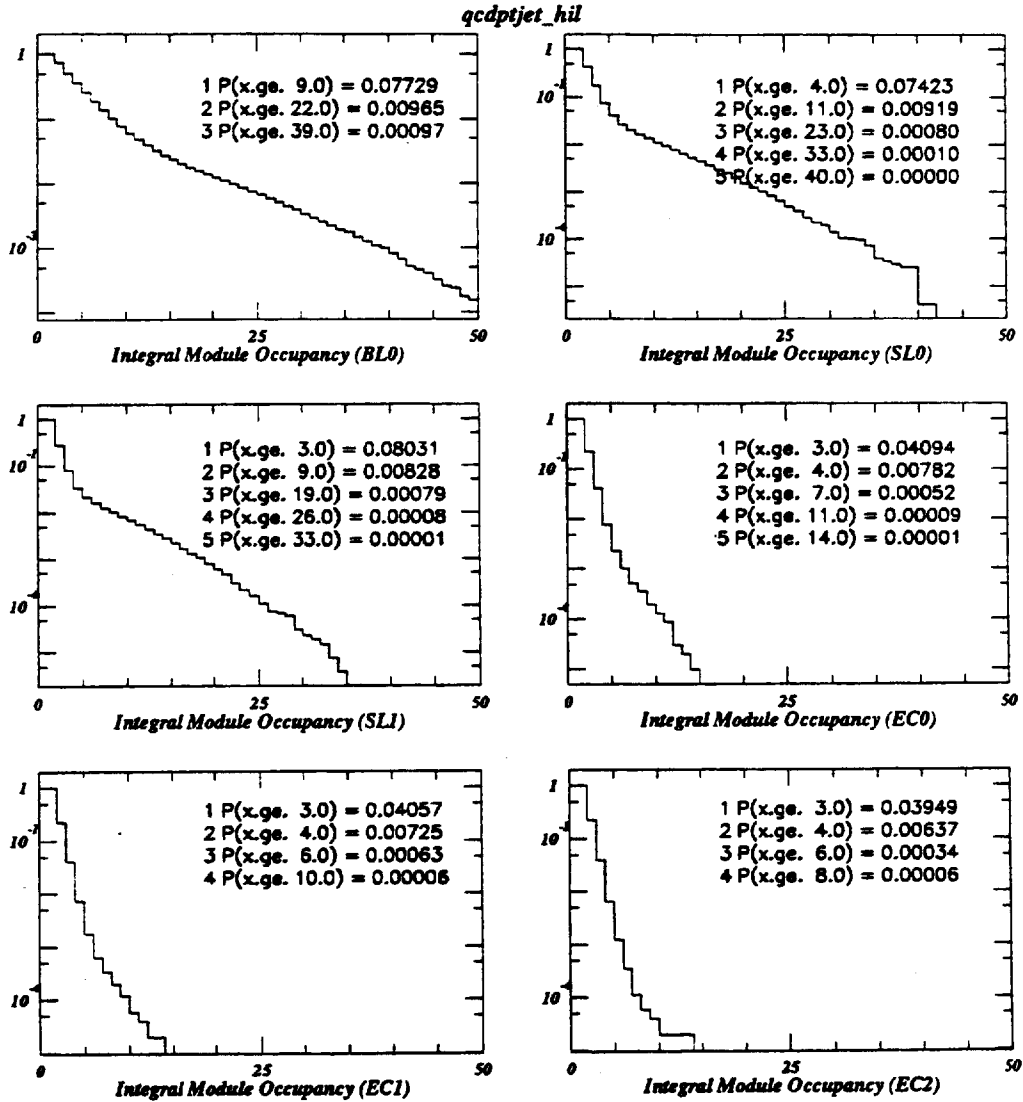


Figure 143: A series of plots for the various elements of the pixel system showing the integral of the module occupancy. The integral is performed from right to left, so that each bin indicates the fraction of detector elements in the sample which were traversed by greater than or equal to the number of charged tracks indicated on the horizontal scale within the Level 1 latency period. The generated event sample was 1 TeV Dijet events at a luminosity of 10^{34} .

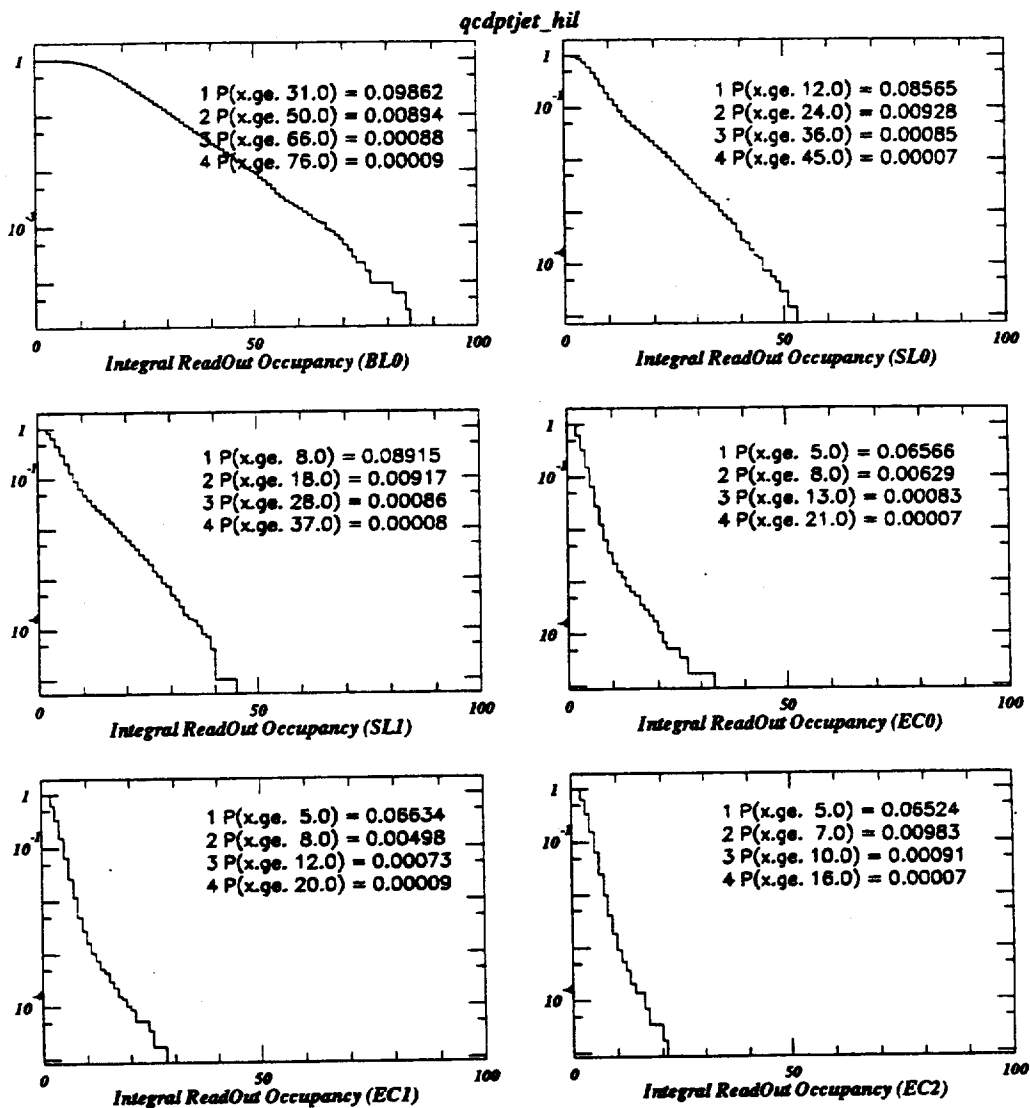


Figure 144: A series of plots for the various elements of the pixel system showing the integral of the readout unit occupancy. The integral is performed from right to left, so that each bin indicates the fraction of detector elements in the sample which were traversed by greater than or equal to the number of charged tracks indicated on the horizontal scale within the Level 1 latency period. The generated event sample was 1 TeV Dijet events at a luminosity of 10^{34} .

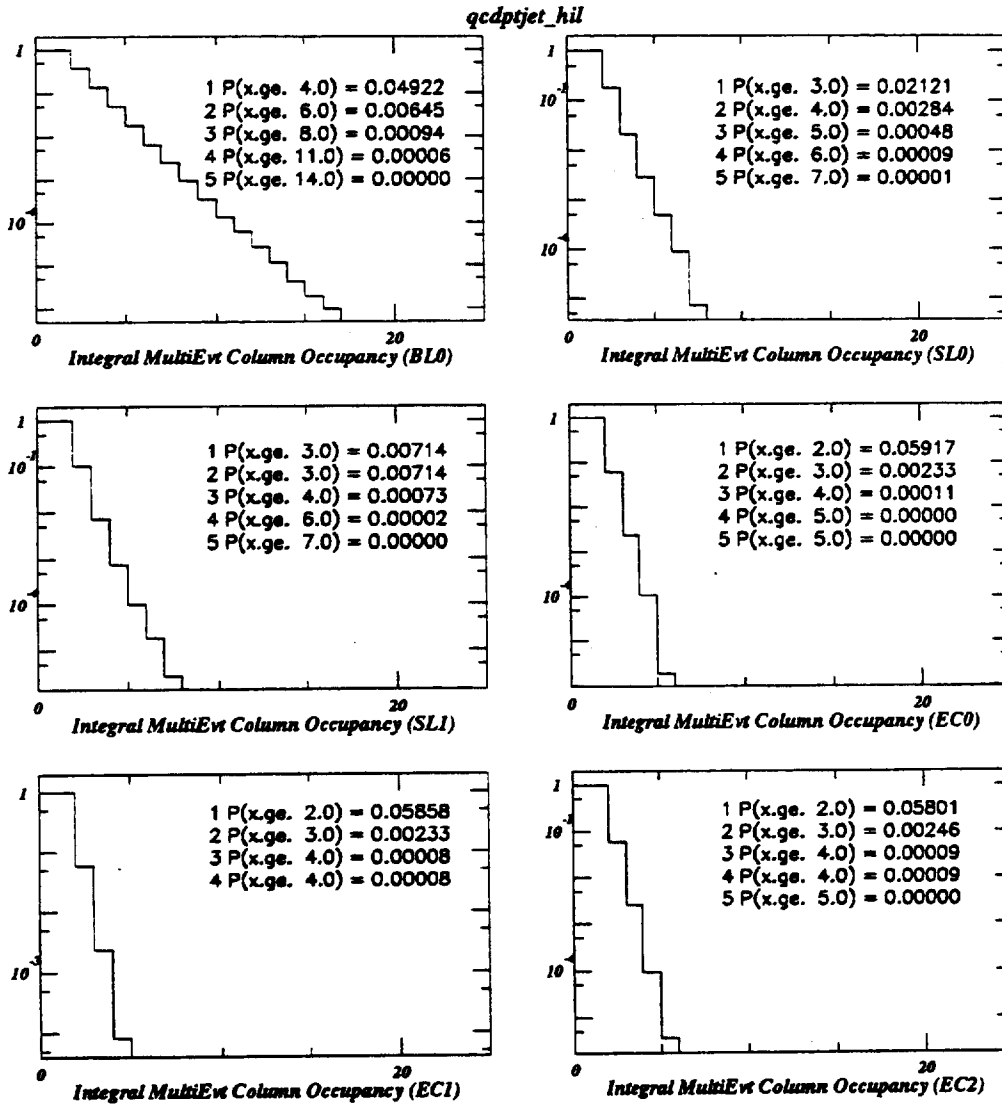


Figure 145: A series of plots for the various elements of the pixel system showing the integral of the accumulated column occupancy for a Level 1 latency period of 80 crossings. The integral is performed from right to left, so that each bin indicates the fraction of detector elements in the sample which were traversed by greater than or equal to the number of charged tracks indicated on the horizontal scale within the Level 1 latency period. The generated event sample was 1 TeV Dijet events at a luminosity of 10^{34} .

2. The worst-case data flow from a given crossing would be about 35 pixels for a BL0 chip, and about 20 pixels from a SL or EC chip.

At the Module level:

1. The average data flow from MinBias events at 10^{34} is then roughly 24 pixels per beam-crossing from a BL0 module, 7 pixels per beam-crossing from a SL0 module, and 4 pixels per beam-crossing from a disk module. Assuming the full 10^5 Hz L1 trigger rate, this leads to a 2-3 MB/sec dataflow from each outer module, and 10 MB/sec from the *b*-physics layer.
2. The worst-case data flow from a given crossing would be about 290 pixels from a *b*-physics layer module, 180 pixels for a barrel module and 65 pixels per module in the disk system. This estimate may be too conservative, because the entire factor of 10 described in Section 3.9.1 has been applied. If one assumes the present estimate for the LBL design of 100 nsec per pixel to transfer the analog information out of a column, and that the chips on a module operate in a strictly daisy-chained manner (a simple-minded design), then the worst-case readout time for such an event, containing 1 TeV jets, would be about 18 μ sec. For the average case given above, the time would be under 1 μ sec, which is small compared to the 10 μ sec Level 1 trigger separation at the maximum 10^5 Hz rate. This suggests that the average transfer rate for pixel data at the chip level could be relaxed to 5 MHz instead of 10 MHz.

At the Readout Unit level:

1. The average data flow from MinBias events at 10^{34} is then roughly 40 pixels per beam-crossing from a barrel stave, and 16 pixels per beam-crossing from a disk unit (which presently consists of four wedges). Assuming the full 10^5 Hz L1 trigger rate, this leads to a 10-15 MB/sec dataflow from each stave in the SL layers.
2. The worst-case data flow from a given crossing would be about 240 pixels for a barrel stave and 110 pixels per readout unit in the disk. If one assumes that the readout is performed by a 1 Gbit/sec fiber-optic connection, then the resulting data would take roughly 8 μ sec, which is within the average separation between triggers at the maximum Level 1 trigger rate. A slower 160 Mbit/sec fiber would be unable to keep up with the average rate, and could lead to significant dataflow problems if the occupancy of the detector were to turn out to be greater than the present estimates.

Finally, we note that the barrel as proposed (that is SL0 and SL1), has a total of 224 staves, which would produce an aggregate dataflow of 2.4 GB/sec for MinBias events at 10^{34} (note this would only increase by 50% if the full 100 KHz Level 1 bandwidth was saturated by 1 TeV jet pairs). The corresponding data flow from the disk system would be given by the 288 wedge readout units producing a total of 1.8 GB/sec. The *b*-physics layer alone, because of its large coverage in pseudorapidity, produces 1.8 GB/sec by itself at 10^{34} , and would exceed reasonable bandwidth limits for fiber transmission on the allocated 32 fibers. At 10^{33} , the data rate is reduced by a factor of seven, and would not cause significant problems. The total system, without *b*-physics layer, produces 4.2 GB/sec of data distributed over 512 optical fibers when running at the maximum Level 1 rate.

Table 23: A summary of the relevant dataflow rates for the ATLAS pixel detector used in the present simulation. The average occupancies to compute these numbers have been derived from MinBias events at 10^{34} . The typical worst-case occupancy for a single beam-crossing at the readout unit level is about 2–3 times larger than the average, so the large data collection area of the readout unit has smoothed many of the fluctuations in local event complexity.

| Layer | NFibers | MB/sec/fiber (AVG) | Total MB/sec |
|----------------------------|---------|--------------------|--------------|
| BL0 | 32 | 57.6 | 1843.2 |
| SL0 | 72 | 17.6 | 1267.2 |
| SL1 | 104 | 10.8 | 1123.2 |
| EC0 | 72 | 6.4 | 460.8 |
| EC1 | 72 | 6.4 | 460.8 |
| EC2 | 72 | 6.4 | 460.8 |
| EC3 | 72 | 6.4 | 460.8 |
| Total (no <i>b</i> -layer) | 464 | - | 4233.6 |
| Total (<i>b</i> -layer) | 496 | - | 6076.8 |

3.9.6. Summary

The present note has summarized a preliminary analysis of the dataflow issues in the ATLAS pixel detector. This study does not yet include a detailed detector model, and so several correction factors have been applied to generate the results. These factors should be somewhat conservative, but it would also be prudent when designing a system of this complexity to include an additional safety factor of order two or more. Note that the present study does indicate that the difference in dataflow between MinBias events at 10^{34} , and more complex 1 TeV dijets, is quite small (less than 50%), hence it should not be necessary to simulate more complex events in order to understand the average data rates. However, the spectrum of fluctuations, particularly at the pixel array chip level, is strongly affected by the presence of high- P_t jets, and the effects of these fluctuations must be included in more detailed simulations.

A summary of some of the preliminary conclusions is given in the following points. The actual dataflow numbers are summarized in Table 23.

1. For the present ATLAS layout, the End of Column logic for the SL and EC layers requires roughly 4–6 buffers in order to avoid losing data during the assumed 2 μ sec Level 1 trigger latency. This assumes that it is possible to collect the useful charge information from a track within a single beam-crossing period. If this is not the case, then it is likely that one will need to double the present average occupancies by collecting pixel information for two successive beam-crossings.
2. A pixel data transfer speed of about 100 nsec per hit pixel to move data from the column level to a module level buffer gives adequate performance with some additional

safety factor. A more accurate estimate of this parameter probably requires a detailed VHDL or MODSIM simulation of the dataflow in order to understand the effects of fluctuations in data volume as the average bandwidth of the data transfers approaches the bandwidth capability of the system. A safety factor of two here is probably appropriate here to avoid unstable behavior of the system. This flow rate requires operating the local buss which connects the individual pixel array chips to the module level buffering at a data rate of roughly 40 MB/sec. In order to support this transfer rate at lower power and with low noise, it may be necessary to use very small digital voltage swings (perhaps as small as 100 mVolts).

3. It seems quite likely that an additional readout chip will be required at the module level, in order to provide the necessary low-latency readout required by the pixel arrays (which have minimal buffering at the End of Column in order to reduce the dead space in the pixel array chip). This readout chip would also provide buffering of the data at the module level, avoiding running the moderately high-speed 40 MB/sec busses described above over long distances.
4. A data transmission scheme in which data is bussed to the end of the barrel cylinders and the outer radius of the endcap disks is preferred, and appears to be feasible using roughly 500 optical fibers. A module level transmission scheme, as proposed by the SCT group, would require bringing roughly 2500 fibers out of the pixel detector (and presumably as many as 2500 clock and control fibers would also be required for input).

3.10 Optical links for the ATLAS pixel detector

3.10.1 Introduction

As explained in detail in the previous section the experimental configuration can be summarized as follows. The total data load from the barrel modules at the nominal luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ is 2.4 GBytes/sec, while the same quantity from the disk layers is 1.8 GBytes/sec. This data rate is evaluated assuming that the complete detector is read out every 1st level (L1) trigger at a rate of 100 kHz and that the data format is defined to be 32 bits/hit pixel. Given the data flow calculated above we propose the following layout: in the barrel region there will be one fiber at each end of a ladder, while for the disk region one fiber will serve four wedges. In summary there will be 512 fibers carrying roughly 4.2 GBytes/sec of data (i.e. 8 Mbyte/sec per fiber).

3.10.2 Digital data transmission via a RD23 optical link

- Transmitter

The proposed transmitter is based on the Asymmetric Fabry Perot Modulator (AFPM) made by reflective Multi Quantum Well (MQW) structure InGaAs/GaAs developed by GEC-Marconi. A scheme of a 4-channel AFPM modulator is shown in figure 146. One of the advantages of reflection modulators is the need of only one fibre, through which the the Continuous Wave (CW) laser light travel together with the light reflected by the MQW. The

signal is the extracted via a coupler at the sending/receiving station, which then acts as an optoelectronic transceiver.

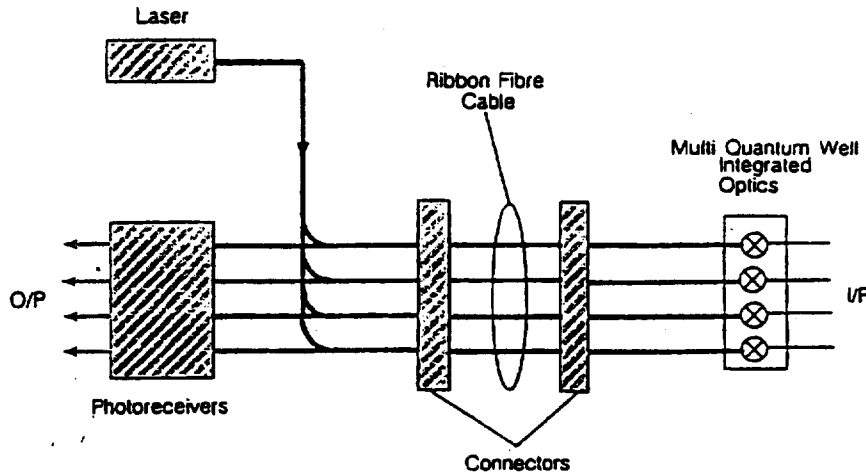


Figure 146: Scheme of a 4-channels AFPM system

The use of essentially passive device as the AFPM modulators, compared to the directly modulated emitters, has distinct advantage in terms of power, radiation resistance and speed. The bench and beam test of a 4-channel AFPM have shown [69] satisfactory performance in terms of speed, S/N ratio and radiation resistance to γ and neutron fluxes. The transmitter has been developed and optimised for analogue optical links for the inner tracker of Atlas and of CMS. The bandwidth and S/N ratio obtained show that the link is suitable for digital data transmission at a bit rate ≥ 12 Mbyte/s (equivalent to a 30 MHz data rate with S/N 150 which has been measured [69]). The electrical and optical required power for one modulator channel in the transmitter array is less than 1mW and does not contribute appreciably to the pixel detector power budget. The final package of the MQW transmitter will be made of 12 channel arrays (8 channels for data transmission and 4 channels for services (clock, etc.)), the fibers will be butt-coupled to the modulator active area using precision drilled spacers which will determine the position and the orientation of the fibers ends with great accuracy, the schematics of this layout is shown in figure 147.

Fibers ribbon is attached to a transmitter and the fibers are single mode type made with pure silica core fluorine doped (PSC/F₂). The packaged array has a footprint of 8x10 mm² and an height of 6 mm. This dimension fit well with the different layers of pixel detector . Infact for each end of the two barrel layers the total number of 8-channel transmitters is 14 (= 140 mm) that fit well within the total length of the two circumferences. Tha same is true for the disk and for the B layer. For the radiation hardness one must remember that the 1 MeV equivalent neutron fluence level at 11,5 cm layer for $L=10^{34}$ cm⁻²s⁻¹ is about $8.3 \cdot 10^{13}$ cm⁻² per year and the total dose is between 1 and 2 MRad per year. Recent measurements [69] made on modulator at $1.3 \cdot 10^{14}$ cm⁻² and with an irradiation of γ from ⁶⁰Co equivalent to 20 MRad at a rate of 205 Krad/hr show very small variation in spectral reflectance for neutrons and no variation at all for gammas. A change of the reverse current from 5nA to 100nA has been observed in some of the MQW; this has no pratical relevance and is probably due to surface effects, as shown in figure 148.

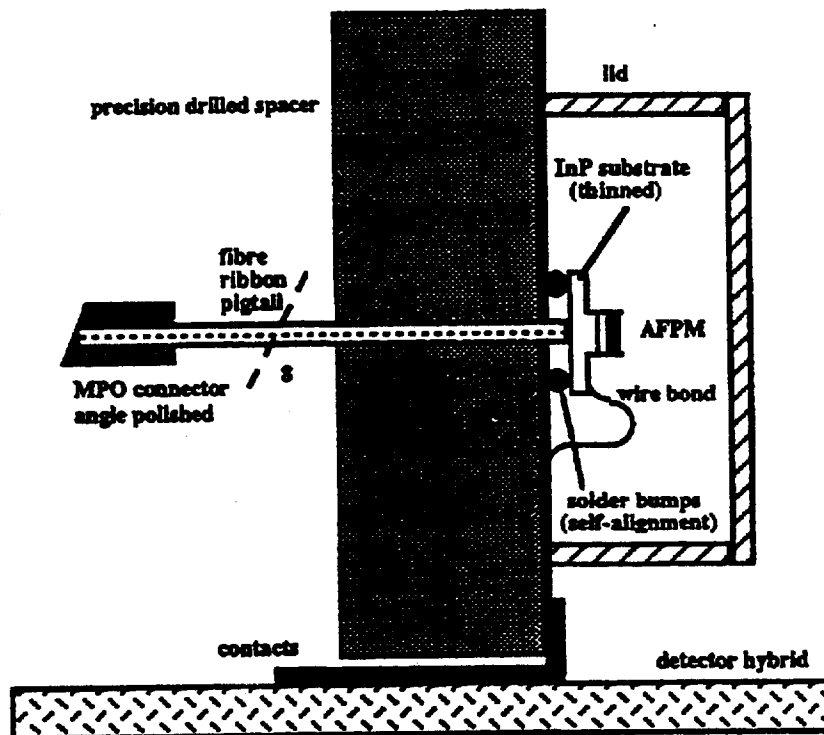


Figure 147: Schematic of butt-coupled MQW

This effect is reversible and full recovery is observed in all cases (figure 149)

- Optical fibres

70m of PSC/F₂ single mode fibers have been irradiated by neutrons and by γ (same conditions as for the MQW modulators). No significant effect is expected after 10 years of LHC operation taking into account the fluence rate and the fibre recovery. The larger effect is the one induced by γ irradiation (figure 150) , but the overall induced attenuation will be less than 0.6 dB after 10 year on the length of the fiber going from the detector to the trigger room. These results show that the transmitters and the single mode fibers are radiation resistant at level of fluences and doses to which the pixel detectors must cope with.

- Transceiver

The transceiver (laser/coupler/photodiode) exists to-day but uses discrete components and it is therefore not suitable for large scale production. A hybrid or monolithic version must be provided. The hybrid version can be developed more quickly than the corresponding monolithic and several technologies (OEIC) are presently being investigated. The preferred solution is a planar opto-hybrid on Si substrate. Silica-on-silicon waveguides allow for high efficiency coupling to optical fibres, aligned using V-grooves. Lasers and photodiodes are die components bump bonded on the substrate. Prototypes of this solution will be prepared, in the framework of RD23, by the end of 1995.

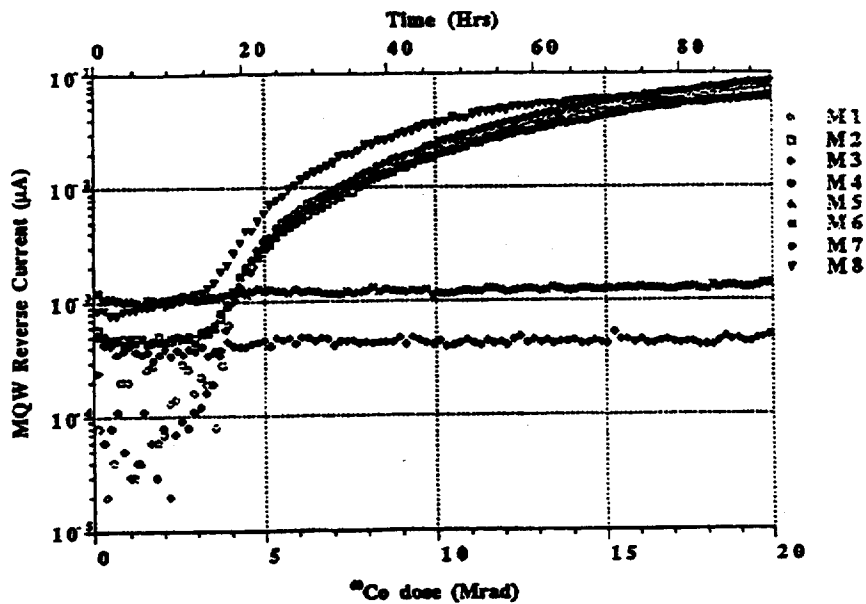


Figure 148: Leakage current under gamma irradiation for MWQ samples

- Receiver board

The transceiver will be assembled with the readout electronics on a VME board. The receiver board will be simplified with respect to the analogic case because many functions will be made on the front end electronics. The transimpedance linear preamplifier will be followed by a commercial electrical bit regenerator before storing the digital information into local memories that will be addressed by the 2_{nd} level trigger processors and, later, by DAQ computers .

3.11 Pixel Readout Electronics

The pixel detector is composed of about 1.5×10^8 pixels contained in about 3×10^4 front-end chips. The electronics is composed of two parts: — the on-detector and off-detector electronics. Figure 151 shows an example of the relationships among the major blocks of electronics. The function of the on-detector electronics is to detect hits, save them pending a Level 1 trigger and read out the hits defined by the trigger. The function of the off-detector electronics is to provide services (power and high voltage), clocks and control (commands such as trigger and control register values) for the on-detector electronics and the buffering of event data for transmission to the DAQ and Level 2 trigger processors. The numbers in this section, and in figure 151, are presented in the context of the LBL design and the data flow rates given in section 3.9 without the B-physics layer.

3.11.1 Pixel Electronics On-Detector Basic Functionality

The on-detector electronics is comprised of the front-end chips, a smaller number of readout and control (ROC) chips and multiplexing electronics for input/output to/from optical fibers.

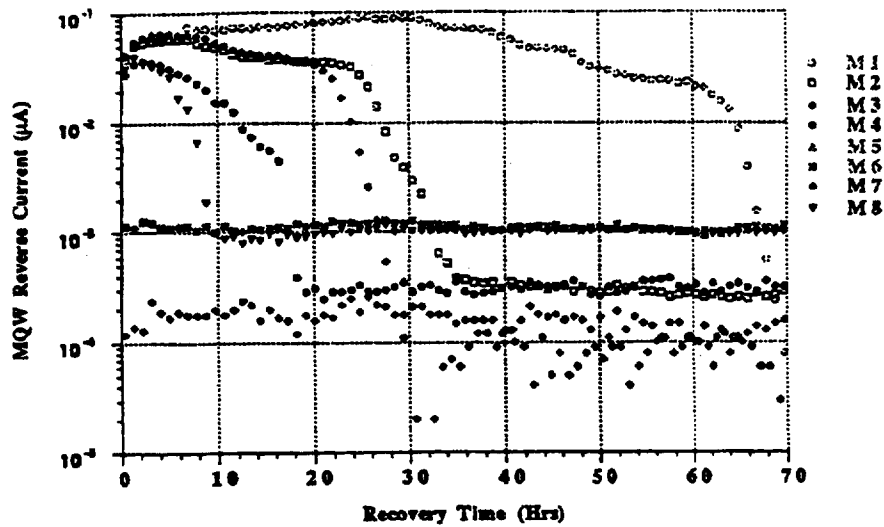


Figure 149: Leakage current under recovery for MWQ samples

The number of the multiplexing (readout units) is not yet well defined but we assume here that 4-6 ROCs will be included in each readout unit as defined in 3.9 — one-half of barrel stave and four disk wedges. After a Level 1 trigger accept, the data will be digitized and readout to the off-detector electronics. Other function that must be supported are test pulse injection and masking of defective channels or chips.

3.11.1.1 Interfaces to the On-Detector Electronics The interface is composed of the following items (see figure 152):

- a. Data to the off-detector electronics. This data link is optical. The exact speed and number of links is under discussion, but we assume here the minimum number of links, which is about 500. If greater bandwidth is required, additional fibers would be needed. These could be implemented as additional fibers per readout unit or by increasing the number of readout units e.g., one fiber per module. The difference between the two is a matter of the amount of multiplexing and resulting fiber speed. Functionality is the same for the options. Data rates for the minimum fiber option are given in section 3.9. Detector data are delivered by the fibers to receiver cards.
- b. Clock, commands and control. This link is composed of optical fibers that contain the following information:
 1. Clock at the beam crossing frequency,
 2. Level 1 trigger,
 3. Control information composed of reset, master reset, data to set control functions, etc. Definition and protocol of these signals is yet to be completed but the general classes of information given above must be supported.

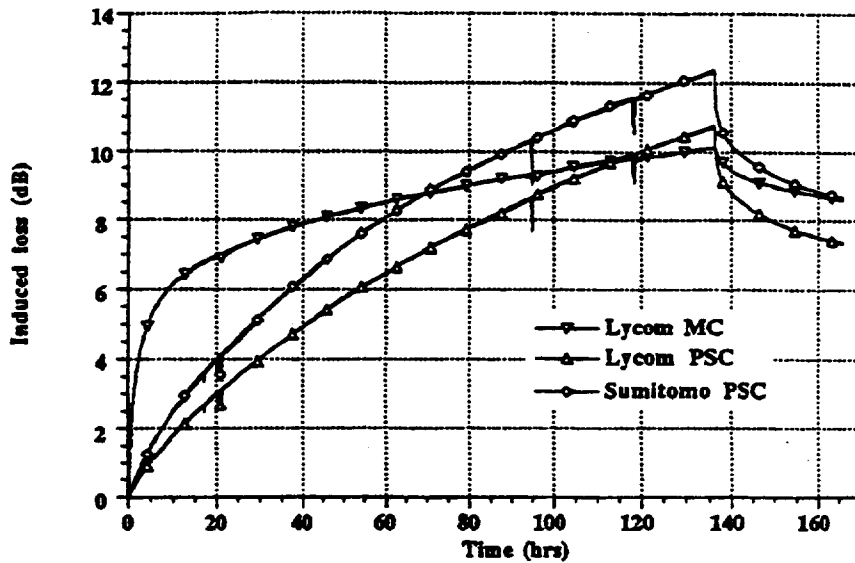


Figure 150: Time profile of induced loss and recovery after 20 MRad γ irradiation (fibre length = 90m)

c. Services

The services are composed of detector high voltage, DC power, analog level for control (test pulse amplitude and thresholds) and temperature monitors. It should be noted the analog levels could be generated in the on-detector electronics. Service cables will be designed to provide a minimum number of radiation lengths.

3.11.1.2 Pixel Readout Chip and Detector The electronics for the pixel front-end chip has been described previously. Here we will assume that after a Level 1 trigger accept, a pixel column or the readout control will have stored the desired hits and their correlation to the 8 bit beam crossing counter. Functionality of the readout control and optional ADC circuitry is to gather the data from a given crossing and place it in a 32 bit \times 64 deep FIFO. Data stored are a 6–8 bit amplitude, 8 bit crossing counter, 8 bit row location, 5 bit column number and 1 bit to indicate no data. The length and location of the buffer memories requires more optimization.

Data from the 32 \times 64 FIFO are pushed to the next level of multiplexing in a serial format. Serial format has been picked to reduce the number of lines on the module hybrid. The derandomizing buffers in the front-end chips allows the serial lines from each front-end chip to be operated at a frequency as low as 10 MHz if needed and consistent with the average event rate. However, large events will require a readout time that exceeds $2^8 \times 25 \text{ nsec} = 6.4 \mu\text{sec}$, in which case the 8 bit crossing counter could repeat, potentially causing confusion in building events. The solution to this problem requires further study, but one cure would be to add more bits to identify the trigger time.

Control of registers (mask, test, etc.) is accomplished by a serial slow control link that provides for the setting of pixel masks, test pulse enables and counter offsets. Serial format

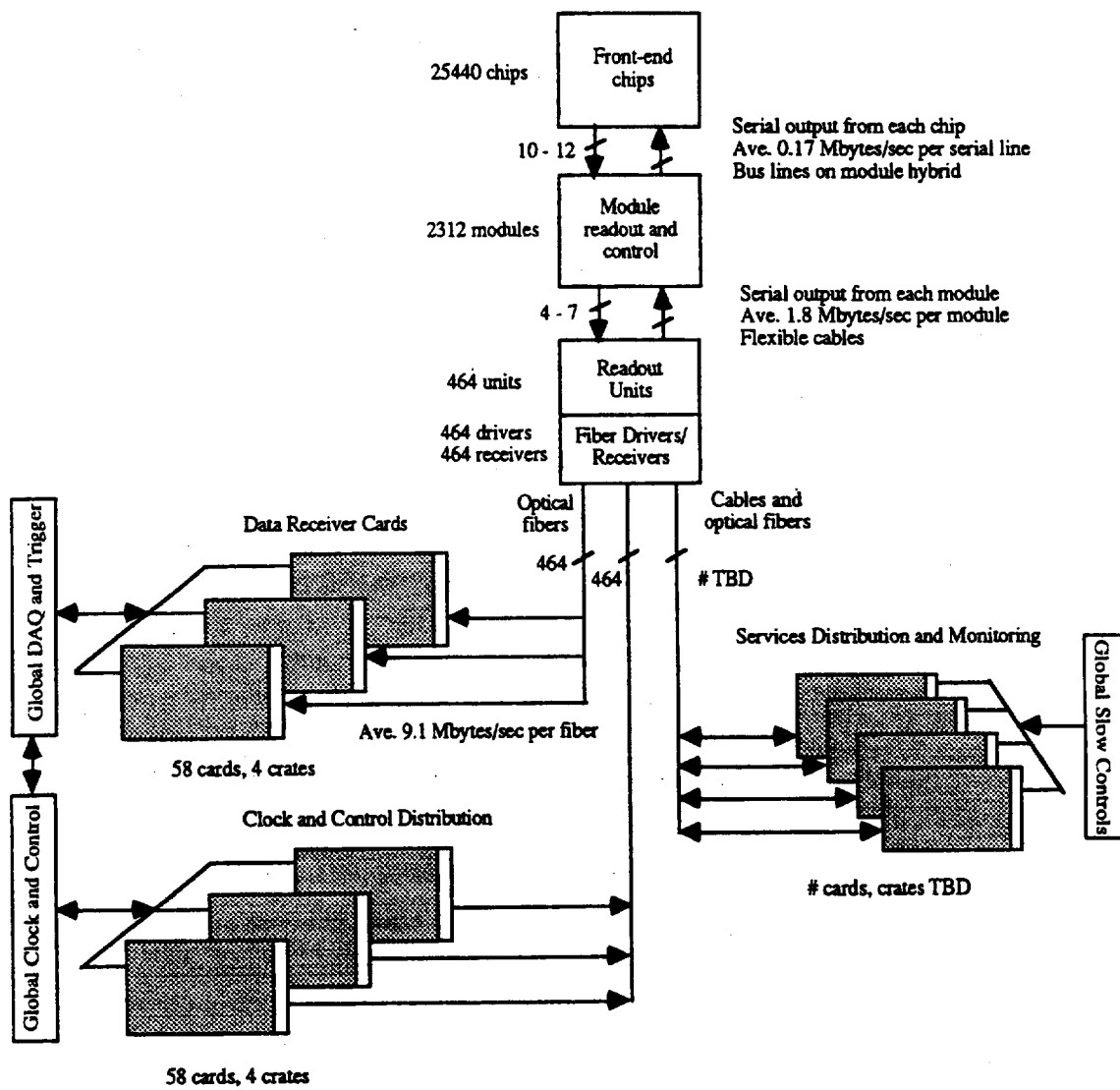


Figure 151: An example of the pixel data flow architecture

On-detector Pixel Electronics

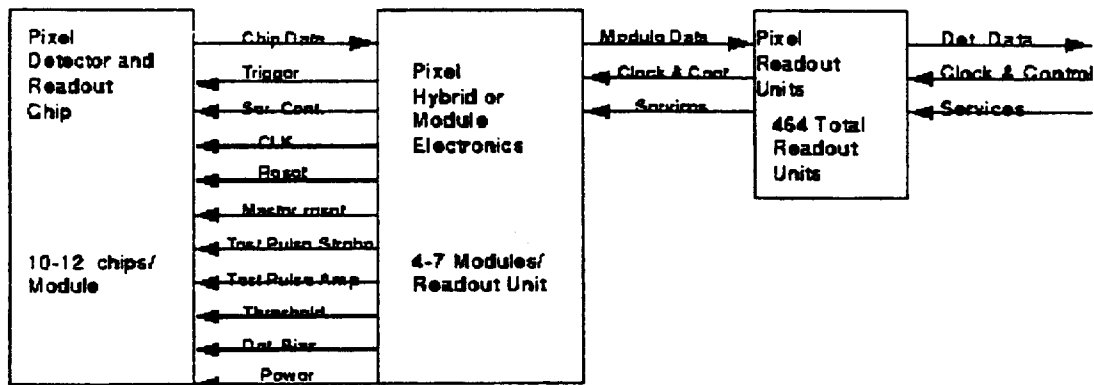


Figure 152: On-Detector Pixel Electronics.

has been chosen to reduce the number of lines on the hybrid.

3.11.1.3 Pixel Module Electronics There are approximately 2500 pixel modules. The pixel module electronics has two main functions. One is to receive the front-end readout data and build a mini-event. The other is to decode the clock and control data to support the pixel front-end chips. These functions are shown in figure 153. Services consisting of power, detector high voltage and analog voltages for test pulse amplitude and thresholds are fanned out to the front-end chips supported on a module. Clock and control is composed of several signals. There could be the following lines/signals: clock at the beam crossing frequency and 3 lines/bits of command (decoded as trigger, control with serial data following on these lines, strobe test pulse, reset, master reset, etc.). The exact details will be defined at a later time.

It is necessary for the pixel module electronics to know what the trigger identifiers are and what order they will arrive from the read out chips. This is accomplished by duplication of the 8 bit crossing counter with an offset that is used to validate a trigger on the readout chip in the 8 deep trigger FIFO that keeps track of triggers. Each data source is stored in a 32×64 word FIFO. Events are built and transmitted by circuitry that reads the next trigger number from the trigger FIFO. Then the data storage FIFOs are scanned for hits belonging to that trigger number. The hit data is transmitted from the module in serial format to the next layer of multiplexing. Four bits of address must be added by the module electronics to identify the chips on a module (total of 32 bits per word). If there is no data for one of the active inputs (time out) an error code is attached to the output data. The transmission rates and FIFO lengths need additional evaluation.

3.11.1.4 Pixel Readout Units The functionality of the circuitry is similar to the pixel module electronics described above. There are three differences. The input FIFO is 32 bits

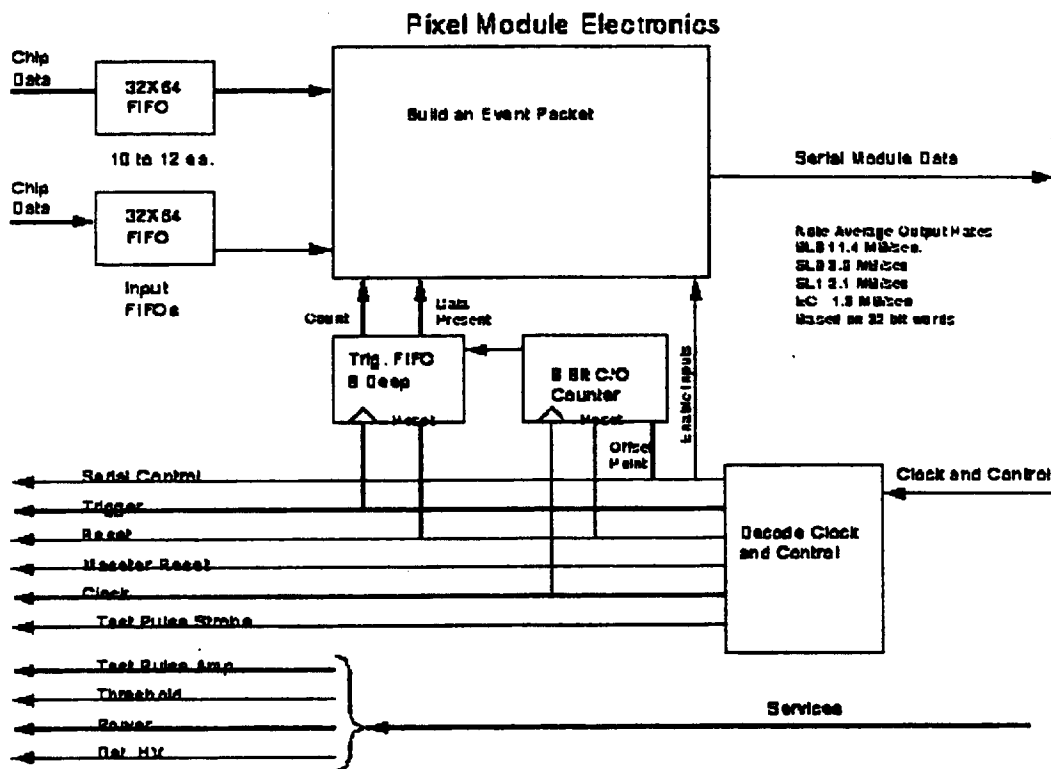


Figure 153: Pixel Module Electronics.

by 256 words deep to allow for the larger event size. Optical drivers have been added to the serial output. The speed of optical transmission and the degree of multiplexing are obviously related in this model. They effect the FIFO depth needed to derandomize the data.

3.11.2 Off-detector Electronics Basic Functionality

The pixel off-detector electronics provides three basic functions. One is to receive the on-detector data, buffer it and present it to the DAQ and Level 2 trigger. The second is to provide control signals such as trigger and register control. And the third is to provide power, biases and slow control monitoring.

3.11.2.1 Interfaces to the Off-Detector Electronics The interfaces to the on detector electronics are detailed in section 3.11.1.1. Interfaces to the rest of ATLAS are listed below:

a. Data to DAQ or Level 2 trigger

These data links are expected to be optical and operate at about 1 giga-bit per second. There are about 200 of these links to carry the required bandwidth. The number depends on the level of multiplexing and the inclusion, or not, of the B physics layer at full luminosity. Each link will provide data from one event at a time. The format is yet to be defined, but it is essential that a unique identifier be attached to an event. If there is no data, a dummy event is sent.

b. ATLAS network

This is a general purpose network that supports the activities in a crate. It has several function that include those listed below:

1. down loading of programs,
2. down loading of control information,
3. monitoring of event data,
4. slow controls functions such as setting of test pulse amplitudes,
5. slow control function such as reading temperature,
6. voltage and currents,
7. and special instruction to the electronics.

c. ATLAS clock and control

This is a high speed optical link the supports such global actions as are listed below:

1. Level 1 trigger,
2. master reset,
3. reset,
4. test pulse strobe,
5. etc.

3.11.2.2 Pixel Receiver and Control Electronics The main function of the receiver card is to collect data from all of the inputs and present data to the DAQ and Level 2 trigger from each card. There could be 32 to 200 of these cards (58 in a model with 8 fibers per card, as in figure 151), since the number depends on the level of multiplexing and the number of fibers. At the highest level of multiplexing, the worst case would be one optical fiber to the DAQ for each input operating near the 1 giga-bit speed. This area needs analysis to find the best optimization of the required fiber speeds. These cards are crate based as shown in figure 151. The crate processor performs the function of general control, slow control, error monitoring and data sampling. Pixel clock and trigger distribution accepts the high speed ATLAS clock and control and interfaces the information to the receiver cards over the local clock and control bus.

The pixel receiver card is informed of an event over the local clock and trigger distribution bus. The control circuitry that is connected to the local clock and control bus informs the receiver circuitry. The data are gathered and transmitted as is the location to use in the linked list (see figure 154). There are 8 to 24 (space limit) data receiver circuits on a board. Each data receiver places the information from its input fiber in a dual ported memory. If no data are present, a dummy data word is saved in the dual ported memory. The functionalities of this operation are listed below:

- detect header(identify event),
- receive and format data,
- place data in dual ported memory and at the end of the data place pointers and header in the linked list.

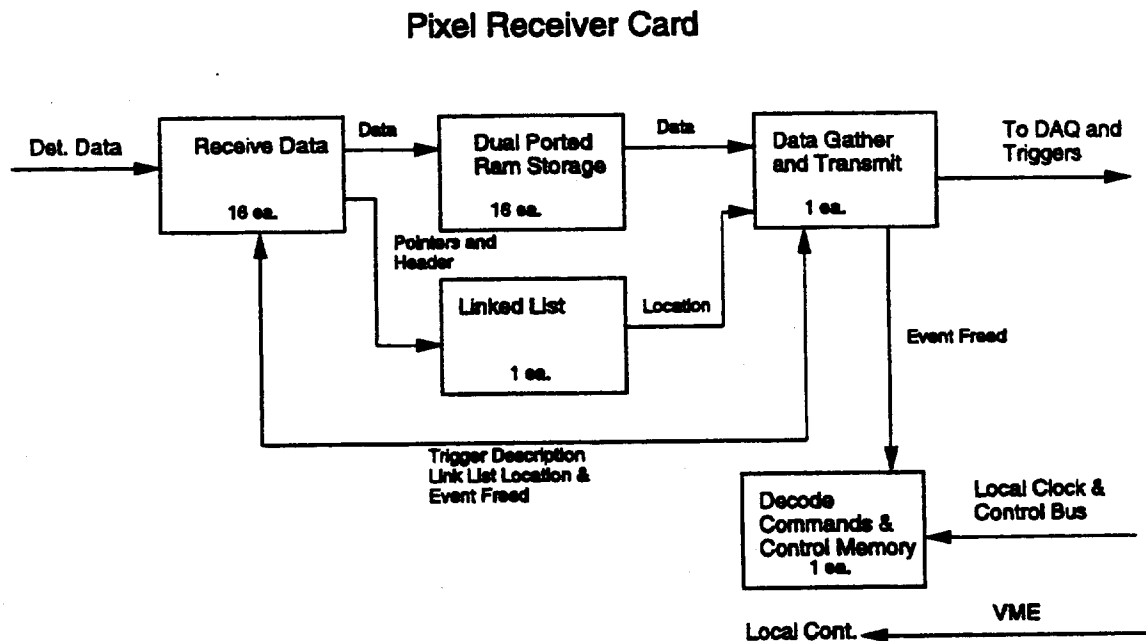


Figure 154: Pixel Receiver Card.

When all receivers have read and stored their data and pointer, the data-gather- and transmitter-circuit will read the linked list and extract the data from the dual ported memories. Four to five address bits are added to the data at this point. Data are pushed to the DAQ and Level 2 trigger over optical fibers. When all data have been transmitted to the DAQ, the control circuitry is informed. It informs the receivers to free the dual ported memory for that event.

The function of the pixel clock and trigger distribution card is to receive the high speed ATLAS clock and control optical information and distribute it over a local bus to the cards in the crate and the on-detector electronics. The high speed data are separated into three types of data. One is the clocks data type. Another is the serial control data type that is used for global commands. The last is crossing specific data type. Crossing specific data are then decoded into commands such as master reset, reset, Level 1 accept, strobe test pulser, etc. Clocks are phase adjusted to the local time frame. This information is distributed over the local crate bus to the card in the crate. The functionality above is generic and expected to evolve.

3.11.2.3 Pixel Service Electronics The pixel service electronics main function is to distribute voltages to the on-detector pixel electronics and to provide monitoring of these electronics. It is assumed that each card will support 16 read out units. The crate count is 2 to 13 crates depending on the level of multiplexing. Each crate has a processor and about 15 pixel service cards. The pixel DC and detector bias supplies feed through the pixel service cards. The processor performs the function of slow controls and monitoring of voltages, currents and temperatures.

The pixel service card can be thought of as a 1 to 16 distribution card. It takes the power and control data and distributes it. It has the circuitry to measure temperature and power voltages and generate analog voltages. The DACs may be located in the on-detector electronics.

3.12 Detector Control for the ID Pixel Layers

3.12.1 Important Quantities

In order to guarantee a proper functioning of the pixel detector a continuous survey of the following parameters/quantities is needed:

- The detector depletion voltages and currents have to be monitored and controlled.
- All supply voltages and currents which are necessary for the readout chips, repeaters and further readout electronics have to be monitored and controlled.
- All voltages and currents which determine the proper operation of the readout chip (preamplifiers, delays, compensation of the depletion currents and thresholds) need to be surveyed. The regulation of these parameters requires a more sensitive equipment. As some of these quantities are correlated a more sophisticated control system is necessary.

- The temperatures on the detectors and the cooling system and the nitrogen flux have to be monitored and controlled.
- Especially at small radii the position monitoring of the detectors is absolutely necessary. Capacitive probes could be an appropriate device.

3.12.2 Requirements to the Detector Control System

We plan to follow the hardware and software recommendations of the general detector control group. We intend to link to standard skeletons at a low level assuming that the standard includes all necessary tools:

- to detect proper functioning of the detectors,
- to detect and diagnose fault conditions,
- to react automatically to errors (e.g. switching off voltages in case of high temperatures or sensing, masking and cataloguing of new noisy pixel cells).

An user friendly graphic discription of the components and their relations is needed. Having this tool people on shift could debug errors and human interaction will be possible.

Special tools for detector experts are used to observe e.g. longtime stabilities or to perform calibration runs for threshold between two fills.

Sensitivity, watchtime periods and reaction times for the control of the different quantities needed to be adaptable to different conditions.

A possibility to write and read test pattern has to be foreseen.

4 A look into interesting developments of the pixel approach: integrated pixels, Ga As pixels, diamonds, etc

4.1 Monolithic Pixel Detector Developments

1. Integrating Pixels and Electronics in Bulk Silicon: USA

In 1989, a group from Stanford and Hawaii Universities proposed the development of a monolithic pixel detector with integrated VLSI readout electronics [70, 71, 72, 73]. The implementation is shown in fig 155.

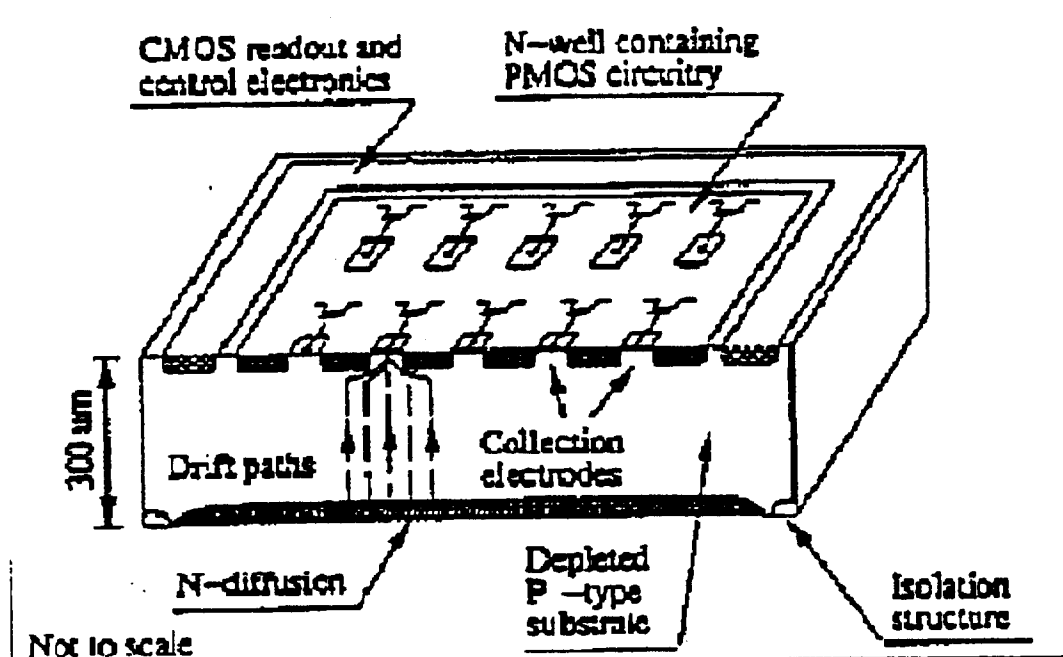


Figure 155: The monolithic pixel detector and electronics geometry developed by the Hawaii-Stanford collaboration. Readout electronics is accommodated in n-wells implanted in the p-type substrate.

Onto a depleted p-type substrate, n material is diffused to make the detector diodes, and n wells are implanted for the PMOS readout electronics, covering 90 % of the area. The detector array contains (30×10) pixels of $(34 \mu\text{m} \times 125 \mu\text{m})$. To minimise loss of charge, signal charges are steered between the readout electronics n wells onto low capacitance ($14 \mu\text{m}$) collection electrodes. Pixel readout is sequential by row and column shift registers operating at 8 MHz. No sparse scan is implemented.

While the fabrication of the monolithic detector is clearly complex, requiring a total of 16 masks -13 front side, 3 back side - it makes use of standard BiCMOS process steps where possible; the exception being the back side patterning, which needs one mask.

Detectors fabricated in this way have shown a signal to noise ratio greater than 80:1. and excellent spatial resolution [71, 72, 73]. In beam tests of a telescope of 4 detectors

in a 600 GeV/c μ beam at FNAL, a spatial resolution of $\sigma = \pm 2 \mu\text{m}$ was seen along the 34 μm pixel axis (using analogue charge sharing between neighbouring pixels). Along the 125 μm pixel axis it was found that tracks crossing the outboard 25 μm bands of the pixels shared charge with their neighbours, allowing a spatial resolution of $\sigma = \pm 5.3 \mu\text{m}$, while in the central 75 μm of the pixels the resolution of $\sigma = \pm 22 \mu\text{m}$ was consistent with $(75 \mu\text{m}/\sqrt{12})$.

2. Bond and Etch-Back SOI Developments in the USA

In this fabrication process [74], being investigated by a collaboration of UC Davis, LBL and SLAC, oxide is grown on two silicon wafers, which may be of different resistivity. These are then bonded to form a SOIOS sandwich containing about 100 nm of oxide. One wafer is then substantially thinned (etched) to leave a thin silicon layer for electronics to be implanted. The other forms the detector substrate. This promising technique offers the possibility of pixel devices with total thickness of about 200 μm , with electronics having the inherent radiation tolerance advantage of thin film SOI. Test structures have been fabricated at U.C. Davis and LBL, and are currently under evaluation.

3. SOI Detector - Electronics Integration in Europe (RD19)

RD19 is collaborating with IMEC, Leuven, Belgium in the development of an adapted SOI processing technology which has been applied to SOI fabricated by SIMOX, ZMR and bonded wafer techniques [75, 76, 77]. In the SIMOX ("Separation by Implantation of Oxygen") process, an insulating buried layer is formed by oxygen ion implantation at 500-700°C, followed by annealing at 1360°C. In ZMR ("Zone Melting and Recrystallisation") technique, a scanned laser beam melts silicon in small zones, which then recrystallises on top of the oxide layer. It is expected that these SOI approaches will offer more freedom in detector geometry than the n-well electronics approach, and that full CMOS circuits with good radiation hardness can be built in the thin silicon layer directly above the detector.

Since SIMOX and ZMR both have high temperature process steps, with the possibility of contamination and introduction of structural defects, the two goals were to evaluate detectors in the bulk silicon, and transistors and test structures in the SOI layer. In two processing runs, repeatable detector leakage currents in the range 5 - 20 nA cm⁻² were seen from the SIMOX and ZMR processes (on 1500 Ω cm (100) Si). MOSFETs in the SOI layer had similar noise levels to MOSFETs formed in typical bulk analogue processes. This work represented the first integration of SOI electronics with pin diodes on high resistivity silicon.

4. Other European Monolithic Detector Developments

Monolithic pixel detector prototypes have been fabricated at IMEC, Leuven in a p-well CMOS process. In this process, p-wells to contain pixel readout electronics are implanted in n-type high resistivity silicon [78, 79]. For efficient charge transfer in the p-well architecture, the electric field within the high resistivity detector substrate must be carefully screened from the potentials on components contained in the p-wells. A number of different readout building blocks, including amplifiers, comparators and

shift registers have been successfully demonstrated in the technology, and a possible architecture for 2D sparse analogue readout of pixel charge has been developed [78].

Other investigations of the design and performance of pixel detectors with integrated amplification and storage have been made at MPI, Munich [80] and are described in more detail in the following section.

4.2 DEPFET Pixel Detectors

Development of pixel detectors based on another function principle is pursued at MPI-Munich. This development is still in a generic stage but promises significant advantages over the "conventional" baseline approach of two dimensional diode arrays connected by flip chip bonding to the readout electronics, each pixel requiring its own amplifier discriminator and readout logic.

Instead the basic pixel element itself already has simultaneously detector and amplification properties. Its power consumption is very small due to the extremely small capacitance of the collecting "electrode". Since the signal is already amplified in the individual pixel it can be split and read out simultaneously in different ways. Combining e.g. the outputs of pixels in a row, the pixel detector can be read out like a strip detector. If the split up amplified signals are connected along several lines of (e.g. three) different directions the device acts like several strip detectors being physically positioned on the place. Therefore ambiguities in space point assignement - which are present in double sided strip detectors - can be resolved locally without necessity of prior track reconstruction.

The detector concept is based on the DEPFET (Depleted Field Effect Transistor) principle shown in fig. 156. Several not yet published features have been added to this concept so as to make it applicable to the high rate environment at LHC. They include a automatic threshold voltage compensation for the DEPFET and a clearing structure for signal and thermally generated charge which allows continually sensitive operation of the device.

In the following a short description of the basic DEPFET detector-amplifier structure and the modifications of a pixel cell for LHC applications (fig. 157) will be given.

4.2.1 The DEPFET principle

The basic DEPFET structure consists of a field effect transistor built on a substrate which is completely depleted from a large rectifying junction on the backside of the substrate. A potential minimum for electrons forms below the transistor channel, respectively the (external) gate of the transistor. This potential minimum is called internal gate, since electrons produced in the bulk by e.g. ionizing radiation will be collected there. They will change the conductivity of the channel by influence thus increasing the transistor current.

Signal charge therefore can be determined by comparing the transistor current with the current obtained with emptied internal gate. The internal gate can be emptied in several ways. In the structure shown in the figure it is accomplished by putting a short positive pulse on the clear contact, thus changing the potential distribution inside the bulk in such a way that the potential minimum below the channel disappears and the signal charge flows towards the clear contact.

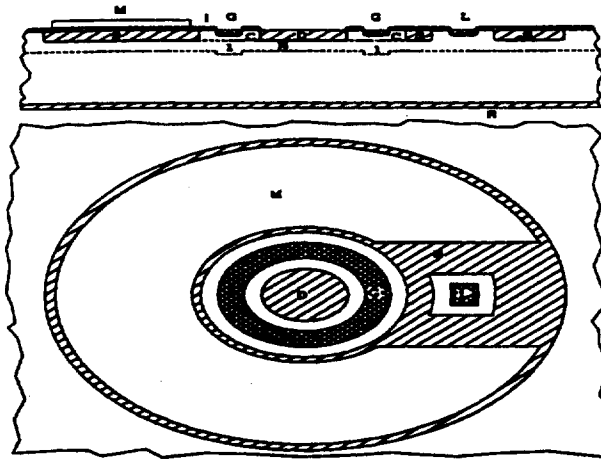


Figure 156: Basic DEPFET structure

An interesting feature of the device is the fact that the charge is not destroyed by the readout. It can therefore be measured several times. One can make use of this fact in a pixel device composed of many of DEPFETs put side on side and allowing selected readout of single pixels or group of pixels by proper biasing of source, drain and gate of these transistors. A coarse scan of the device determining the region of interest may be followed by a single pixel readout of interesting regions.

4.2.2 LHC DEPFET pixel cell

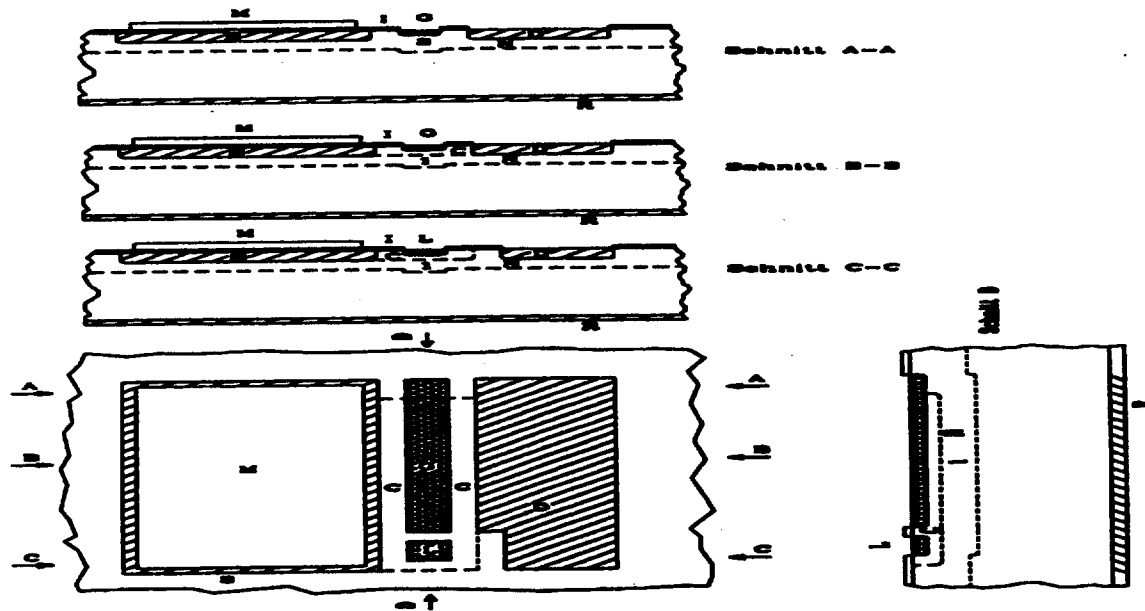


Figure 157: Basic cell of a linear DEPFET structure with built in transistor threshold compensation and continuous clearing

The pixel detector suggested in the previous section is not adequate for LHC operation for several reasons:

- the pixel device has to be continuously sensitive.
- due to the high bunch crossing rate and long trigger delay clearing after each crossing is not possible.
- all transistors have to be on permanently.
- individual transistors will vary in their threshold voltage. As source, gate and drain voltages are common to all transistors of the device, turning on all transistors simultaneously will cause many of them to draw very large power.
- signal and leakage currents have to be drained away from the internal gate in a continuous fashion.

A structure having the required properties is shown in fig. 157. As before the JFET transistor is located on top of the fully depleted bulk and the signal electrons are collected in the internal gate, steering the transistor current. Readout of the amplified signal can be done through the source and/or the drain of the transistor.

Threshold compensation is achieved by connecting the source through a capacitor to a fixed voltage (which may be the input voltage of a charge sensitive amplifier). The capacitor is naturally integrated into the device using the oxide as dielectricum. This capacitor will charge up until the drain current drops to zero. If at a certain time a individual pixel collects some signal charge the corresponding transistor will collect the charge in its internal gate and the transistor will become conducting again until the capacitor has charged up to the new equilibrium voltage again. Charge is amplified by the ratio of source coupling and gate capacitance.

Clearing of the gate is performed by a n-p-n⁺ structure which is naturally formed from the n-doping of the internal gate, the p-doping of the transistor channel and the n⁺ doping of the clear contact (also used for the top gate of the transistor). The internal gate will adjust its voltage automatically in such a way that the pixel leakage current flows across this structure towards the clear contact (held at constant potential).

Further improvement and simplification of the device properties is achieved by connecting the (partially filled) internal gate with the external gate.

Dividing of the amplified signal into several readout directions can be achieved by splitting the source capacitor into several smaller capacitors.

4.2.3 Status of project

A 32x32 DEPFET pixel matrix is currently under test. The matrix bases still on the older devices shown in figure 1. A spectroscopic energy resolution of 30 electrons was measured at room temperature with a rather conservative designed DEPFET (9 micron channel length). New test devices operating with individual threshold compensation and continuous clear mechanisms were also fabricated. The first statically measured parameters are all in the expected range.

4.2.4 Further efforts

The required operation speed for ATLAS of 20ns time resolution makes it necessary to incorporate a current source into the pixels. Also a second metallization layer has to be implemented in order to provide delay free cross points for multi directional readout lines. For irradiation tests the already produced prototypes are intended to be used.

4.3 The GaAs pixel detectors

4.3.1 Introduction

Pixel detectors offer significant advantages over silicon microstrip detectors for applications in high radiation zones at the LHC. The detector signal/noise ratio is typically much higher because of the smaller element capacity and the effects of radiation damage are less catastrophic. The greater radiation hardness of GaAs offers even more potential for withstanding the neutron and charged particle fluences of $> 10^{14}/cm^2$ expected at the small radii of vertexing layers in ATLAS or CMS. In the following, a description is given of the first experimental results obtained with a GaAs pixel array in a CERN test beam.

4.3.2 Detector fabrication

GaAs pixel detectors are presently fabricated by evaporating metal contacts on polished and deoxidized surfaces. They are therefore surface barrier (Schottky) diodes.

Wafers are mechanically thinned to about 200 μm , and then polished with a chemo-mechanical process. This is based on bromine-methanol, or sodium hypochlorite, or hydrogen peroxide, the latter giving the best detector performance.

A photolithographic process is then used, including 4 mask stages:

- Schottky contact evaporation,
- passivation etching,
- wettable metal evaporation,
- back contact evaporation.

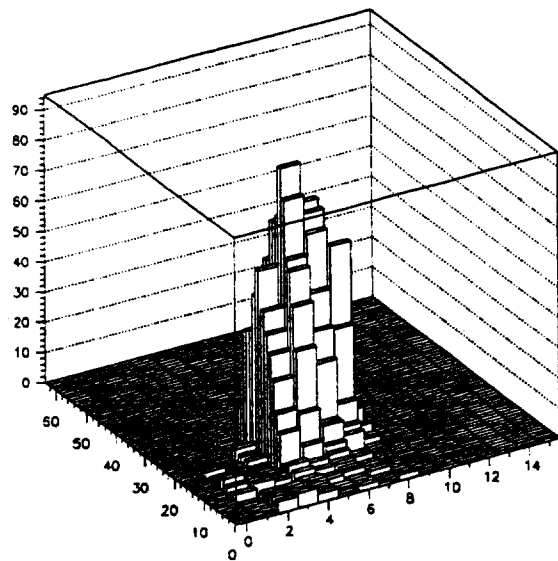
Ti-Pd-Au is presently used as the rectifying contact. This gives a good adhesion to the substrate and is thermally stable.

As passivation a 100 nm thick layer of silicon nitride is deposited. Windows are then dry etched to allow evaporation of a gold layer which acts as the wettable metal for indium bump bonding.

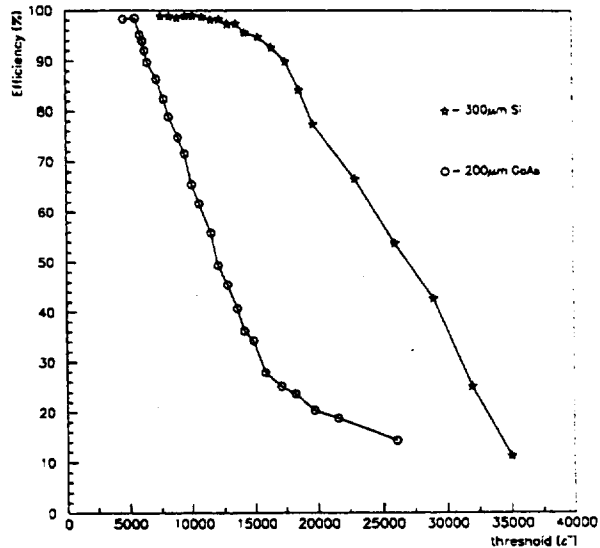
The back contact is optimized to be non-injecting, and uses Ge-Pd-Au layers with low temperature annealing. An infra-red camera is used to align the back contact mask to the front one.

The resulting yield is comparable with that of Si devices. In-house tests show a visually defect-free array yield of about 95%.

The pixel detector is then bump-bonded to the previously-bumped, $\Omega 2$ read-out chip [29] at the Caswell laboratories of GECMMT.



(a) Beam profile



(b) Discr. threshold scan

Figure 158: Results of tests of first pixel detector in GaAs

4.3.3 Test Beam results

A telescope comprising two silicon pixel detectors and one GaAs pixel detector was set up in the H6 test beam at CERN [81, 82]. Suitable small scintillation counters provided a trigger for the DAQ system which utilised a MacIntosh computer to control three $\Omega - Ion$ CAMAC modules. The beam profile obtained from coincident hits in the three pixel detectors is shown in Figure 158 together with the results of a scan of the discriminator threshold voltage in the digital read-out chip. The detection efficiency for the GaAs pixel layer was determined as a function of the reverse bias on the detector as the ratio of the number of coincident hits in all three detectors to the number of coincident hits in the two silicon layers. The result is shown in Figure 159. The figures demonstrate the ability of GaAs pixel detectors to provide good detection efficiency for charged particles in layers of $200\mu m$ at voltages above 100 V. The radiation hardness of GaAs detectors has already been established at neutron fluences in excess of $10^{14} n/cm^2$, in the case of simple Schottky diodes on industry standard, semi-insulating substrate wafers, and above $10^{15} n/cm^2$, as shown in Figure 160 in the case of $\pi - \nu$ junction devices formed by in-diffusion of deep level donors like Fe or Cr into standard substrates [83, 84].

4.3.4 Conclusions

Further work remains to be done to optimise the performance of both the GaAs pixel detectors themselves and the read-out electronics for operation at the high rates of the LHC. Understanding of the charge transport mechanisms and radiation damage effects in the ma-

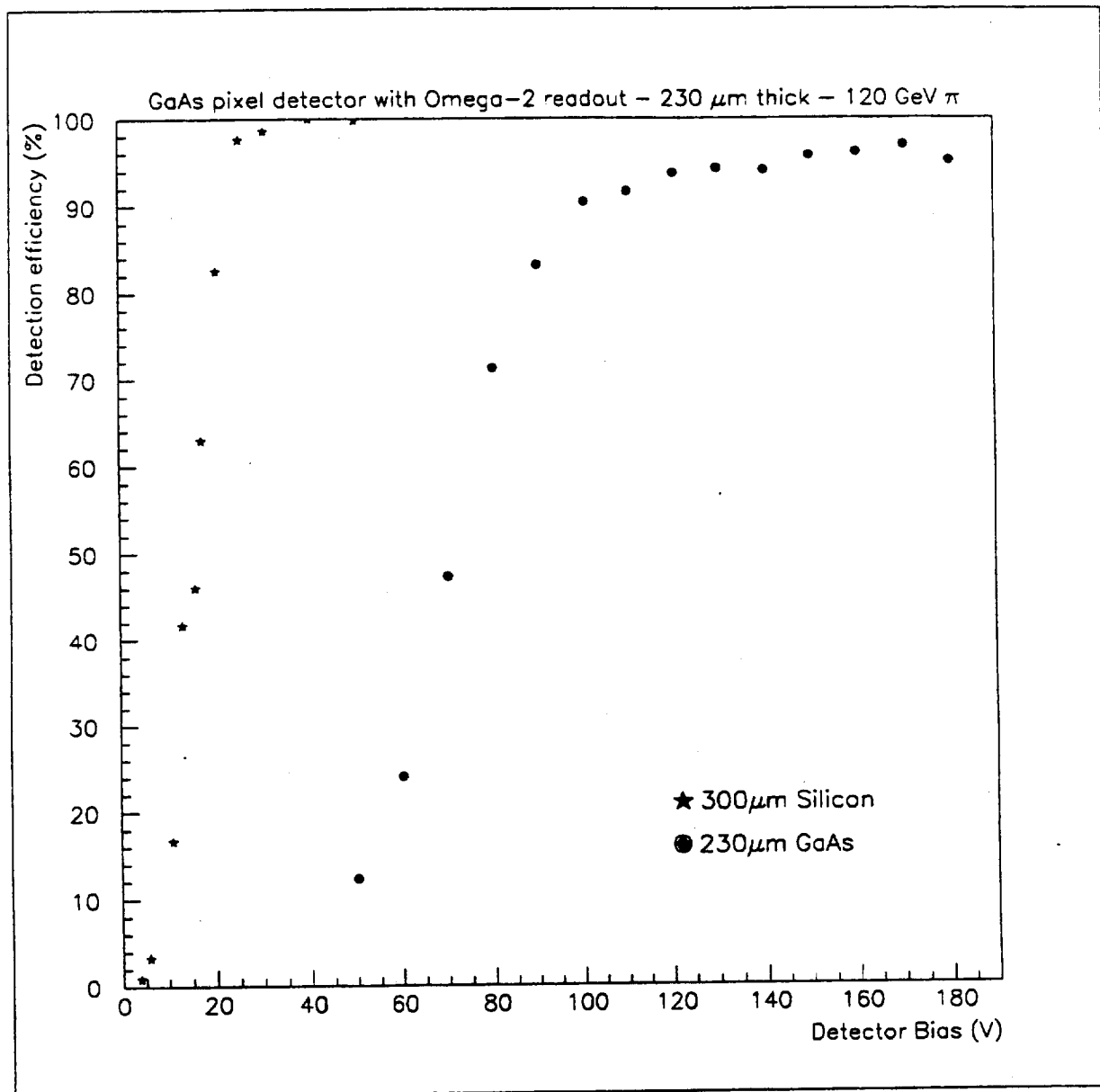


Figure 159: Efficiency of GaAs pixel layer as a function of reverse bias

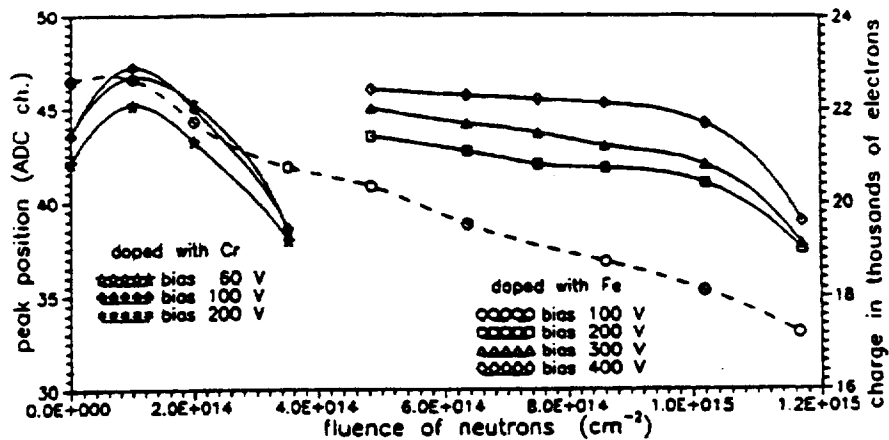


Figure 160: Variation of collected signal charge with neutron dose for Tomsk detectors

material are also the subject of continuing efforts. Nevertheless, GaAs pixel detectors have already established their potential as contenders for inclusion in LHC applications in the most demanding radiation environments.

4.4 Polycrystalline Diamond as a Substrate for Pixel Detectors

4.4.1 Generalities on diamond as a detector

Natural diamond has had a long history of use for particle detection - predating the use of silicon - principally in instrumentation for nuclear test diagnostics. In recent years, the practical use of diamond as a detector material in high energy physics has been made possible [85] by recent advances in Chemical Vapour Deposition (CVD) processing, which allows diamond to be produced economically in large quantities, with high purity, relative to that of natural type IIa diamond.

Table 24 compares the properties of diamond relevant to detector applications with those of silicon. The very high band gap of 5.5 eV makes diamond a very good insulator, with resistivity ultimately determined by the concentration of impurities and defects. The large resistivity allows a high electric field to be applied across a diamond layer without producing a significant leakage current. There is no need, as in the case of silicon detectors, for the reverse biasing of implanted pn junctions. The material is correspondingly immune to doping changes and type inversion under irradiation, and detector fabrication is particularly simple, with very few masking and patterning operations. Fig 161 indicates the functional simplicity of a diamond detector.

The large band gap of diamond does, however, also result in signal sizes only about half those in silicon, and the major challenge in diamond detector research and development is the maximisation of the signal within the inevitable constraint imposed by the band gap.

Although an electrical insulator, diamond has very high thermal conductivity (exceeding that of copper by a factor of about 5), giving it an advantage over all the ceramic substrate

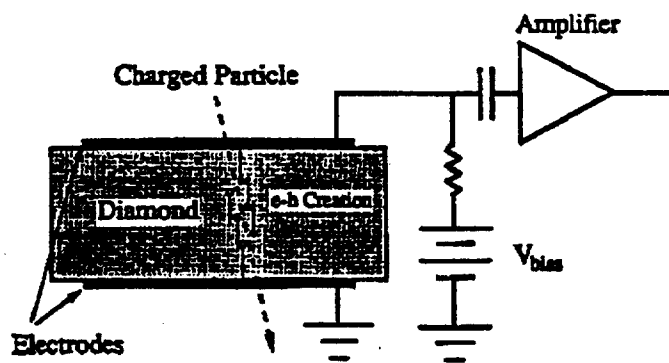


Figure 161: Schematic of diamond detector operation.

materials in thermal management.

Table 24: Properties of diamond relating to its use as a detector material.

| Property | Diamond | Silicon |
|---|---------------------|---------------------|
| Band Gap (eV) | 5.5 | 1.12 |
| Breakdown field (V/cm) | 10^7 | $3 \cdot 10^5$ |
| Resistivity (Ω cm) | $\geq 10^{11}$ | $2.3 \cdot 10^5$ |
| Intrinsic Carrier Density (cm^{-3}) | $\leq 10^3$ | $1.5 \cdot 10^{10}$ |
| Electron Mobility ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$) | 1800 | 1350 |
| Hole Mobility ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$) | 1200 | 480 |
| Saturation Velocity ($\mu\text{m}/\text{ns}$) | 220 | 82 |
| Dielectric Constant | 5.7 | 11.9 |
| Thermal Expansion Coefficient (K^{-1}) | $0.8 \cdot 10^{-6}$ | $2.6 \cdot 10^{-6}$ |
| Thermal Conductivity ($\text{Wm}^{-1}\text{K}^{-1}$) | 1000-2000 | 150 |
| Energy to create e - h pair (eV) | 13 | 3.3 |
| Density (g cm^{-3}) | 3.5 | 2.33 |
| Mean no. e - h pairs created per 100 μm | 3600 | 9200 |
| Mean no. e - h pairs created per 0.1 % X/X0 | 4500 | 8900 |

4.4.2 Chemical Vapour Deposited Diamond

In contrast to more traditional high-temperature, high-pressure diamond synthesis, which can produce crystals typically 1 mm in size, CVD diamond wafers as large as 18 cm in diameter can be processed. The rapid development of CVD diamond processing has driven the cost per carat (200 mg, or about 4.6 cm^2 for $300 \mu\text{m}$ thickness) down by a factor of 20 in the period 1989-94. In CVD diamond production, a small additive of hydrocarbon gas - such as methane - is mixed with molecular hydrogen, and the mixture heated, either by microwaves, a hot filament or some other energy source. The resulting reactive gas mixture is brought into contact with an elevated temperature substrate, typically silicon, where the carbon-based radicals are reduced to link together with single bonds to form a diamond lattice. Crucially important is the (high) concentration of hydrogen in the primary gas

mixture, which helps prevent graphite formation. The diamond films made in this process typically grow in a polycrystalline columnar structure, starting from small ($1 \mu\text{m}$). the maximisation of the signal within the inevitable constrainrandomly-oriented grains on the substrate side, which grow into alignment with the fastest growing (110) crystal orientation. It has recently been shown [86] that the electrical properties of CVD diamond vary with depth. Carrier lifetime and mobility are lower on the substrate side than on the growth side. The removal of material from the substrate side of CVD diamond films has been found to improve the electrical performance on which detector operation depends by 40 % from that of the as-grown film.

The figure of merit for polycrystalline diamond film for detector applications is the average charge carrier collection distance, d_c (μm), that an electron - hole pair created by the passage of an ionising particle separate under the influence of an applied electric field E .

$$d_c = (\mu_h \tau_h + \mu_e \tau_e) \cdot E \quad (7)$$

where μ_h (μ_e) and τ_h (τ_e) are the hole (electron) mobilities and lifetimes respectively. Since observed charge, q_{obs} , in a non-dioidic detector is related to the specific generated charge, per μm , Q_{gen} , according to:

$$q_{obs} = d_c Q_{gen} \quad (8)$$

it is important to maximise the carrier mobilities and lifetimes for a given electric field. As the result of close cooperation with CVD diamond manufacturers, collection distance in CVD diamond for detector applications has steadily improved in recent years, and is now routinely better than that of natural type IIa diamond (fig 162).

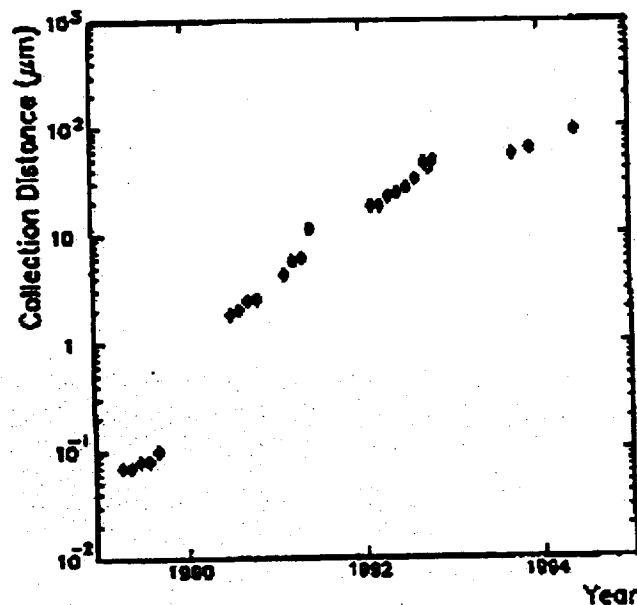


Figure 162: The recent history of collection distance in CVD diamond (electric field $100\text{V}/100\mu\text{m}$).

4.4.3 Recent tests of diamond detectors

Over the past two years, studies have been made of the performance of CVD diamond in tracking and calorimetry applications. Small diamond strip detectors have been fabricated and studied with the aid of a beam telescope in a 50 GeV p beam at CERN [87] and a small tungsten-diamond calorimeter containing 20 (3 cm \otimes 3 cm \otimes 500 μ m) sampling layers was tested in a beam at KEK [88].

Strip detectors were constructed on (8 mm \otimes 8 mm \otimes 300 μ m) diamond with 64 strips at 100 μ m pitch and 50 μ m width. A guard ring was present. A metallic Au (300 nm) on Cr (50 nm) contact was made to each side of the detector, and the strip pattern created with a wet etch process. Generally, the first metal in contact with the diamond determines the electrical properties of the contact. Chromium, Titanium and other transition metals that form carbides tend to produce ohmic contacts to diamond. An I-V curve for six ganged strips fig 163 indicates very low levels of leakage current. Figure 164 shows the collection distance for the same sample. Between 100-125 V, its slope changes, as does that of the I-V curve, indicating a saturation of the carrier mobility, an increase in the number of carriers, and a change in the resistivity of the material. Such effects are common in diamond.

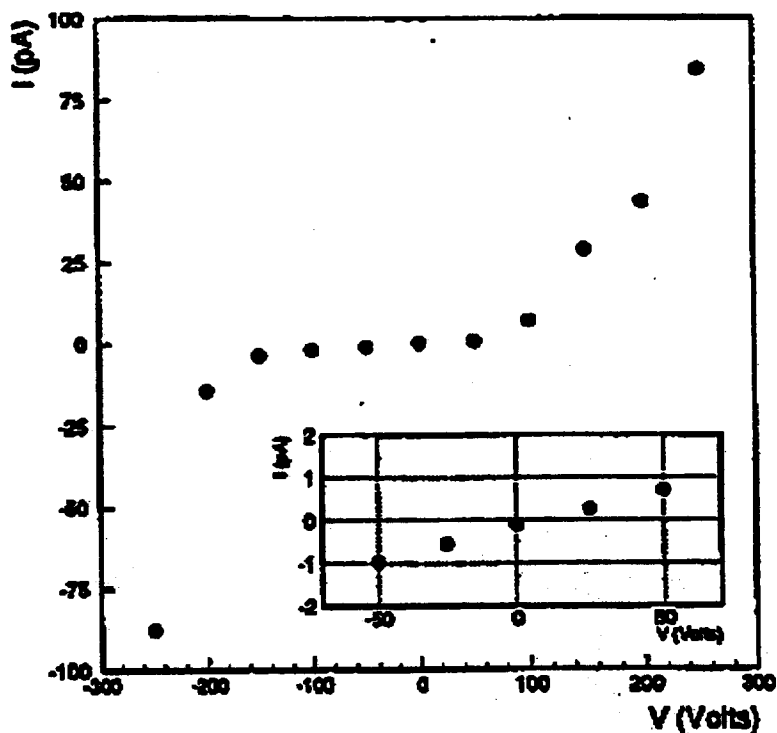


Figure 163: I-V Characteristics of six ganged strips from a diamond strip detector.

The position resolution measurement of the diamond detectors was measured with a telescope of 8 silicon strip reference detectors (4X, 4Y), each with an intrinsic resolution of 6.5 μ m, with analog data acquired by a system of VME Scirocco processors [89] In these tests, the strips on the diamond detectors were DC coupled to individual Viking preamplifier channels [90] (also read out by SCIROCCOs) and the detector bias voltage applied to the common rear electrode and filtered locally.

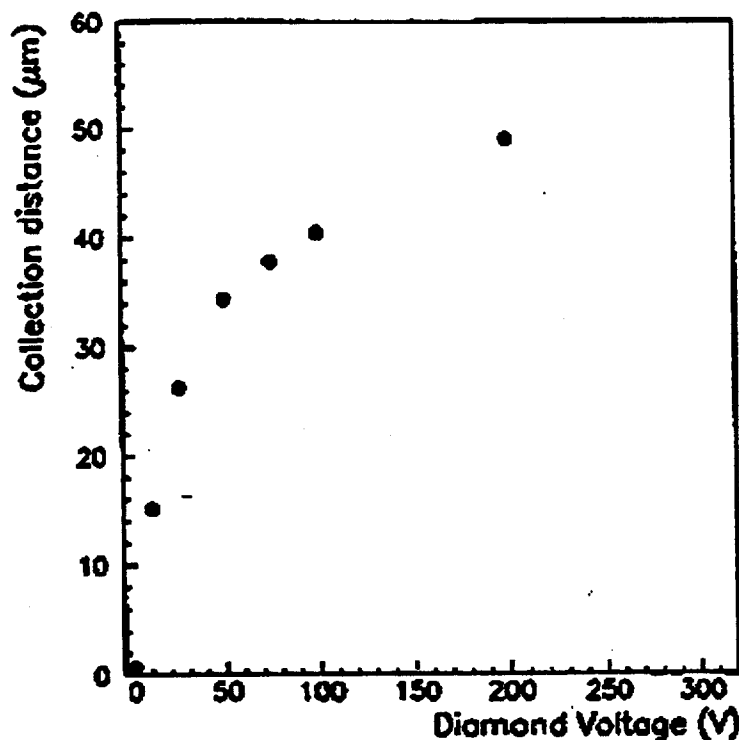


Figure 164: Charge collection distance as a function of bias voltage for a diamond strip detector

Data were taken in normal incidence only. Charge clusters in the diamond detectors lying close to reconstructed tracks contained two strips on average. At a detector bias of 195 V, a fit the measured signal to noise ratio of about 6.3 gave a most probable (Landau) charge for a minimum ionising particle of 875 ± 105 electron-hole pairs (Fig 165). Noise from the detectors was small in comparison with the electronics: leakage current was ≤ 1 nA for all strips combined, while individual strip resistances were lower than the equivalent channel resistance of the preamplifier input FET. A lower limit for the detector efficiency (not taking into account dead readout channels) was 86 % at $V_{bias} = 195$ V. The detector resolution (at $V_{bias} = 195$ V) was calculated taking into account the analog pulse heights from the strips. With the signal to noise of about 6:1, this was (25.4 ± 0.9) μm ; an improvement of about 12 % with respect to $100 \mu\text{m}/\sqrt{12}$.

A major goal for the short term in the RD42 program is significantly improved signal, through cooperation with CVD diamond producers, in CVD diamond having better collection distance. Several of the collaborating institutes have collection distance measurement apparatus, which can provide rapid feedback to manufacturers for the optimisation of processing parameters. The trend of rapid improvement in collection distance is expected to continue: it is hoped that CVD diamond samples with a collection distance of at least 125 μm [91] will be available for beam testing in early 1995, with further enhancement later in the year.

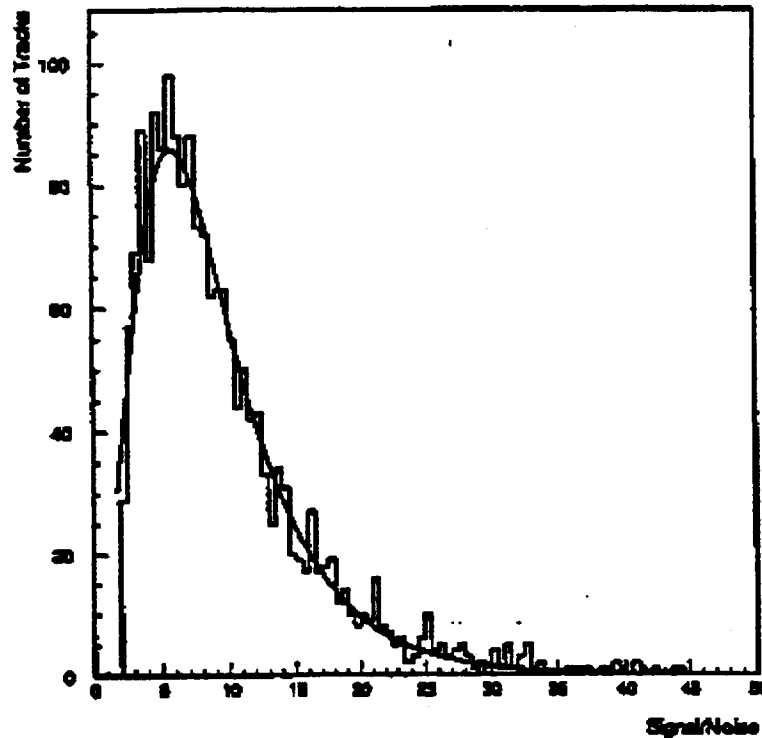


Figure 165: Signal to noise distribution for hits well matched to charged particle tracks as predicted by the silicon telescope. The most probable signal is 6.3 ± 0.2 times the average single strip noise.

4.4.4 Radiation Hardness Studies of Diamond

High energy particles displace atoms in the diamond lattice to produce vacancies and interstitials. Radiation damage in diamond from electrons has been extensively studied [96]. It is known that 2 MeV electron irradiation produces about 0.3 vacancies $\text{electron}^{-1} \text{cm}^{-1}$, recognisable from their optical spectra [93]. Early data [94] suggest that neutrons produce about 500 times more vacancies than do electrons. While it appears that these primary defects have very little effect on the electronic properties of the detector - and far less so than the same damage levels in silicon - further irradiations (at Sandia and Los Alamos National Laboratories) are planned by the RD42 collaboration, which will also make comparisons with natural type IIa and silicon at every dose level.

These studies will be part of a program to measure radiation damage conditions relevant to the LHC operating environment, in terms of the particle species and energies, and under a variety of detector operating conditions. This program will also include irradiations with pions (at PSI) and protons of at TRIUMF and Heidelberg.

4.4.5 Conclusion

Although the signal size from the present generation of diamond detectors is too small for use in large area microstrip detectors, cooperation with manufacturers to improve process parameters has led to a rapid improvement in the most critical electrical parameter - the

charge collection distance. If this trend continues and diamond is shown to be hard under irradiation to the levels expected during years of operation at LHC, diamond could become a very interesting material for the fabrication of pixel detectors for the innermost region of an inner tracking and vertex detector. Even with signals a factor of 2-3 smaller than silicon, diamond pixel substrates would be well suited to use with the extremely low noise (100-200 e^- rms) fast rise time radiation hard electronics already under development for pixel detectors.

5 Role of the Barrel Sector Prototype project

5.1 Introduction

The "Barrel Sector Prototype" (BSP) of the ATLAS inner detector will afford the opportunity to study the overall system performance of a small region of the inner detector - containing pixels, gallium arsenide, silicon microstrips and a straw tube tracker/TRD - in a magnetic field, with high multiplicity events produced from the interaction of a high energy beam with a variety of targets.

These tests will be a vital step in the evaluation of the various detectors and readout schemes under development for ATLAS, and in understanding their mechanical and electronic integration into the overall inner detector. The BSP will be a vehicle for the simultaneous operation of readout electronics for a number of different detector types, transferring data through optical links under ATLAS readout protocols to DAQ having full ATLAS functionality. Front end data reduction, storage to accommodate simulated level 1 trigger latency, and time stamping to 25 ns resolution will be tested in the BSP.

The understanding of global alignment requirements and the implementation of techniques for alignment monitoring will also be major developments from the BSP effort.

The BSP is planned for construction in 1996, and for beam testing in 1997. It is planned to be installed in the H8 beam at the CERN North area. The particle species, energies and intensities that can be delivered by this beam, for 10^{12} incident protons at 450 GeV/c, are shown in table 25. (ref: [97])

Table 25: H8 beam types, energies and intensities from 10^{12} incident protons at 450 GeV/c

| Particle Species | Energy | Intensity (per pulse) |
|------------------|-----------|-----------------------|
| p | 450 GeV/c | 10^6 |
| π^+ | 200 GeV/c | $2 \cdot 10^7$ |
| π^- | 200 GeV/c | $7 \cdot 10^7$ |
| ^{32}S | 200 GeV/A | 10^6 |

A large dipole magnet [98], already located in the H8 beam, can provide a field of 1.8 Tesla ($\pm 5\%$) and has a vertical aperture of 1.6 m and overall length 3.5 m. Although not presently equipped with the necessary cryogenics, this magnet could be brought back into operation to for BSP testing. Although the dipolar field will not completely simulate the detector plane/solenoidal field configuration of the ATLAS inner detector, a good approximation to the configuration is possible with the cylindrical tracker elements aligned parallel to the dipole field (ie: mounted vertically).

5.2 Pixel detector geometry and mechanical support in the Barrel Sector Prototype

The pixel detector ensemble implemented in the BSP will contain axial ladders and disk segments implemented with pixel detector tiles in the geometries planned for LHC. These ($6.28 \otimes 2.16$ cm) for the cylindrical layers and ($9.8 \otimes 0.7-1.3$ cm) for the disks. Axial ladders will be positioned in a prototype support structure to have the same azimuthal overlaps

planned for the real detector (see 1.2 and 1.3), to allow the projective viewing of tracks passing through the overlap and non-overlap regions of the inner layer, and aid in efficiency measurements.

The mechanical structure for the BSP pixels is expected to contain support and cooling channels for two ladders at the nominal radii of 4 and 11.5 cm (subtending about 45° and 15° in azimuth respectively), three ladders at the nominal radius of 16.5 cm (subtending about 17° in azimuth) and disk segments at their nominal z positions (see 1.2 and 1.4). Each disk segment will similarly investigate overlap, and could contain a 4 wedge shaped tiles (giving azimuthal coverage of about 14°) There is insufficient magnetic aperture to accept the full z - length pixel ensemble (the same is true for example for the TRT straw tubes), and the overall dimension of the BSP parallel to the magnetic field is as yet undecided.

With the modular tile placement scheme under study for the cylindrical pixel layers, it is probable that ladders in the BSP will not be instrumented over their full lengths, but will carry tiles in projective z positions that will convey the most useful information. Tiles of different levels of development could be tried in different positions and easily exchanged.

The pixel support structure incorporated into the BSP will accurately represent - in almost all respects - a prototype of the final structure, excepting the substitution of aluminium for beryllium for the shell material (with dimensional adjustments to assure the same rigidity as the final beryllium structure) to reduce the cost. Mechanical integration of the cylindrical and disk pixel surfaces with the rest of the inner detector support will be thoroughly investigated in the BSP.

Since the bi-phase evaporative cooling offers lower mass than cooling using all liquid or water-ice binary mixtures, we will continue to investigate this scheme as part of our pre- BSP RD program. It is to be hoped however that a single cooling technology will eventually prove suitable for the whole of the ATLAS inner detector, even though the operating temperatures may differ from one part to another.

The BSP will be an important vehicle for the understanding of the absolute and relative alignment required between detectors in the same layer and in successive layers. Possible techniques that may be employed include TV holography, X-ray diagnostic devices and frequency scan interferometry (Ref: [41]).

5.3 Pixel beam testing prior to BSP operation.

Early in 1995, it is planned to test two readout chips implemented at CPPM in the DMILL radiation hard technology (see 3.6): a simple readout chip from the DMILL "FERMION" reticle, and a $16 \otimes 8$ array with full LHC functionality from the "HADRON" reticle will be tested bonded to small pixel arrays. Later in the year, implementations of the same circuits in the Thomson HS013-HD will be tested, together with the LBL4 ($12 \otimes 64$) columnar readout chip. These tests will be made using a silicon beam telescope built at CPPM, which will have a stand alone DAQ and will be installed upstream of the dipole magnet intended for the BSP. The telescope will be integrated into the RD13 DAQ in the same way as the other prototype detector test systems (SCT, TRT, etc). This will allow data correlation for tracking and triggering, and will be a valuable preparation for the integrated DAQ of the BSP. It is planned to test the readout capability for particles separated by 50-200 ns (a few BCOs), a critical requirement for the pixel readout architecture, and will require high

intensities of about 10^7 per spill. Measurements of resolution as a function of incident angle in the direction of the short (ϕ) and long (z) pixel axes are planned.

5.4 General Pixel Milestones relevant to the ATLAS Barrel Sector Prototype

Year 1

- (1) Preparation of BSP project proposal; definition and scope (following choice of final ID geometry by ATLAS ID community).
- (2) Continue to evaluate radiation hard electronics technologies and pixel detectors with aim to establish acceptable survivability lifetimes for each layer radius.
- (3) Production of readout circuit elements in radiation hard technologies, thinned detectors and detector structures to study substrates that are non fully depleted.
- (4) Proof of operation of pixel detector "tiles" carrying several readout chips in test beams.
- (5) Evaluation of bi-phase cooling technology, as possible low mass cooling option.
- (6) Evaluation of mechanical stability of water/ binary ice (higher mass) cooled support structure, and of (lower mass) bi-phase fluid-cooled support structure.
- (7) Development of prototype DEPFET technology pixel detectors.
- (8) Evaluation of different readout circuit architectures by simulation, source and beam tests of prototypes bonded to pixel detectors.
- (9) Studies of readout strategies applicable to DEPFET pixel detectors.
- (10) Evaluation of bump bonding technologies from several manufacturers to understand yield, cost in large volume applications etc.

Year 2

- (1) Design of pixel support structure, based on demonstrated feasibility of preferred cooling technique(s).
- (2) Definition of alignment procedures to be used in the BSP.
- (3) Selection of one or two promising readout architectures, and first pixel tiles with functional (sparse scan/ time stamped) readout, following standard ATLAS DAQ protocols, data rates etc, though not necessarily in a radiation-hard technology.
- (4) Appearance of first prototype readout chips in radiation tolerant technology.
- (5) Continuing development of DEPFET technology pixel detectors, together with exploitative readout circuit architectures.
- (6) Proof of the ability of the detector wafer to cope with raised depletion voltage after irradiation to levels expected at LHC.

Year 3

- (1) Construction of Pixel sector structure and cooling system, and hook-up to cooling fluid recirculator.
- (2) Ladders equipped with readout (item 3 in year 2).
- (3) First testbeam evaluation of whole BSP pixel system (instrumented cylinder and disk pixel layers).
- (4) Evaluation of data for alignment, resolution, pattern recognition.
- (5) First radiation tolerant tiles with full readout capability.

6 Conclusions

In this document we tried to describe in detail all the work currently going on for the pixel project in Atlas. It is clear that still a strong R&D effort must be pursued in the near future in order to study all the details of the project. This effort, which must be well coordinated to avoid duplication, is fully justified by the potential, in term of physics measurements, that the pixel detectors will bring to ATLAS.

References

- [1] Letter of Intent of ATLAS: CERN/LHCC/92-4 LHCC/I2 (1992)
- [2] Letter of Intent of CMS: CERN/LHCC/92-4 LHCC/I1 (1992)
- [3] "A Radiation Hard Detector for Tracking and Secondary Vertex Finding for the EAGLE Detector at the CERN LHC": C. Arrighi et al: ATLAS INDET-NO-009 (April 1992)
- [4] "Radiation Doses Expected in LHC inner detectors: an update": T. Mouthuy: ATLAS INDET-NO-028 (Oct 6, 1993)
- [5] SCT Group: ATLAS Internal Note INDET-NO-085 (1995)
- [6] J. Jernigan et al, "Preliminary Test Results from a Telescope of Hughes Pixel Arrays at FNAL" SLAC Pub 5925 (1992)
J. F. Arens et al, "Progress Report of the Collaboration for the Development of Pixel Vertex Detector Technology" SSC Pixel Detector Development Collaboration (Oct 1, 1992)
- [7] C. Kenney et al "A Prototype Monolithic Pixel Detector" Proc. 1st Intl. Symposium on Development and Application of Semiconducteur Tracking Detectors, Hiroshima (May 1993); Nucl. Instr. & Meth A 342 (1994) 59
- [8] D. Bintinger et al: "Pixel Detector Description for Simulation for the ATLAS Technical Proposal" ATLAS INDET-NO-XXXX (November 30, 1994)
- [9] Letter of Intent of COBEX: CERN/LHCC/93-50 LHCC/I6 (1993)
- [10] Letter of Intent of GAJET , CERN/LHCC/93-54 LHCC/I7 (1993)
- [11] Letter of Inten tof LHB, CERN/LHCC/93-45 LHCC/I5: (1993)
- [12] ATLAS Experiment Technical Proposal CERN/LHCC/94-43,LHCC/P2 15 December 1994(tracker performance section of ID chapter)
- [13] S. Roe, Contribution to 2nd Int. Workshop on B-Physics at Hadron Machines, Le Mont St. Michel, France (April 1994)
- [14] S. Gadomski, presentaton at ATLAS Inner Tracker Performance Meeting (October 24, 1994)
- [15] ATLAS Experiment Technical Proposal CERN/LHCC/94-43,LHCC/P2 15 December 1994 (B physics section of physics chapter)
- [16] "B_s mixing measurement in ATLAS": P. Eerola, S. Gadomski and B. Murray ATLAS INDET-NO-039 (17/6/94)
"Measurement of B_s mixing in ATLAS": S. Gadomski
"A possible new layout for the ATLAS Barrel Inner Detector S. Gadomski, S. Roe and P. Weilhammer ATLAS INDET-NO-035 (30/11/93)

- [17] See for example "Tracking for B physics in CMS": J. Hassard and S. Margetides. Proc. Snowmass meeting on B physics in Hadron Colliders, July 1993.
- [18] E.H.M. Heijne et al. *The silicon micropattern detector: a dream?* Nucl. Instr. Meth. A273 (1988) 615 (London PSD Conf.1987)
- [19] H. Spieler *Integrated microsystems as a driving force in modern detector design* Ed. M. Budinich et al., Int. Conf. on the Impact of Digital Microelectronics and Microprocessors on Particle Physics, Trieste 28-30 March 1988 World Scientific, Singapore, 1988 1672
- [20] M. Campbell et al. *A 10 MHz micropattern CMOS front-end for direct readout of pixel detectors* Nucl. Instr. Meth. A290 (1990) 149
- [21] E.H.M Heijne et al. *R&D Proposal: Development of hybrid and monolithic silicon micropattern detectors* CERN DRDC/90-81
- [22] F. Anghiolfi et al. *RD19: Status report on 1993: Development of hybrid and monolithic silicon micropattern detectors* Status Report 1993 CERN DRDC/93-54, presented January 1994
- [23] F. Krummenacher *Pixel detectors with local intelligence: an IC designer point of view* Nucl. Instr. Meth. A305 (1991) 527 (2nd Leuven Pixel Workshop)
- [24] E.A. Vittoz *Tradeoffs in low-power CMOS analog circuits for pixel detectors* Nucl. Instr. Meth. A275 (1989) 472 (1st Leuven Pixel workshop)
- [25] F. Krummenacher *An experimental 10 MHz low power CMOS analog front-end for pixel detectors* Nucl. Instr. Meth. A288 (1990) 176 (5th Munich Symposium 1989)
- [26] N. Redaelli et al. *Performance of a VLSI analogue readout cell for hybrid silicon pixel detectors (ANAPIX)* submitted to IEEE NSS 1994
- [27] L. Bosisio et al. *Measurement and tridimensional simulation of silicon pixel detectors capacitance* IEEE Nucl. Sci. Symp. ConfRecord IEEE 93ch3374-6 (1994) 338
- [28] D.J Pedder *Flip-chip solder bonding for advanced device structures* Plessey Research Review 1989,p.69
- [29] F. Anghinolfi et al. *A 1006 element hybrid silicon pixel detector with strobed binary pitput* IEEE Trans. Nucl. Sci. NS-39 (1992) 650
- [30] M.G. Catanesi et al. *Results from a hybrid silicon pixel telescope tested in a heavy ion experiment at the CERn Omega spectrometer* Nucl. Physics B (Proc. Suppl.) 32(1993) 260 (Como 1992)
- [31] M. Campbell et al. *Development of a pixel readout chip compatible with large area coverage* Nucl Instr. Meth. A342 (1994) 52 (Hiroshima Symp. 1993)
- [32] E.H.M. Heijne et al. *First operation of a 72k element hybrid silicon micropattern pixel detector array* Nucl. Instr. Meth. A349 (1994) 138

- [33] "Silicon PIN Diode Hybrid Array for Particle Detection: Building Blocks for Vertex Detectors at the SSC" G. Kramer et al SLAC-PUB-4942 (May 1989) Presented at 1989 Industrial Symposium on the Supercollider New Orleans LA (February 8-10 1989)
- [34] "Development of a Customized SSC Pixel Detector Readout for Vertex Tracking" O. Barkan et al SLAC-PUB-5358 (October 1990) Contributed to Symposium on Detector Research and Development for the SSC, Ft Worth, TX (Oct 15-18, 1990)
- [35] "Pixel Vertex Detector 1993 Program Overview" Presented by D. Nygren, LBL SSC Pixel Detector Development Collaboration (Adept IC Design, Lawrence Berkeley Laboratory, Berkeley Space Science Laboratory, FNAL, U.C. Davis, Hughes Aircraft Co. U. Iowa, INFN Milano, U. Pavia, U. Pisa, U. Oklahoma-SLAC) Presented at US Department of Energy Review, March 25, 1993
- "A Pixel Unit Cell Targeting 16 ns Time Resolution and Radiation Hardness in a Column Readout Particle Vertex Detector" M. Wright, J. Millaud and D. Nygren LBL 32912 and Proceedings of the International Conference on High Energy Physics and Technology, Como Italy (June 1992)
- "SSC Pixel Array Architecture" J. Millaud et al, and "SSC Pixel Unit Cell Design and Performance" M. Wright et al Presented at the Conference on Front-End Electronics for Silicon Detectors at Future High Luminosity Colliders. Mammoth Hot Springs WY (September 17-19, 1992)
- [36] H. Spieler (LBL) Private communication, June 1994
- [37] Proposal for the Upgrade of DELPHI in the Forward Direction The DELPHI Collaboration: CERN/LEPC/92-13 16 October 1992 also DELPHI 92-142 GEN 135 (October 16, 1992)
- [38] "A Sparse Scan Circuit for Pixel Detector Chips" P. Delpierre and J.J. Jaeger: Nucl. Instr. and Meth. A305 (1991) 627
- "A Sparse Scan Circuit for Pixel Detector Readout" J.J. Jaeger et al: IEEE Trans Nucl Sci NS-40 (1993) 400
- [39] "The Mechanical Structure of the Inner Tracker for ATLAS", A. Fallou, E. Perrin and G. Tappern: Proc. International Workshop on Advanced Materials for High Precision Detectors, Archamps, France (August 28-30, 1994)
- [40] Draft input to Pixel Backup Document of the ATLAS Technical Proposal: LBL, Univ. California Irvine, INFN and Univ. Milano and Univ. Wisconsin, September 1994
- [41] C. Daum "Alignment of the ATLAS Inner Detector" : ATLAS INDET-NO-060 (September 12, 1994)
- [42] "Z Resolution and Placement Precision Requirements for B physics with the ATLAS Silicon Tracker": V. Büscher and A. Weidberg ATLAS INDET NO-054 (June 29, 1994)
- [43] G. Hallewell et al; "A Sonar - Based Technique for the Ratiometric Determination of Binary gas Mixtures": Nucl. Instr. and Meth A 264 (1988) 219

- [44] "Transfert Thermique dans un Detecteur de Particules a Semi-conducteur": L. Patrone (CPPM) (30/6/93) Rapport de Stage de Maitrise de Physique et Applications, Faculté des Sciences de Luminy.
- [45] A. Van Ginneken, Non Ionizing Energy Deposition in Silicon for Radiation Damage Studies, Technical Report FN-522, Fermi National Accelerator Laboratory, 1989
- [46] A. Mekkaoui, private communication
- [47] R. Wunstorff, PhD thesis, University of Hamburg, 1992, DESY FH1K 92-01 (1992)
- [48] "Radiation Damage Estimates in Silicon Detectors S. Roe, Contributed paper to Beauty '94
- [49] "Radiation Damage Projections: Current Status" A. Chilingarov and S. Roe ATLAS INDET-NO-031 (16/11/93)
- [50] The RD2 collaboration, Progress report on the RD2 project, CERN/DRDC/93-18 (March 1993)
- [51] F. Lemeilleur et al, Neutron, Proton and Gamma Irradiations of Silicon Detectors, CERN/ECP 93-8, (Sept 93)
- [52] Z Li, Investigation on the Long-term Radiation Hardness of Low Resistivity Starting Silicon Material..., Brookhaven National Laboratory, BNL 60155 (Feb 1994)
- [53] D.J. Pedder, Plessey Research Review, 1989 (Proprietary process of GEC Marconi Materials Technology Centre, Caswell, Towcester, UK)
- [54] "A Mixed Analogue-Digital Radiation Hard Technology for High Energy Physics Electronics: DMILL" ("Durci Mixte sur Isolant Logico-Linéaire") M. Dentan et al: CERN DRDC RD Proposal CERN/DRDC/92-31 DRDC/P42 (May 14, 1992)
- [55] "A Demonstrator Analogue Signal Processing Circuit in a Radiation Hard SOI - CMOS Technology" F. Anghinolfi et al: CERN DRDC R and D Proposal CERN/DRDC/90-79 DRDC/P21 (December 11, 1990)
- [56] J.P. Colinge, Silicon-On-Insulator Technology: materials to VLSI, Kluwer Academic Publishers, 1991.
- [57] J.L. Leray et al. "From substrate to VLSI: investigation of hardened SIMOX without epitaxy, for dose, dose rate and SEU phenomena", IEEE Trans. Nucl. Sci., Vol 35, No 6, pp 1355-1360.
- [58] J.L. Leray et al. "CMOS/SOI hardening at 100 Mrad(SiO₂)", IEEE Trans. Nucl. Sci., Vol 37, No 6, pp 2013-2019.
- [59] T.P. Ma and P.V. Dressendorfer, (Eds.), "Ionizing Radiation Effects in MOS devices and circuits." New York: Wiley-interscience, 1989.

- [60] P.J. McWhorther and P.S. Winokur, "Simple Technique for Separating the Effects of Interface Traps and trapped Oxide Charge in Metal-Oxide-Semiconductor Transistors.", *Appl. Phys. Lett.*, vol. 48, pp 133-135, 1986.
- [61] L.A. Glasser and D.W. debberpuhl, *The Design and Analysis of VLSI Circuits*. Addison Wesley 1985.
- [62] A. Mekkaoui. "Prototype ??"
- [63] "Study of a cmos-jfet-bipolar radiation hard analog-digital technology suitable for High Energy Physics Electronics", M. Dentan et al., *IEEE Trans. Nucl. Sci.* 40(6), p1555, December 1993.
- [64] "Radiation effects on SOI analog devices parameters", O. Flament et al., *IEEE Trans. Nucl. Sci.* 41(3), p565, Juin 1994.
- [65] "A Mixed Analogue-Digital Radiation-Hard Technology for High Energy Physics Electronics". RD 29 Status Report, CERN/DRDC/93-45, 19 October 1993.
- [66] "Study of proton radiation effects on analog IC designed for high energy physics in a BiCMOS-JFET radhard SOI technology", L. Blanquart et al., submitted for publication in *IEEE Trans. Nucl. Sci.* december 1994.
- [67] "Heavy ion sensitivity of SRAM in SOI bulk-like technology", V. Ferlet-Cavrois, O. Musseau, J.L. Leray, Y.M. Coic, J.L. Pelloie, presented at RADECS, France (1993).
- [68] "Systeme de Lecture d'une Matrice de Pixels pour LHC" V. Bonzom CPPM Pixel Internal Note 3 (November 4, 1993) also Slides presented by V. Bonzom at RD19 meeting November 24-25, 1993
- [69] "Status Report on the RD23 Project: G. Stefanini et al: CERN/DRDC 94-38, 6 October 1994
- [70] "A Proposed VLSI Device for Particle Detection: S. Parker et al: *Nucl. Instr and Meth.* A 275 (1989) 494
- [71] "Performance of a Monolithic Pixel Detector" C. Kenney et al *Proceedings of the International Conference on High Energy Physics and Technology, Como Italy (June 1992)*
- [72] "Monolithic Pixel Detector Results: Tracking at 500 GeV/c" S. Parker et al Presented at the Conference on Front-End Electronics for Silicon Detectors at Future High Luminosity Colliders. Mammoth Hot Springs WY (September 17-19, 1992)
- [73] S. Parker (Univ Hawaii): Private Communication (June 1993)
- [74] "Monolithic Pixel Detector Design Based on Bond and Etch-Back SOI" S. Mani Presented at the Conference on Front-End Electronics for Silicon Detectors at Future High Luminosity Colliders. Mammoth Hot Springs WY (September 17-19, 1992)

- [75] "Development of Silicon Micropattern (Pixel) Detectors" P. Delpierre et al: Nucl. Instr. and Meth. A 315 (1992)133
- [76] "Detector Diodes and Test Devices Fabricated in High Resistivity SOI Wafers": L. Bosisio et al IEEE Trans Nucl Sci NS-40 (1993) 230
- [77] "Integration of CMOS Electronics in an SOI Layer on High Resistivity Silicon Substrates" B. Dierickx et al IEEE Trans Nucl Sci NS-40 (1993) 414
- [78] "Fully Integrated CMOS Pixel Detector for High Energy Particles" G. Vanstraelen et al Nucl Instr and Meth A275 (1989) 574
- [79] "Monolithic Integration of Solid State Particle Detectors and their Read-out Electronics on High Resistivity Silicon" G. Vanstraelen: PhD Thesis, Katholieke Universiteit Leuven, (December 1990)
- [80] "Design and Performance of Semiconductor Detectors with Integrated Amplification and Charge Storage Capability" : B. Heinemann et al: Nucl. Instr and Meth. A 305 (1991) 517
 J. Kemmer and G. Lutz Nucl. Instr and Meth. A 253 (1987) 365
 J. Kemmer et al: Nucl. Instr and Meth. A 288 (1990) 92
- [81] C.DaVia et al., *A hybrid pixel detector for the readout of scintillating fibres*, Contributed paper to ICHEP - 94 Conference, Glasgow, 20-27th July, 1994
- [82] J.Ludwig, *GaAs Microstrip Detectors*, Contribution to I.C.H.E.P. 94, Glasgow July 20-27th, 1994
- [83] V.B.Chmill et al., *Radiation Resistans of GaAs Structures Based on $\pi - \nu$ Junction*, ATLAS Internal Note INDET-NO-036, 3rd February, 1994;
 I.H.E.P. Preprint 93-95, Protvino 1993 (in Russian)
- [84] V.B.Chmill et al., *GaAs Detectors based on $\pi - \nu$ Structures*, Nucl.Instr. and Meth. in Phys.Res. **A326**, (1993) 310;
Exploration of GaAs structures with $\pi - \nu$ junction for coordinate-sensitive detectors Nucl.Instr. and Meth. in Phys.Res. **A340**, (1994) 328;
- [85] "Development of Diamond Tracking Detectors for High Luminosity Experiments at the LHC" RD proposal CERN/DRDC 94-21 DRDC/P56 (May 5, 1994) RD42 Diamond Detector Collaboration (Univ. Aveirio, Univ. Bristol, CERN, MPI Heidelberg, Lawrence Livermore NL, Los Alamos NL, CPPM, INFN Milano, Ohio State Univ., Univ. Pavia, Rutgers Univ., LEPSI, Strasbourg, Inst. Hochenergiephysik, Vienna)
- [86] M.A. Plano et al., Appl Phys Lett 64 (1994) 193, S. Zhao, "Characterization of the Electrical Properties of Polycrystalline Diamond Films" PhD thesis, Ohio State University (1994)
- [87] F. Borchelt et al; submitted to Nucl. Instr and Meth (1994)

- [88] R.J. Tesarek et al; submitted to Nucl. Instr and Meth (1994)
- [89] C. Colledani et al: "A High Resolution Beam Telescope" CRN-LEPSI note, to be published
- [90] E. Nygard et al: Nucl Insrt and Meth A 301 (1991) 506
- [91] Presentation by H. Kagan at RD42 Collaboration meeting, LEPSI, Strasbourg, August 29,30, 1994
- [92] E.R Vance et al J. Phys D5 L40 (1972)
- [93] S. Dannefaer and D. Kerr: Diamond Related Matter 1, 407 (1992), G. Davis et al Phys Rev B46, 13157(1992), D. W. Palmer in "Properties of Diamond - a Data Review" ed. G. Davis, (IEEE London, 1994)
- [94] E. W. Mitchell in "Physical Properties of Diamond." ed. R. Berman (Clarendon, Oxford, 1965)
- [95] L. S. Pan et al Lawrence Livermore National Laboratory, CA 94551, USA; Private communication (1994) work in progress, to be submitted to Appl Phys Lett
- [96] E.R Vance et al J. Phys D5 L40 (1972)
- [97] Handbook of experiments at CERN, 1993; ISSN 0259-093X, November 1993, p7
- [98] M. Morpurgo; Cryogenics, July 1979, p 411