Silicon strip vertex detector for ATLAS

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Abstract

Technical aspects of the proposal to build a vertex detector of silicon micro-strips for ATLAS [1] are discussed. All parameters have been optimized for physics performance: radiation length $< 0.5\%\ X/X_0$, resolution in $R\varphi \sim 10\mu$m and resolution in $z \sim 20\mu$m. The proposal is based on existing technologies and on experience from the DELPHI Vertex Detector.

1 Motivation

The impact parameter resolution given by a cylindrical detector layer can be parameterized in the following way:

$$\sigma_{\rm IP} = A \oplus \frac{B}{p_{\rm T}} \frac{1}{\sqrt{|\sin\theta|}} \tag{1}$$

$$\sigma_z = A_z \oplus \frac{B_z}{p_{\rm T}} \frac{1}{\sqrt{|\sin\theta|^3}} \tag{2}$$

where A is the asymptotic resolution for high transverse momentum charged particles and B is the multiple scattering term. The dependence of both terms on the first layer radius is shown in Fig.1 for different resolutions and radiation lengths.

For B-physics studies, where typical track momenta are of the order of a few GeV, it is essential to minimize the multiple scattering contribution to the measurement error. The radiation length of the innermost layer should be minimal. For other physics, involving heavier objects (e.g. t-quark), where track momenta are higher, it is more important to improve the resolution in order to reduce the asymptotic term. For both, it is advantageous to reduce the innermost layer radius.

We propose to build the vertexing layer using double sided silicon strip technology. Silicon strips offer the best performances in the critical aspects discussed above: spatial resolution below 10 μm for $R\varphi$ and below 20 μm for z readout with

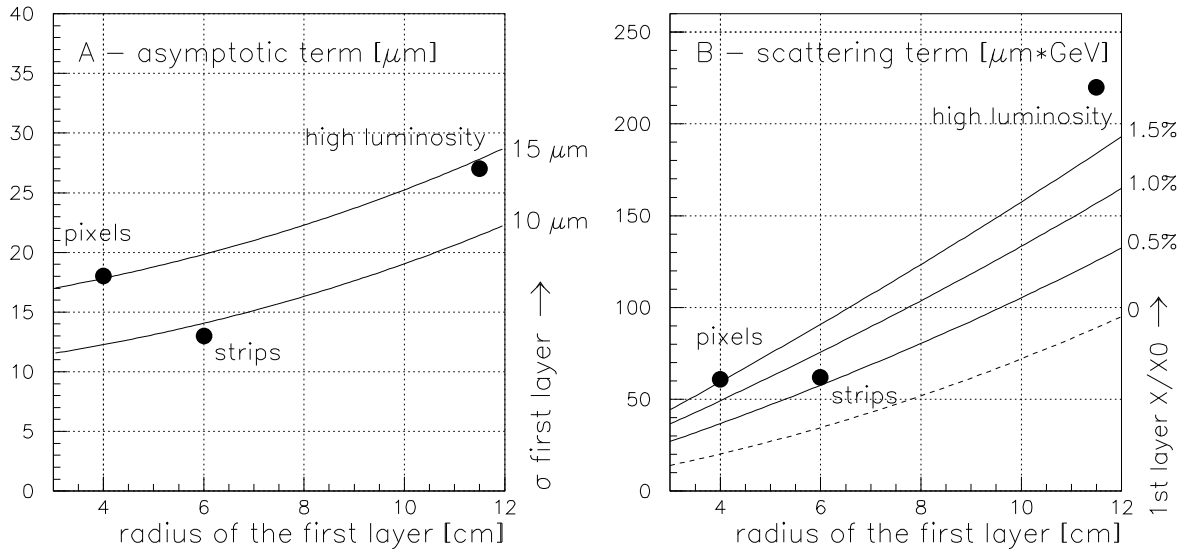

Figure 1: Asymptotic and multiple scattering terms of the impact parameter resolution versus the innermost layer radius. Lines represent approximate analytical calculations. Points represent Monte-Carlo calculations for the different variants of vertexing layers of ATLAS Inner Detector.

$< 0.5\%$ X/X0. The layout is similar to the one used in the DELPHI Vertex Detector, having no electronics and almost no support structures in the active region.

The radius of the silicon micro-strip vertex detector was tentatively set to 6 cm at the time this detector was proposed [1]. According to present radiation damage predictions this would allow 5 to 6 years of low luminosity operation. It should also be possible to operate such detector for one year at the intermediate luminosity of $5 \cdot 10^{33}\ cm^{-2}s^{-1}$. Both radiation damage predictions and occupancy calculations indicate, that the radius can be decreased to $\sim$ 4 cm if only low luminosity running is foreseen. The final decision on this parameter will be taken when more precise radiation damage predictions are available and a more complete study of pattern recognition has been carried out. An artists view of the layer is shown in figure 2, with a 6 cm layer radius and a 5 cm beam-pipe diameter.

The readout scheme proposed in this paper is based on existing bipolar amplifiers and allows 52 cm long detector modules. Assuming a radius of 6 cm this gives a rapidity coverage of $|\eta| < 2.2$ (or $|\eta| < 1.5$ subtracting 2σ of the primary vertex distribution from the length).

Impact parameter resolution degrades for small polar angles, and is not useful beyond $\eta \sim 2$. Any extension of a vertex detector does not justify sacrifices in resolution of the central part.

The impact parameter resolution given by the layer, in the present layout of

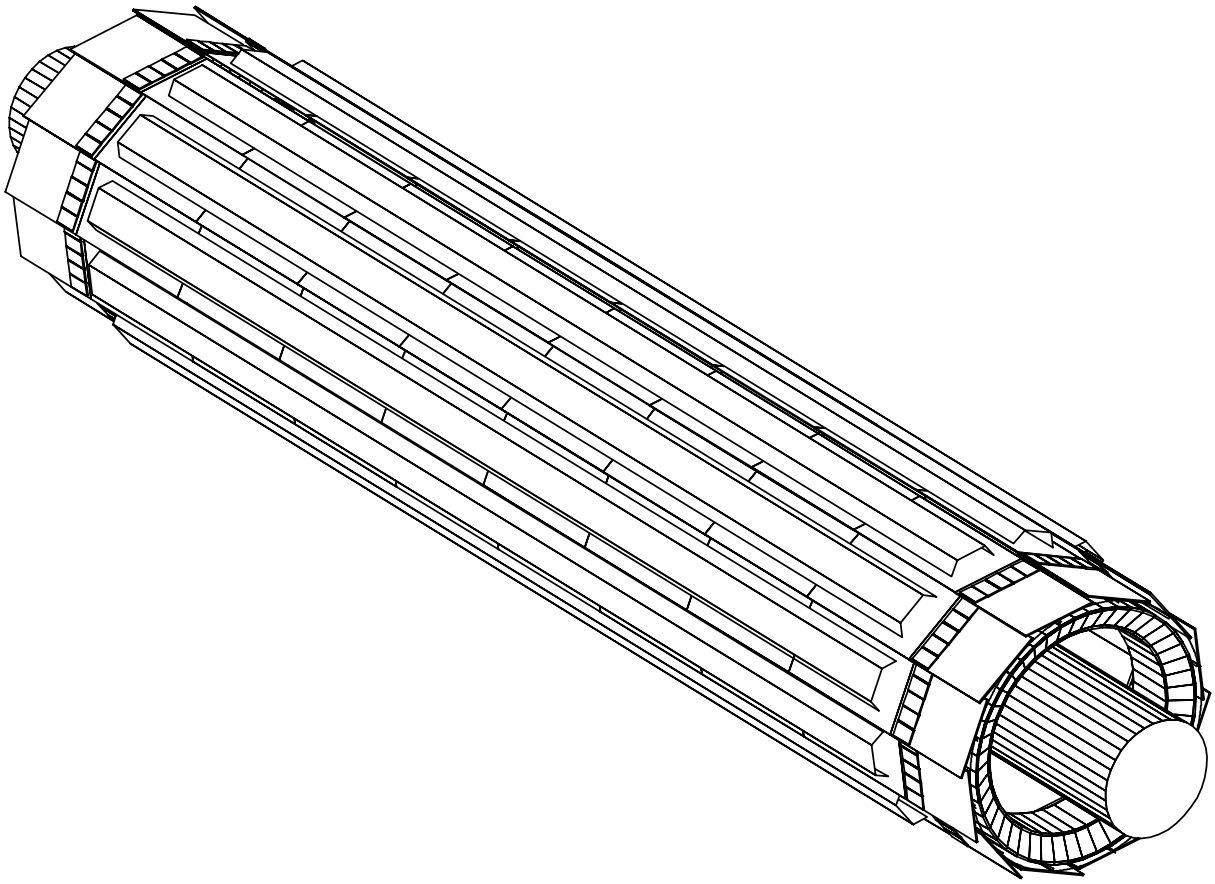

Figure 2: A view of the silicon strip vertex detector.

ATLAS ID, is

$$\sigma_{\rm IP} = 13 \oplus \frac{62}{p_{\rm T}} \frac{1}{\sqrt{|\sin\theta|}} \quad [\mu{\rm m}] \tag{3}$$

$$\sigma_z = 39 \oplus \frac{90}{p_{\rm T}} \frac{1}{\sqrt{|\sin\theta|^3}} \quad [\mu{\rm m}] \tag{4}$$

($p_{\rm T}$ in GeV), for 6 cm radius.

2 Detectors

The basic sensors are assumed to be double sided, double metal silicon strip detectors 6.5 cm by 3.3 cm, with strips crossed at 90 degree. The $R\varphi$ readout will be done using p-side strips with 50 μm readout pitch and 25 μm diode pitch. Four units will be tailored together forming 26 cm long half-modules. This geometry should achieve a resolution of about 10 μm , taking into account the signal-to-noise ratio which is expected due to the big capacitive load (see next section).

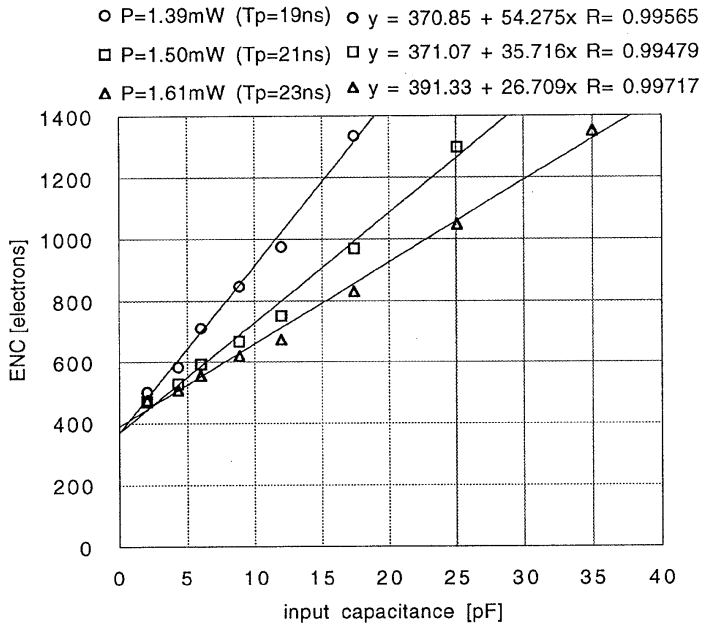

Figure 3: Measured noise slope of the bipolar amplifier designed for NA50 experiment

For the z readout we propose to use the n-side strips with 200 μm readout pitch. Capacitive charge division should allow to reach a resolution of $\sim 20\mu$m. The widths and the number of intermediate strips will be optimized to minimize the charge loss due to backplane capacitance.

Since the readout electronics will be placed only at the end of a module the baseline option for the detectors is double metal technology. Alternatively we have at our disposal another well proven technique, namely the fanout using kapton cables, which introduces only a small additional amount of material.

Because the vertexing layer will be placed at a radius of 6 cm or lower the radiation damage to the detectors is a critical issue. The increase of depletion voltage will be the limiting factor determining the detector lifetime. Estimates of radiation damage predict lifetimes of 5 to 6 years at 10^{33} $cm^{-2}s^{-1}$ [1]. An expected leakage current is $\sim 2\mu$A per strip after 5 years, assuming detector cooling to $\sim 0°$C.

Occupancy from minimum bias events is about 1% at L=10^{33} $cm^{-2}s^{-1}$ assuming 26 cm strip length.

3 Front-end electronics

The layout of the vertexing layer results in a big capacitive load for the front-end electronics. The deconvolution CMOS front end electronics would have to be run with a high drain current in the input stage in order to achieve tolerable noise levels with this high capacitance. An alternative solution would be to use front-

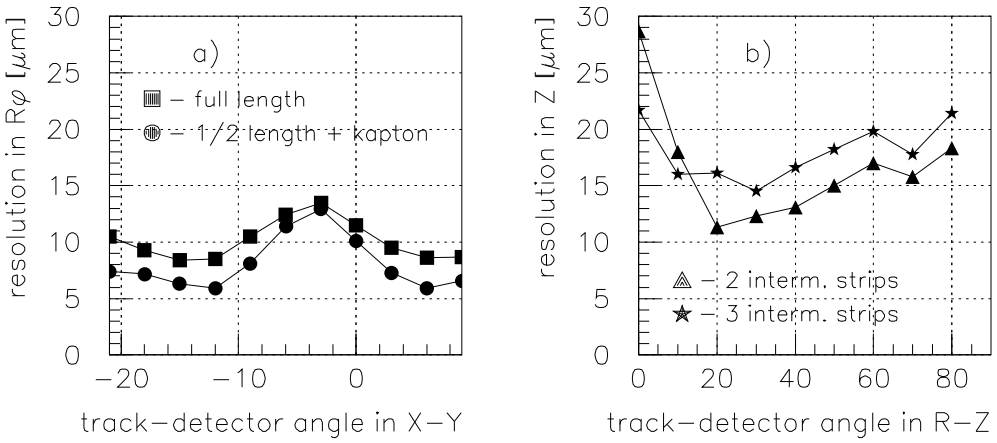

Figure 4: Spatial resolutions in $R\varphi$ and in z as a function of track-detector angle. In both cases the angle is in the plane orthogonal to strip direction.

end electronics based on a bipolar input transistor. Three versions of fast bipolar front-end electronics have been developed; two for the SDC silicon tracker and one for the NA50 silicon multiplicity detector. The noise of the NA50 chip has been measured at different currents used in the input stage. Very promising results which have been obtained are shown in figure 3. For a capacitive load of 35 pF, a noise $<$ 1400 electrons has been measure with a total power dissipation of 1.6 mW/channel, including the preamplifier, the shaper and the discriminator.

2μA of leakage current per strip introduces some extra parallel noise - 700 electrons for the bipolar amplifier with 20 ns peaking time and 480 electrons for the deconvolution CMOS front-end. The shaping given by deconvolution reduces the parallel noise [2], but in both cases the series noise due to detector capacitance is dominant.

To obtain the required spatial resolution capacitive charge division will be used and therefore the pulse height information is required. The bipolar preamplifier-shaper chip will be followed by an analog data buffer and sparse data scan circuitry. The possible readout schemes are those proposed for the main silicon tracker and no extra development will be needed, except for the adjustment of the preamplifier.

4 Spatial resolution

A Monte-Carlo program [3] was used to calculate the spatial resolution from the detectors and readout electronics discussed above. The program simulates charge collection in a silicon detector and generation of the current pulses on readout strips. Response of the front-end electronics is then calculated using SPICE. The full equivalent circuit of the strip detector as well as models of front-end electronics including noise parameters were implemented. Finally realistic cluster search and position

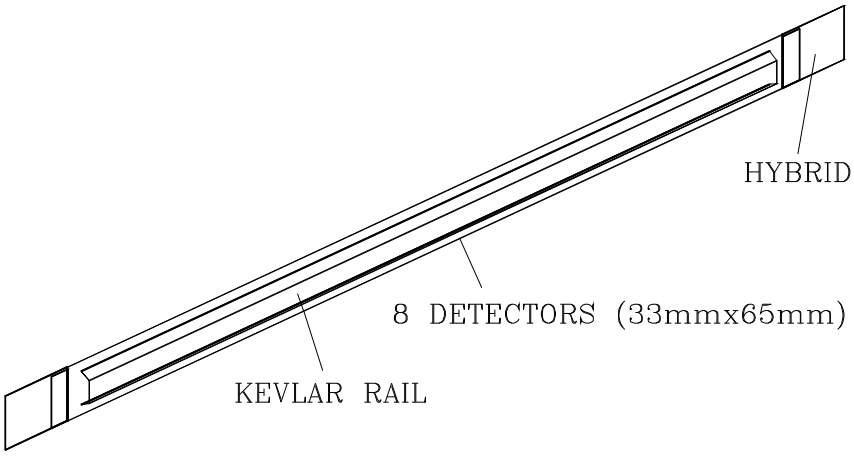

Figure 5: A view of the detector module

calculation algorithms are used to determine spatial resolution and efficiency. The program agrees well with existing experimental data for different strip pitches.

We assume strip capacitance values of 1.2 pF/cm for 50 μm readout pitch and 25 μm strip pitch on p-side, 0.5 pF/cm for kapton fanout, 1.5 pF for 200 μm readout pitch and 67 μm strip pitch on n-side. Results for the 26 cm long half-module are shown in figure 4 for $R\varphi$ and z strips. In both cases the scanned angle is in the plane perpendicular to strips. For a 3.3 cm wide detector placed at a radius of 6 cm and rotated 6 degrees (see section 5) angles between -21 and +9 degrees are of interest in X-Y plane.

In case of $R\varphi$ even with 26 cm long strips the average resolution is $\sim 10\mu$m. This could be improved by using 13 cm long strips and a kapton fanout. For tracks at -3 degrees the Lorentz angle compensates the track angle and the charge is collected practically on one strip, this deteriorates the resolution.

In case of z strips the resolution given by 200 μm pitch with one intermediate strip is adequate for all tracks except for a small fraction of almost exactly perpendicular ones. The benefits of varying the strip pitch along z will be investigated.

The studies of different readout pitches and connection schemes will continue in order to optimize these parameters.

5 Mechanical structure and cooling

The mechanical design of the vertexing layer is based on experience from the DELPHI Vertex Detector. An 8 detector long module will have all the readout electronics and its cooling placed near the end-rings. Essentially only silicon detec-

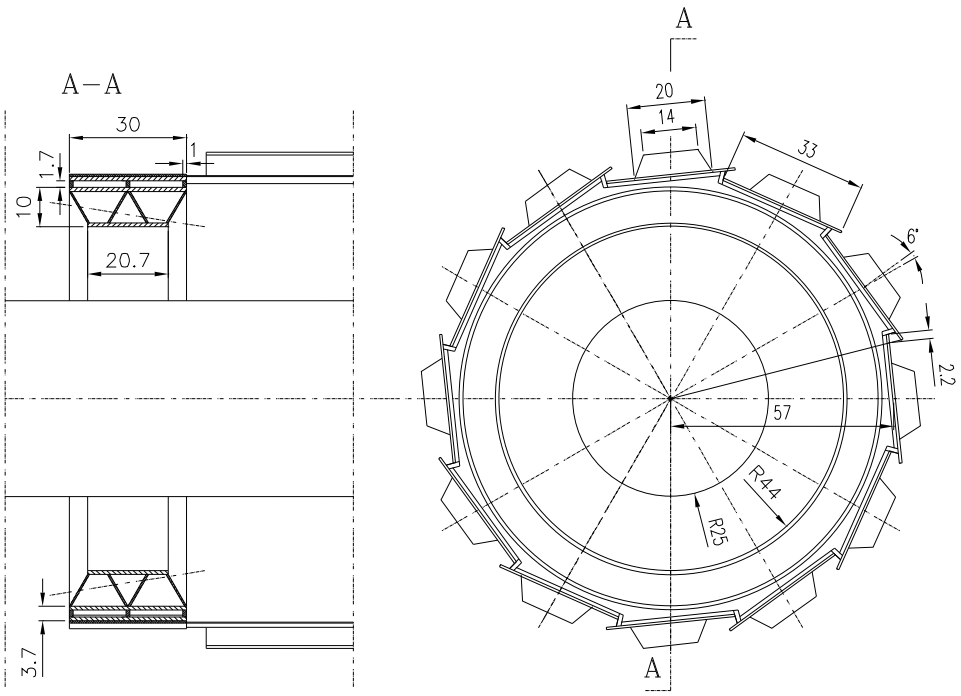

Figure 6: Cross-section of the end-ring support structure (left) and a view of the layer seen in X-Y plane (right)

tors remain in the active area of the layer. Mechanical stability is given by a light weight kevlar fiber structure glued to the detectors. This is shown schematically in Fig.5. The chosen solution minimizes multiple scattering.

Similar modules of 48 cm length have recently been constructed for DELPHI. Mechanical stability measurements have been done and the modules fulfill the requirements for DELPHI Vertex Detector.

Arrangement of the detector modules is shown in Fig. 6. 12 modules of 3.3 cm width are needed to form a layer of 5.7 cm average radius. Small overlaps in $R\varphi$ plane are include to allow the alignment with tracks.

Cross-section of the end-ring, made from carbon fiber is also shown in Fig. 6. Aluminum, as used in DELPHI Vertex Detector, is a possible backup. More studies and construction of prototypes are needed before a decision on this point can be taken.

A cooling channel of ~ 12 mm^2 cross-section will be sufficient to extract the heat produced by the readout electronics. The maximum radiation length of the end-ring support structure including cooling pipe is $\sim 4\%\ X/X0$, localized in the $2.2 < |\eta| <$

Table 1: Cost For ATLAS Silicon Vertex

item	specification	MSFr
Detectors	Prototyping	0.18
	Number requ'd (incl Assembly loss) 144 90SFr/cm^2 ie 1,930/detector	0.28
	Total (excluding contingency 0.12)	0.46
Fanins	144 @ 1000SFr/Set(+10%R&D)	0.16
Electronics	Frontend developement	0.20
	Incremental cost 3SFr/Channel	0.14
	Total(excl 0.1MSFr contingency)	0.34
Hybrids	Number requ'd 144 (400SFr/Hybrid + Prototype)	0.07
Engineering	Design/Purchase/Supervision	0.05
	Module Assembly	0.05
	Kevlar structures	0.10
	Cooling(Liquid,Gas)	0.05
	Tooling for installation	0.10
		0.35
	Total (excl 0.3 contingency)	1.38

The numbers:

1	Cylinder	
12	Ladders	Aim to build 18
2	Modules/Ladder ie 24	36
4	Detectors (33mmx65mm)/Module ie 96	Purchase 144
640	Readout channels/module side ie 30,720channels (240chips)	Purchase 360

2.5 rapidity range. The ceramic hybrid and readout electronics contribute another 4% $X/X0$ in the narrow $|\eta|$ region of 2.2 to 2.3 because of the shallow angle.

It is expected that temperature of detectors will have to be maintained at the level of 0 to 5 degrees C and the cooling of the vertex detector will be integrated with other SCT components.

6 Cost

The costing shown in table 1 is done under the following assumptions:

1. The Vertex layer is costed as an incremental cost to the SCT tracker.
2. Detectors - 2 prototype runs + production, 90 SFr/cm^2
3. Electronics- 2 prototype runs for Front-end. Back-end and readout is standard

ATLAS ie 3 SFr/channel

4. Mechanics - Cost sensitive to the amount of inhouse effort available
5. Cooling - Assumes incremental cost

7 R&D program

The development of the double-sided detectors which give the best performance in spatial resolution is the central task. The most suitable technology is to use double-metal technology in order to route the z-strips to the end of the detector. Technology has been developed by SI, Hammamatsu, Micron and CSEM. Very promising results have been achieved so far in prototype runs, studying different implementations [4]. The main technical issues to improve on are to minimize the number of pinholes in the oxide and to improve stability of p^+n and n^+n strips w.r.t. micro discharges. The time scale to develop a detector which performs according to the specification is the end of '95.

The readout electronics will be only slightly different to that which is being developed for the main SCT tracker. Optimal adaptation of the input FET in the preamplifier for the CMOS implementation to the higher detector capacitance can be achieved with minimal design effort. The chips can be produced as a by-product of the main development in the same engineering runs in the foundries. First prototype 128-channel chips will be available by the end of '95.

Similarly, a bipolar amplifier for the vertex detector can be developed as a byproduct of the main bipolar development for the SCT. An optimum size of the input transistor has to be chosen to reduce the base spread resistance noise and keep the current density at an acceptable level with radiation effects in view. In addition the current in the input stage has to be tuned for an optimum balance between the series and parallel noise.

The mechanical and cooling structures will have to be developed by following up similar designs as those used in the DELPHI micro-vertex detector.

In 1996 it is planned to build 4 - 6 half-modules for inclusion in the BSP detector, allowing a final evaluation of the overall system.

References

[1] S.Gadomski, S.Roe and P.Weilhammer, *A possible new layout for barrel part of ATLAS ID*, ATLAS Internal Note INDET-NO-035, 30 November 1993

[2] S. Gadomski, G. Hall, T. Hogh, P. Jalocha, E. Nygard and P. Weilhammer, *The deconvolution method of fast pulse shaping at hadron colliders*, Nuclear Instruments and Methods A 320(1992) 217-227

[3] W.Dabrowski, private comunication

[4] F. Djama et al.*Double-Sided Double-Metal AC-Coupled Silicon Microstrip Detectors*, Contribution to the 6th Pisa Meeting on Advanced Detectors, La Biodola, 1994.