ATLAS Internal Note
INDET-NO-039
28 February 1994

Version 1.2
28 February, 1994

Simulation of Silicon Strip Readout in the ATLAS Inner Detector.

A. G. Clark, X. Wu
DPNC, Université de Genève.

G. N.Taylor
School of Physics, University of Melbourne, and PPE Division, CERN.

1. Introduction.

Making use of the capacitance between strips, not all elements of a silicon strip detector need be read out. Capacitive charge division can, in principle, lead to a position resolution which is determined by the element pitch, rather than the readout pitch. However, the method relies on a comparison of the charge distributed to neighbouring readout strips and is thus limited by the signal to noise ratio that can be obtained from the electronics [1].

In the case of the ATLAS Inner Detector silicon layers, at relatively large radii, large detector elements are necessary, and thus the capacitance of the elements is considerably larger than in previous experiments where capacitive charge distribution was used. Coupled with this is the need for front-end electronics with shaping times 20-50 times smaller than in the previous experiments and with lower power dissipation. The inherent signal-to-noise ("S/N") ratios for these preamplifiers is larger and they have a steeper slope with input load capacitance.

To compare the charge division readout with the direct readout of all strips, we have studied two options with an equal density of readout channels:

- 12cm strips of 100μm pitch and direct readout (**Option A**).
- 6cm strips with charge division at 200μm readout pitch (**Option B**),

The possibility of 12cm long strips with charge division readout was found to offer too large an input capacitance for further consideration. A version of Option A with 6cm strips would require twice as many channels of front electronics as that of Option B. The two options chosen thus provide a good comparison of the relative benefits of the two readout methods.

We assume the use of single sided n-type silicon detectors with segmentation provided by p-type implants on the top side.

No consideration is made of "z-pads", where charge division readout is less attractive because of the granularity.

For our studies, we assume the silicon detectors have dimensions 60*51.2*0.3 mm^3, and that they are twinned in Option A to provide strips of length 12cm. We attempt to make the simulations as realistic as possible; nevertheless we accept that the results of each scenario are somewhat optimistic (non-random noise, parasitic capacitances, the use of a step-function comparator etc).

It is shown that noise is the limiting factor in the performance of detectors, with and without capacitive charge sharing.

In section 2, we describe in detail the assumptions of detector and readout design that have been made. In section 3, we show results for each option, detailing limitations due to the readout noise and charge collection inefficiency, on the position resolution and the cluster reconstruction efficiency. The effect and validity of varying the assumed parameters (threshold, inter-strip

capacitance, etc) is then discussed. In section 4, we summarise and compare the results, on the basis of these considerations.

2. Detector and readout design.

In the Appendix, can be found a detailed description of the most important effects that must be considered for charge division readout. The first is the total load capacitance, which increases amplifier noise The second effect is the efficiency for charge collection, which depends on the number of floating strips between readout strips. The charge collection efficiency is sensitive to the ratio of the interstrip capacitance to the capacitance of the strip to the backplane of the detector. The effects considered result in a significant restriction of the position resolution from that which is possible without noise limitations.

Below is listed a comparison of the load capacitance of Option A, with Option B having a single floating strip between each readout strip. The ratio of the interstrip capacitance, C_i, to the capacitance of each strip to the backplane, C_d , is assumed to be 4. These geometries have the same number of readout channels per silicon area. The ratio C_i / C_d for Option A was assumed to be 0.85, (for reasons which become apparent below). A silicon thickness of 300μm is assumed throughout. Also included in all calculations of the load capacitance is a additional 2pF to account for stray capacitance, inevitable in real detector layouts. Although the Option B has a similar load capacitance, it will be shown that it will significantly affect the achievable position resolution using capacitive charge division.

Layout Option	Detector Thickness (μm)	Strip Length (cm)	Readout Pitch (μm)	Strip Pitch (μm)	C_{load} (pF)
A	300	12	100	100	13.1
B	300	6	200	100	13.6

Table 1. Comparison of Option A and Option B (with a single floating strip and with Ci/Cd=4).

As shown in the Appendix the capacitive load can be reduced by increasing the number of floating strips between readout strips, or by reducing the ratio C_i/C_d. However this comes at the cost of reduced charge collection efficiency, and increased detector complexity.

Increasing the number of strips can lead to better position resolution but only if sufficient S/N can be achieved.

To more fully explore the potential for capacitive charge division readout, a simple Monte Carlo study was performed. Various geometries were considered to compare the direct readout with charge division readout.

3. Monte Carlo Study

A layer of silicon counters at radius 50cm was investigated. Counters of 51.2mm width and either 6 or 12cm length were considered. In Option A the counters were assumed to be direct coupled, with each strip a readout strip. In Option B readout strips were assumed to be capacitively coupled, with additional "floating strips" between readout strips. The floating strips were assumed to be uniformly distributed, so that the element size is determined by the overall strip pitch, including the floating strips and detector strips equally.

In evaluating the charge deposition we consider tracks at η=0. With a detector radius of 50cm tracks will traverse the detector at angles of up to 51mrad from the perpendicular to the detectors.

Tracks were generated uniformly in ϕ from one ϕ-edge of the detector to the other. The lengths of each track through each detector element were calculated. Landau distributed signal charge is calculated for each element. Diffusion and magnetic field effects are neglected.

In the case of the capacitive charge division readout, the distribution of the charge from the strip where it is collected to the readout strips is calculated as described in the Appendix.

The load capacitance at the input of the amplifiers is calculated as described in the Appendix. The amplifier noise (rms) is then determined from the load to be [800 + 80×C_l(pF^{-1})] electrons[2]. (As described below, a more optimistic noise is assumed for some of the capacitive charge division options considered.)

The radiation induced dark current and resulting shot noise, is calculated according to the volume of silicon given by the readout channel pitch. This has been shown to be a good approximation in SPICE simulations. The shot noise is assumed to be given by the usual expression:

$$\sigma_{shot}(electrons, rms) = 112\sqrt{\tau_s(ns).I(\mu A)}$$

where τ_s is the shaping time in nsec, and I is the dark current in μA. It was assumed that τ_s=25ns. The shot noise from each strip is reduced by capacitive signal loss in the same way as the signal.

The dark current was determined from the calculated neutron equivalent fluence[3]. At a radius of 50cm this fluence is 0.625x10^{13}n.cm^{-2} per high luminosity (1x$10^{34}cm^{-2}s^{-1}$) year. The total fluence was then calculated for ten years running with a luminosity profile of three years at 1x$10^{33}cm^{-2}s^{-1}$ and seven years at 1x$10^{34}cm^{-2}s^{-1}$ average luminosity, to yield an equivalent fluence of 4.6x10^{13}n.cm^{-2}.

In the expression for the radiation damage induced current per unit silicon volume,

$$\frac{\Delta I}{\Delta V} = \alpha.\Phi$$

the constant α was taken to be 8x10^{-17} A.cm^{-1} with an unannealed fraction of 30%. It was also assumed that the operating temperature was 0°C, resulting in a factor of five in the reduction of the current expected at 20°C. These radiation damage parameters yield the conservative estimate for the current of 0.79μA per readout channel.

Charge loss from radiation damage was assumed to be 1.5% per 10^{13}n.cm^{-2}.

The amplifier noise and shot noise were Gaussian sampled noise and then added to all amplifier channels.

Once the signals to the amplifiers had been simulated, a simple procedure was followed to reconstruct the position of the particles traversing the silicon.

Based upon the noise distribution, a discriminator threshold was set. This should be typically 4σ of the noise pedestal to maintain an acceptably low occupancy. From the remaining signals, clusters of contiguous channels with signals above threshold were found around the maximum signal for the event. The maximum signal in almost all generated events was associated with a "real" charge pulse.

The reconstructed position was determined from the signal weighted average of the central position of each readout strip in the cluster. The data presented were obtained from 10,000 generated tracks in each option considered, thus the statistical errors are of order 1%.

Within the Option B, assuming charge division readout, several parameters were varied to understand better their effect. Table 2 lists the variants simulated.

Option	Readout Pitch (μm)	Strip Pitch (μm)	Ratio C_i/C_d	Charge Coll. Eff. (%)	C_{load} (pF)	Amplif. noise (electrons rms)	Shot Noise (electrons rms)	Total Noise (electrons rms)
A	100	100	0.85	93.2	13.1	1846	463	1903
B1	200	100	5	86.7	13.6	1891	431	1940
B2	200	100	3.5	85.2	11.3	1701	423	1753
B3	200	100	2	81.8	8.6	1491	406	1545
B4	200	67	5	81.1	8.8	1507	403	1560
B5	200	50	5	74.4	6.9	1348	370	1398

Table 2: List of options compared in the Monte Carlo studies.

3.1 Results:

The primary goal of the study was to compare position resolution for the options considered.

3.1.1 Readout on all strips

The signal charge distribution for Option A is shown in figure 1(a). A minimal cut of 2000 electrons has been applied to the data in this plot. The clear separation between signal and noise allows a clean (and insensitive) 4σ discriminator cut which little affects the position resolution, simply given by ≈(Pitch/√12).

The distribution of [rϕ(reconstructed) - rϕ(actual)] is also shown for Option A in figures 1(b)-(d), for noise cuts of 3σ, 4σ and 5σ . The plot shows a uniform distribution between the minimum and maximum values determined by the strip pitch (±50μm) with an rms value of 27μm. This is slightly better than expected for a single element of width 100μm due to tracks which pass through two cells. A summary of these results are shown in table 3.

3.1.1 Charge Division

In the case of charge division readout, the distribution of signal charge is much broader, and is no longer well separated from the noise. The discriminator setting is thus an important factor. A low setting will result in the most of the charge being available for position reconstruction. As the level is increased more of the small signals will be cut resulting in the degradation of the position resolution. It is generally accepted that a 4σ cut is required. Figure 2(a), shows the amplifier charge distribution for Option B1 with the 3σ, 4σ and 5σ cuts marked as vertical lines. Figures 2(b), (c) and (d), show the position resolution with these three cuts applied. Table 3 summarises the results.

With the addition of the floating strip between the readout channels the position resolution can in principle, attain a value of (200/2)/√12 or 28.9μm. The ultimate resolution is defined by the strip pitch, not the readout pitch. The central region of the plots correspond to this resolution.

However, with the noise expected for this configuration, the need to apply a discriminator threshold causes a loss of some signals with the corresponding distortion in the weighted mean of the remaining signals. Thus as the threshold is raised, "tails" in the resolution distribution are formed out to the value defined by the amplifier pitch (in this case 200μm). The tails occur in steps determined by the number of floating strips.

The integral of the tails give a measure of the inefficiency in charge collection with an applied threshold cut.

From the information presented, it is clear that the large noise associated with the high load capacitance results in the relatively high discriminator threshold required. It thus leads to the signal loss and a subsequent degradation of resolution.

From the consideration given in the Appendix, it follows that in the regime with strip pitch larger that about 50μm, the capacitance and hence the amplifier noise, can be reduced by increasing the number of floating strips. (See table 2). This gain is somewhat offset by the reduced charged collection efficiency as the number of strips increases. It should also be noted that with increasing number of floating strips, the spread in the distribution of the charge read by each amplifier increases. As a result, although the noise is reduced by the smaller capacitance the signal distribution also spreads to lower values when additional strips are introduced.

Figures 3(a) show the plot of the expected charge distribution along with the positions of the 3σ, 4σ, and 5σ noise cuts indicated for 2 floating strips between readout strips (Option B4). Figures 3(b), (c) and (d) are plots of [rϕ(reconstructed)-rϕ(actual)] for the configuration B4 for the three threshold settings. Figure 4 shows the corresponding plots for Option B5, with 3 floating strips between readout strips.

As before, a narrow central peak can be seen in the resolution distribution with a width corresponding to the strip pitch. As the threshold increases, tails on either side of this distribution out to limits defined by the amplifier pitch emerge. The steps in these tails are due to the quantised nature of the collected charge with a finite number of floating strips.

Table 3 shows the position resolution (rms) obtained. Also listed is the fraction of events in the tails outside the region defined by the corresponding plot for Option A -- between ±50μm.

Layout Option	Number Floating Strips	Noise (electrons rms)	3σ noise threshold		4σ noise threshold		5σ noise threshold	
			rms(rϕ) (μm)	% in tails	rms(rϕ) (μm)	% in tails	rms(rϕ) (μm)	% in tails
A	0	1903	27.2	0.7	27.5	0.3	27.9	0.9
B1	1	1940	33.6	6.9	44.2	14.4	51.6	21.0
B4	2	1560	31.5	10.6	42.1	24.0	50.0	36.2
B5	3	1398	31.7	14.0	39.4	22.9	46.2	30.9

Table 3. Comparison with different numbers of floating strips between readout strips.

Figure 5 shows a summary of the resolution obtained for the options listed in table 3.

These results indicate that although, in principle, charge division has intrinsically improved position resolution, there are significant tails in the resolution distribution which are sensitive to threshold settings (and threshold drift). This result is true for Option B with either 1, 2 or 3 floating strips. With increasing number of floating strips the transition from the central region to the tail region becomes smoother.

3.1.2 Effect of the Ratio C_i/C_d

Another parameter which can be changed in this analysis is the ratio of the interstrip capacitance, C_i, to the element backplane capacitance, C_d . This ratio is typically 5-10 in current detectors, but as will be seen lower values are preferred here. Lower values result in an improved load capacitance and therefore reduced noise but they also produce lower charge collection efficiencies (See Appendix).

Figures 6 and 7 show charge distributions and position resolution plots for ratio C_i/C_d having values 3.5 and 2. Table 4 provides a comparison of the data for the three values of C_i/C_d = 5, 3.5, and 2 (Options B1, B2 and B3, respectively) together with the data for Option A. For comparison, a summary of the different resolutions is plotted in figure 8.

Layout Option	C_i/C_d	Noise (electrons rms)	3σ noise threshold		4σ noise threshold		5σ noise threshold	
			rms(rϕ) (μm)	% in tails	rms(rϕ) (μm)	% in tails	rms(rϕ) (μm)	% in tails
A	0.85	1903	27.2	0.7	27.5	0.3	27.9	0.9
B1	5	1940	33.6	6.9	44.2	14.4	51.5	20.8
B2	3.5	1753	32.0	5.7	40.1	11.2	49.9	19.3
B3	2	1546	31.0	5.1	38.0	9.6	48.5	18.0

Table 4. Comparison with different values of C_i/C_d

3.1.3 Nearest Neighbour Cluster Logic

It is apparent from the above that when charge sharing is applied, the broadening of the charge collected, together with the high discrimination level required, results in signal loss which degrades the position resolution.

The charge spreading is inherent in the method. Figure 9(a), shows a plot of the charge signal distribution for a modified version of Option B5 with no noise added to the signal (but with the same discriminator setting as necessary with noise). The peaks in the charge distribution correspond to charge collection from the various strips from one readout channel to the next. Figure 9(b-d) show the position resolution obtained with 3σ, 4σ and 5σ threshold cuts. The tails in the distribution remain.

The use of a global discrimination level directly results in the charge signal losses. It has been suggested that logic could be provided in the frontend readout, where nearest neighbours to hits passing a general threshold are also readout, independent of the signal magnitude on these nearest neighbour channels. These data would then be available to improve the position determination "offline".

Such a scheme was tested with the monte carlo simulation. If the maximum signal in any event was above the 4σ cut the event was passed and the maximum signal together with its two nearest neighbours were read out. (In practically all events the largest pulse height was a "real" signal.) The position determination was then made with both of two simple algorithms.

In the first, the signal weighted mean position of the maximum pulse together with both nearest neighbours was determined ("3-ch clustering"). In the second method the signal weighted mean position of the maximum signal with the nearest neighbour with the largest pulse height, was determined ("2-ch clustering").

Figure 11(c) shows position resolution plots for Option A with the simple global discrimination level (a 4σ cut was applied in this figure). In figure 11(d-f) the Option B1 resolution is presented with the three position reconstruction methods applied: the global 4σ cut, and the 3-ch and 2-ch clustering, respectively. Figure 12 shows the corresponding plots for the Option B5. Table 5 gives a summary of the data for all Options studied. The 4σ results are plotted in figures 13 and 14.

Option	3σ				4σ				5σ			
	ε_{clust} (%)	σ(μm) Glob. Thr.	σ(μm) 3-ch Clus.	σ(μm) 2-ch Clus	ε_{clust} (%)	σ(μm) Glob. Thr.	σ(μm) 3-ch Clus.	σ(μm) 2-ch Clus	ε_{clust} (%)	σ(μm) Glob. Thr.	σ(μm) 3-ch Clus.	σ(μm) 2-ch Clus
A	100.0	27.2	-	-	100.0	27.5	-	-	100.0	27.9	-	-
B1	100.0	33.6	39.2	31.5	98.2	44.2	38.9	31.4	89.2	51.6	38.0	31.4
B2	100.0	32.0	37.7	30.9	99.1	40.1	37.5	30.9	93.1	49.9	36.9	31.0
B3	100.0	31.0	36.4	30.4	99.5	38.0	36.3	30.4	95.0	48.5	35.9	30.5
B4	100.0	31.5	30.0	23.2	100.0	42.1	30.0	23.2	99.3	50.0	29.9	23.2
B5	100.0	31.7	27.5	21.9	99.5	39.4	27.2	21.5	97.0	46.2	26.8	21.5

Table 5. Comparison of position resolution and cluster finding efficiency for the various methods described in the text.

Of note in this summary is that the 2-ch clustering offers the best resolution. This is as expected. The data studied correspond to straight tracks and in all events produced "real" hits occur in at most two readout channels. The largest signal of the neighbour to the event maximum was almost always the second "real" signal of the event. In a real experiment, there will be a mixture of data with a variety of hit multiplicities, due to track curvature, delta rays, bremsstrahlung, etc. It will not in general be possible to restrict the inclusion of only the largest of the nearest neighbour signals when determining the position of a cluster.

It is therefore expected that the attainable resolution will be between the 3-ch and 2-ch clustering results.

In table 5 is also listed the efficiency for finding the maximum signal above the 4σ cut. Even with the use nearest neighbour logic, clusters will only be readout out if the maximum of the cluster is well above the noise level. The losses due to this cut are typically a few percent for the data shown.

3.1.5 Relation Between Detector Geometry and Interstrip Capacitance

As discussed in the Appendix, an experimental relation exists between the total strip capacitance and the ratio of strip width to strip pitch[4-8]. for 300μm thick detectors this is:

$$C_{total} = 0.8 * 1.4 \times (\text{width/pitch})$$

A simple model was applied which is valid for relatively small values of interstrip capacitance, where only nearest neighbours need be included in the calculation of the total capacitance. In this model, a consistent picture of capacitances can be obtained. It is found that the range of possible values of the ratio Ci/Cd is limited and dependent on the strip pitch required. In the above results the values of Ci/Cd and the number of strips were chosen independently in order to highlight the effect of changing these parameters. In view of the relationship between these parameters, results have also been obtained with the dependencies explicitly included.

By specifying the ratio, (strip width/strip pitch), and the strip pitch, together with the relations obtained in above considerations, results on the position resolution were obtained and are presented in figures 15 and 16.

As can be seen from figure 15 the larger strip widths at the smaller pitch result in the best resolution. It appears in figure 16 that the position resolution improves going from one intermediate strip to two, but this improvement saturates. The resolution obtained with a constant ratio of width/pitch for three intermediate strips is not significantly better than that obtained for the same ratio with only two intermediate strips. This is a product of the noise limited measurements which do not allow the full potential of the charge division readout to be achieved.

3.1.4 Investigation of A Suggested Detector Layout

In the course of this analysis, a specific suggestion was made to the Inner Detector Review Panel for a detector layout [9]. Capacitive charge division in detectors with readout pitch of 100μm and 200μm was suggested, as listed in table 6.

These layouts were analysed and compared with the corresponding options where all strips are readout, with half the readout pitch but with twice the strip length (Option A, D). The values for C_i/C_d were extracted from the values of C_{is} quoted in [9].

Option	Strip Length (cm)	Readout Pitch (μm)	Strip Pitch (μm)	Ratio C_i/C_d	Charge Coll. Effic. (%)	C_{load} (pF)	Noise (electrons RMS)
A	12	100	100	0.85	93.2	13.1	1903
C1	6	200	100	0.85	67.6	6.4	1066
C2	6	200	50	1.71	51.6	4.9	953
D	12	50	50	2.2	85.0	13.3	1892
E	6	100	50	2.86	69.9	6.3	1044

Table 6. Charge division layouts of [9] compared with corresponding "Option A" designs

In comparing the suggested layouts with the corresponding options with no charge division (Options A, D), the more optimistic amplifier noise of (600 + 65 pF^{-1})electrons was assumed for Options C and E. The same (equivalent) shaping time of 25nsec was assumed for these options in calculating the shot noise, together with a ballistic deficit of 0.9 [9].

Figure 17(a) shows the charge distribution of all signals above 2000 electrons in Option C1. The vertical lines correspond to the 3σ, 4σ and 5σ noise cuts. Figure 17(b) shows the distribution of the maximum charge value found. The 3σ, 4σ and 5σ cuts are shown to give an indication of the inefficiency in finding clusters, produced by the application of the cuts. In the case of figure 17(a), the cuts shown produce the observed resolution broadening described in sections 3.1.1 and 3.1.2. In figure 17(b) the cuts indicate the loss of events expected.

Figure 18 show the similar plots for Option C2.

In figure 19 is presented a comparison of the position resolution obtained for the various position determination methods applied to option A and C1. Figure 19(d),(e) and (f) show the resolution distribution for the simple 4σ global threshold cut, the 3-ch and 2-ch clustering methods respectively. Figure 19(c) shows the results of Option A with the simple threshold cut applied, for comparison.

Figure 20 provides the same comparison for Option C2.

Table 7 provides a summary of the results from these comparison. Results for 3σ, 4σ and 5σ cuts are provided. In the case of the global threshold requirement, this is the level applied to all channels. In the simulation of the nearest neighbour logic, these cuts apply to the search for the maximum signal in the event.

Option	3σ				4σ				5σ			
	ε_{clust} (%)	σ(μm) Glob. Thr.	σ(μm) 3-ch Clus.	σ(μm) 2-ch Clus	ε_{clust} (%)	σ(μm) Glob. Thr.	σ(μm) 3-ch Clus.	σ(μm) 2-ch Clus	ε_{clust} (%)	σ(μm) Glob. Thr.	σ(μm) 3-ch Clus.	σ(μm) 2-ch Clus
A	100.0	27.2	-	-	100.0	27.5	-	-	100.0	27.9	-	-
C1	100.0	30.5	34.9	29.9	99.7	36.3	34.9	29.8	96.1	46.9	34.9	29.8
C2	99.7	39.8	31.6	27.4	97.0	47.2	31.1	27.3	90.0	48.1	29.8	27.6

Table 7. Comparison of position resolution and cluster finding efficiency for Options C1 and C2. Data for Option A is provided for ease of comparison.

It has been suggested that a 100μm readout pitch, 50μm strip pitch layout (Option E, in table 5) might be suitable for smaller radii in the inner detector. To study this geometry, the additional radiation fluence expected at a radius of 30cm was applied. The calculated equivalent fluence over the ten year scenario described above is $1.0 \times 10^{14} n.cm^{-2}$.

Figure 21 shows a comparison of Option E and Option D, similar to those present in figures 19 and 20. More detailed results are provided in table 8. Comparison of Options D and E show results with a similar pattern to that observed above. The basic resolution of the charge division option is similar to that without charge division. Small tails are seen in the charge division option.

Option	3σ				4σ				5σ			
	ε_{clust} (%)	σ(μm) Glob. Thr.	σ(μm) 3-ch Clus.	σ(μm) 2-ch Clus	ε_{clust} (%)	σ(μm) Glob. Thr.	σ(μm) 3-ch Clus.	σ(μm) 2-ch Clus	ε_{clust} (%)	σ(μm) Glob. Thr.	σ(μm) 3-ch Clus.	σ(μm) 2-ch Clus
D	100.0	13.2	-	-	100.0	13.4	-	-	100.0	13.7	-	-
E	100.0	13.7	15.3	13.6	100.0	14.0	15.3	13.6	100.0	14.8	15.3	13.6

Table 8. Comparison of position resolution and cluster finding efficiency for Options E and D

4. Summary

Option A, with the coupling of readout channels to all strips, sets the standard by which charge division results can be judged. It provides the most robust configuration against gain variation and threshold settings. The drawback with this option is the need to double the strip length to maintain the same readout channel density as the charge division options considered. The resolution in r-ϕ is limited to ($1/\sqrt{12}$) x readout pitch.

The interstrip capacitance in this configuration has a larger effect on the load capacitance as this capacitance is direct from each strip to the ground of the neighbour channel. However, the use of a readout channel on each strip is far more robust against noise than is the charge division readout. Even with less optimistic assumptions about the expected noise, and conservative choices of Ci/Cd for this option, the resolution obtained changed little with variations in the parameters.

Option B with capacitive charge division readout can, in principle, attain equivalent or better resolution than Option A, depending on the geometry chosen. The major limitation in achieving this improvement is the noise expected for LHC optimised electronics.

Under realistic assumptions about the noise expected, the conservative requirement of a global 4 σ noise threshold cut results in significant tails in the resolution due to signals below threshold. The degradation results in larger RMS position resolution than in the corresponding "Option A layout".

To avoid this signal loss, nearest neighbour logic is required to collect data from channels adjacent to those passing the threshold, independent of the signal size on these neighbour channels. It is expected that in practice results between the "2-ch clustering" and "3-ch clustering" will be achievable.

The suggested layout [9] chooses a regime of low C_i/C_d, thus reducing the capacitive load, and hence reducing amplifier noise (at fixed preamplifier power consumption). However, this gain is countered by the increased signal spread. Applying a global 4σ noise cut results in significant signal loss, generating large tails in the position resolution. The clustering made possible by nearest neighbour logic achieves, at best, a resolution comparable with that obtained by a corresponding direct readout geometry. This is achieved at the expense of the additional complexity required on the frontend electronics and increased data rates.

It should be noted that the conclusions about these layouts (Options C1 and C2) are reached even with the more optimistic noise performance of the amplifiers assumed for these options.

Analysis of a range of parameters indicates that the optimum capacitive charge division readout geometry would be to use a 50μm or 66.7μm strip pitch in the 200μm readout pitch detectors with a strip width of 20μm. In this case, the calculations show that an improvement in position resolution over Option A of up to 20% is possible, although a somewhat smaller improvement is expected in practice, as discussed in this paper. This result has been shown to be sensitive to the parameters chosen and thus would not be considered a robust property of the method.

This modest potential gain must be weighed against the additional complexity in both the detector design and frontend electronics and readout. The increased cost and radiation sensitivity of AC coupled detectors must also be considered when evaluating the relative performance of the two methods studied.

In all options considered, the amplifier noise associated with the capacitive load dominated the shot noise due to the expected (average) radiation induced dark current.

5. Caveats

The following effects have not been considered in our study, and should be included:

a) ADC Granularity

No digitisation granularity has been included. This will deteriorate all options, but more seriously the charge division options where the signal dynamic range is greatest.

b) Comparator thresholds.

A fixed step-function threshold is assumed. Option B has increased sensitivity to the threshold shape and to channel-to-channel variations, but the quantitative effect is not known.

c) 2-particle resolution.

During high-luminosity operation, 0.5 tracks on average will traverse each phi-z counter. The problems of ambiguities are therefore significant. For minimum bias events, the probability of adjacent tracks is at 1% level for option A, 2-3% for option B. This number is substantially increased for electron tracks, and for jets etc. The quantitative effect is not known, for either option

d) Complete η Range.

The work described here calculated resolutions for η=0, with straight tracks. The angular coverage of the proposed layout should be explored fully. Also, lower momentum, curved tracks should be investigated.

References

[1] Previous transparencies on Capacitive Charge Division:

Phil Allport, "Silicon Resolution Issues", ATLAS ID Review Panel report, 16/11/1993.

Mike Tyndel, "SSM Scalable Silicon Module",BSP Meeting, CERN, 4/11/1993

[2] Progress Report on the RD2 Project, RD2 Collaboration, CERN/DRDC/93-18, 9/3/1993

[3] G.Gorfine and G.Taylor "Particle Fluxes and Damage to Silicon in the ATLAS Inner Detector", ATLAS Indet Note 030, November, 1993.

[4] Yamamoto, K., et al., Nucl. Instr. and Meth. **A326** (1993) 222-227.

[5] Barbaris, E., et al., Talk presented at Int'l Symp. on Dev't of Semiconductor Tracking Detectors, Horishima, Japan, May 22-24, 1993.

[6] Hall, G., et al., Nucl. Instr. and Meth., **A326** (1993) 228-233.

[7] Masciocchi, S., et al., IEEE Trans. Nucl. Sci., **40** (1993), 328.

[8] Kollipara, R., Private communication, February, 1993.

[9] P.Weilhammer, "Si Strip Detectors in the ATLAS ID with Capacitive Charge Division at High Luminosity", IDSC Meeting, CERN, 25/1/94

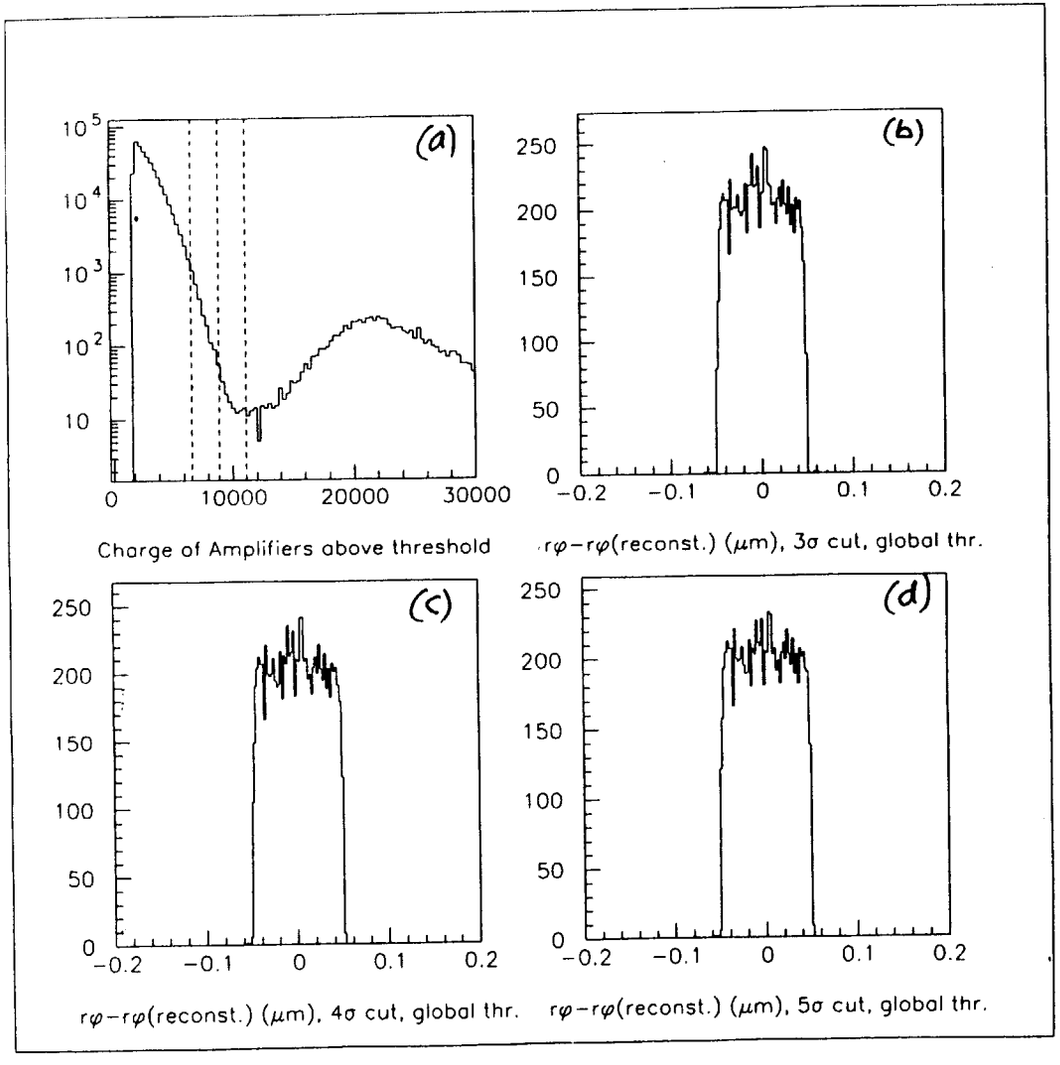

Figure 1: Option A, Global Threshold

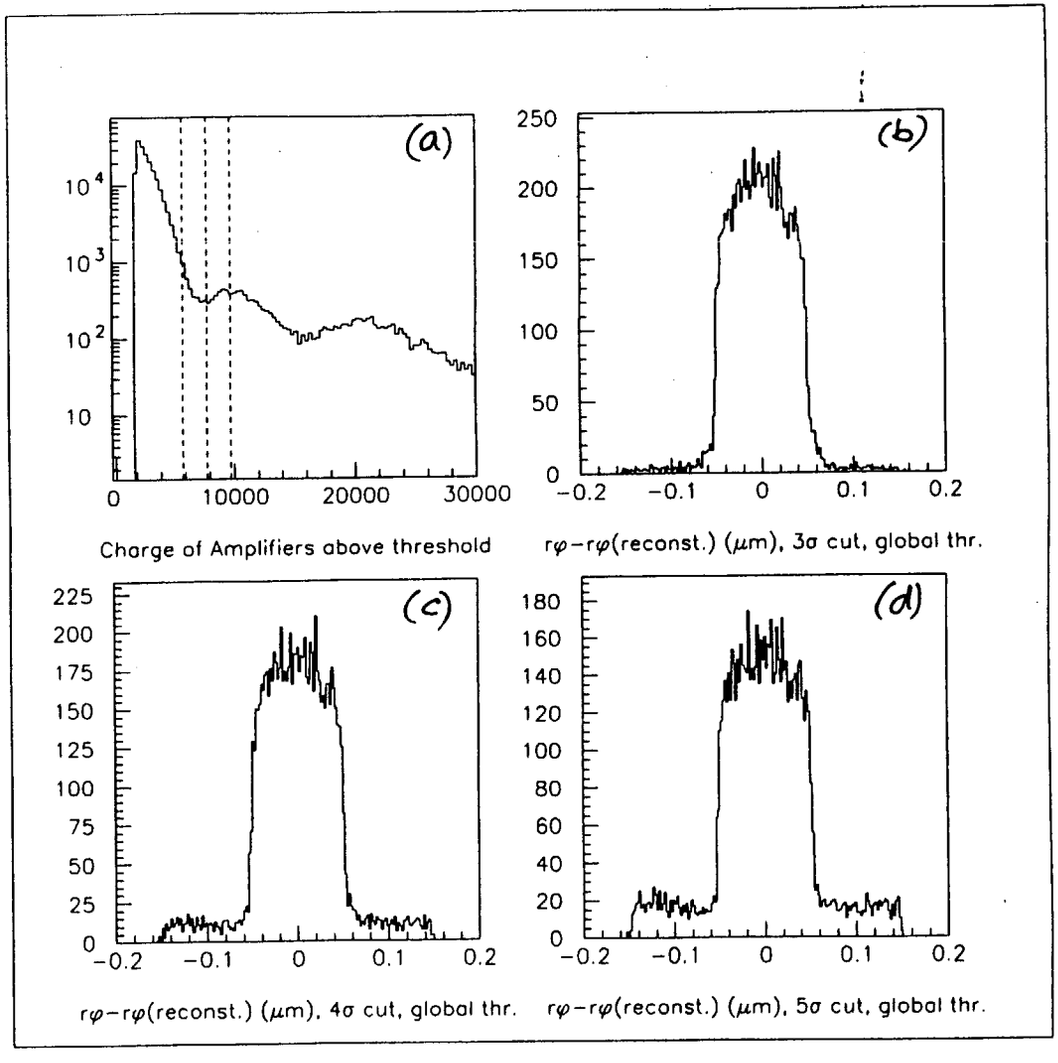

Figure 2. Option B1, Global Threshold

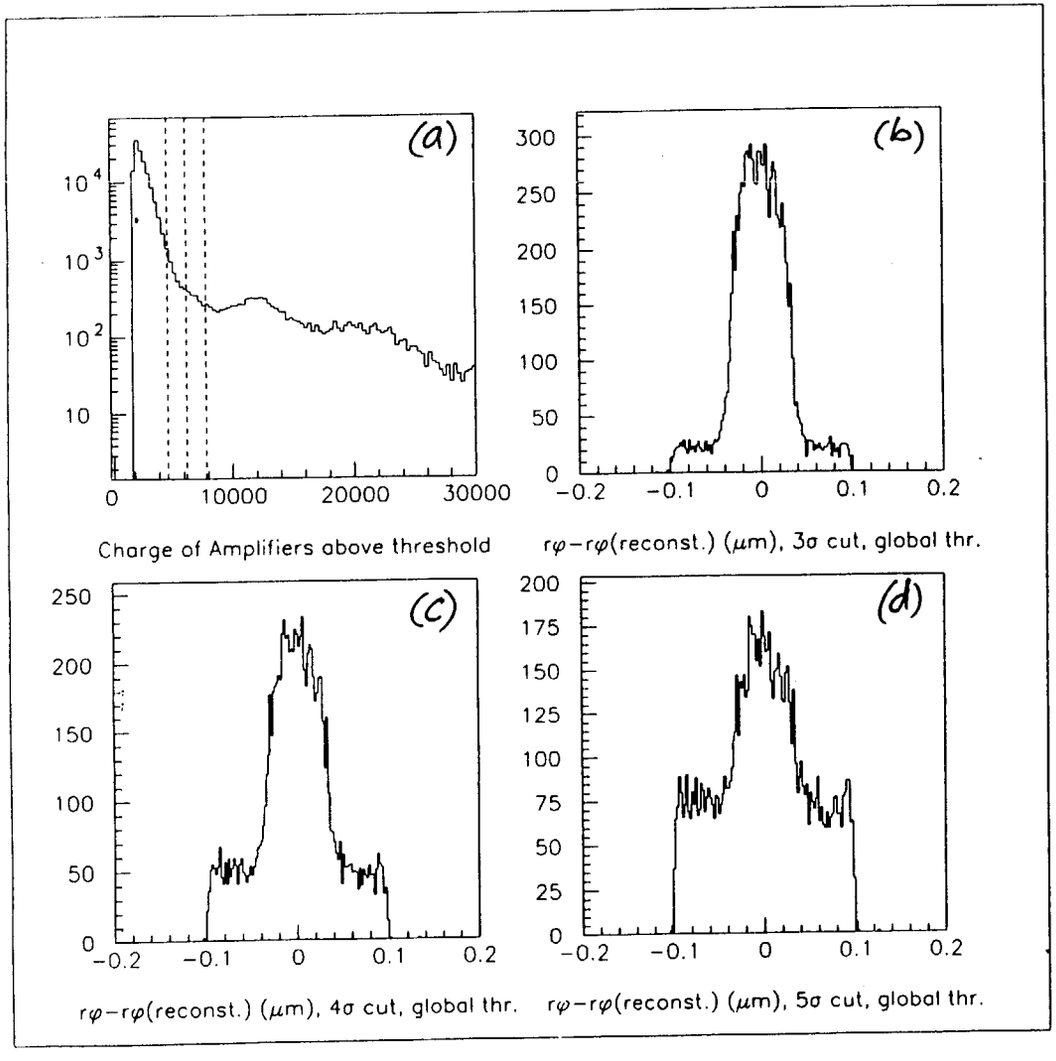

Figure 3. Option B4, Global Threshold

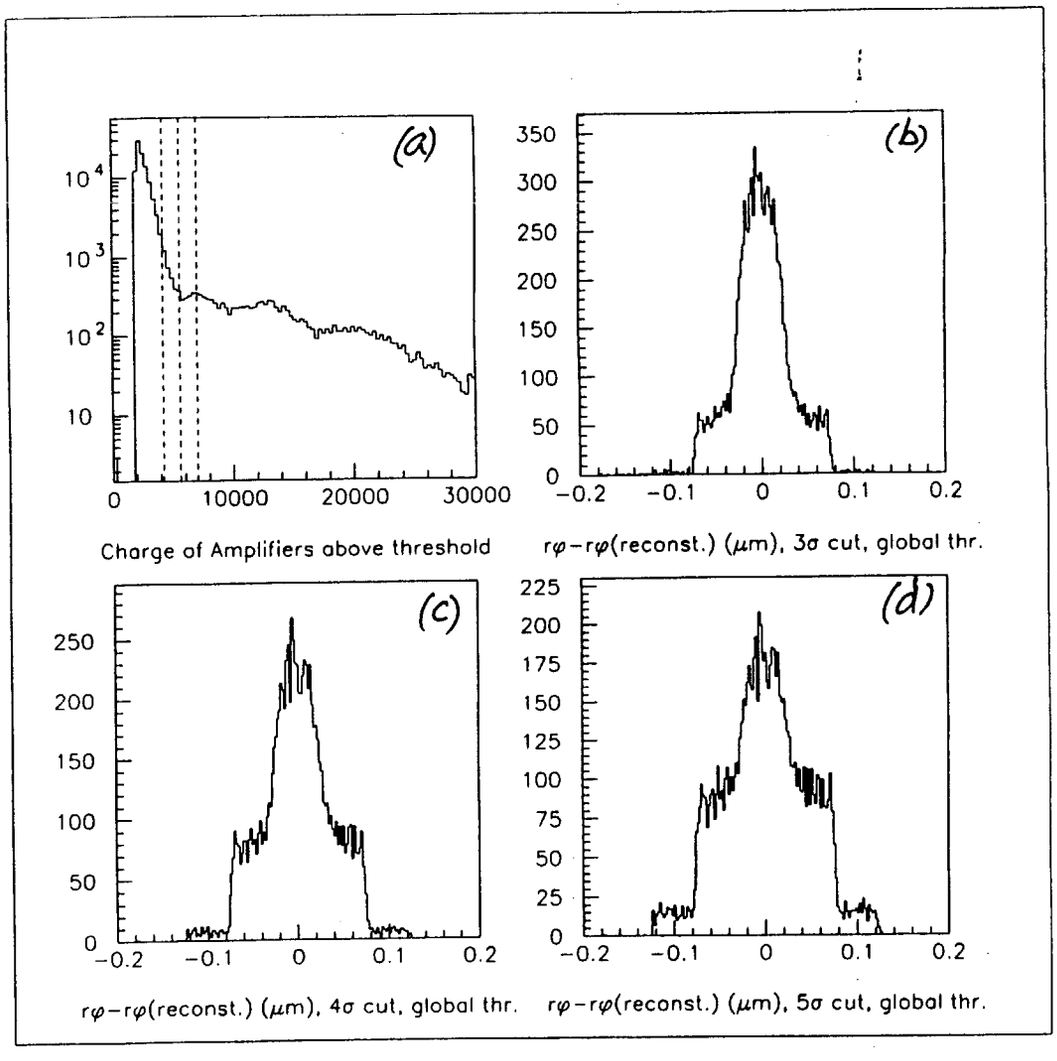

Figure 4. Option B5, Global Threshold

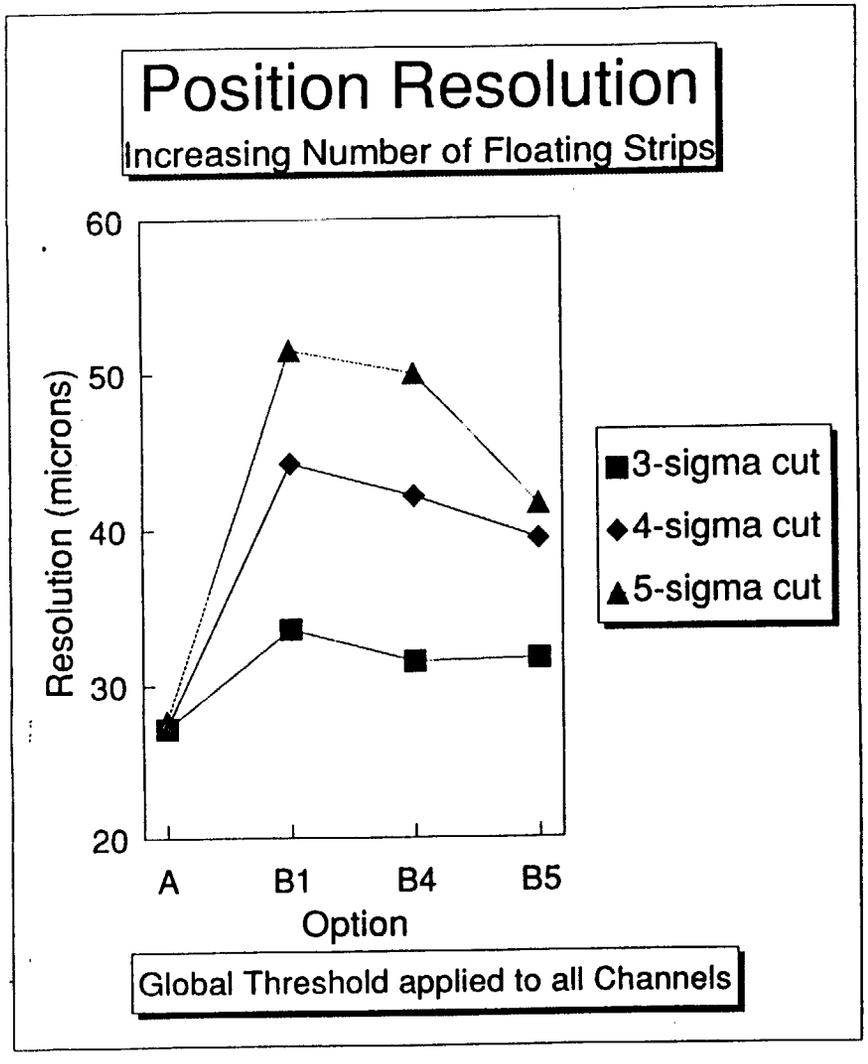

Figure 5. Summary of Resolution Obtained using Global Threshold. Comparison of geometries with different numbers of readout strips.

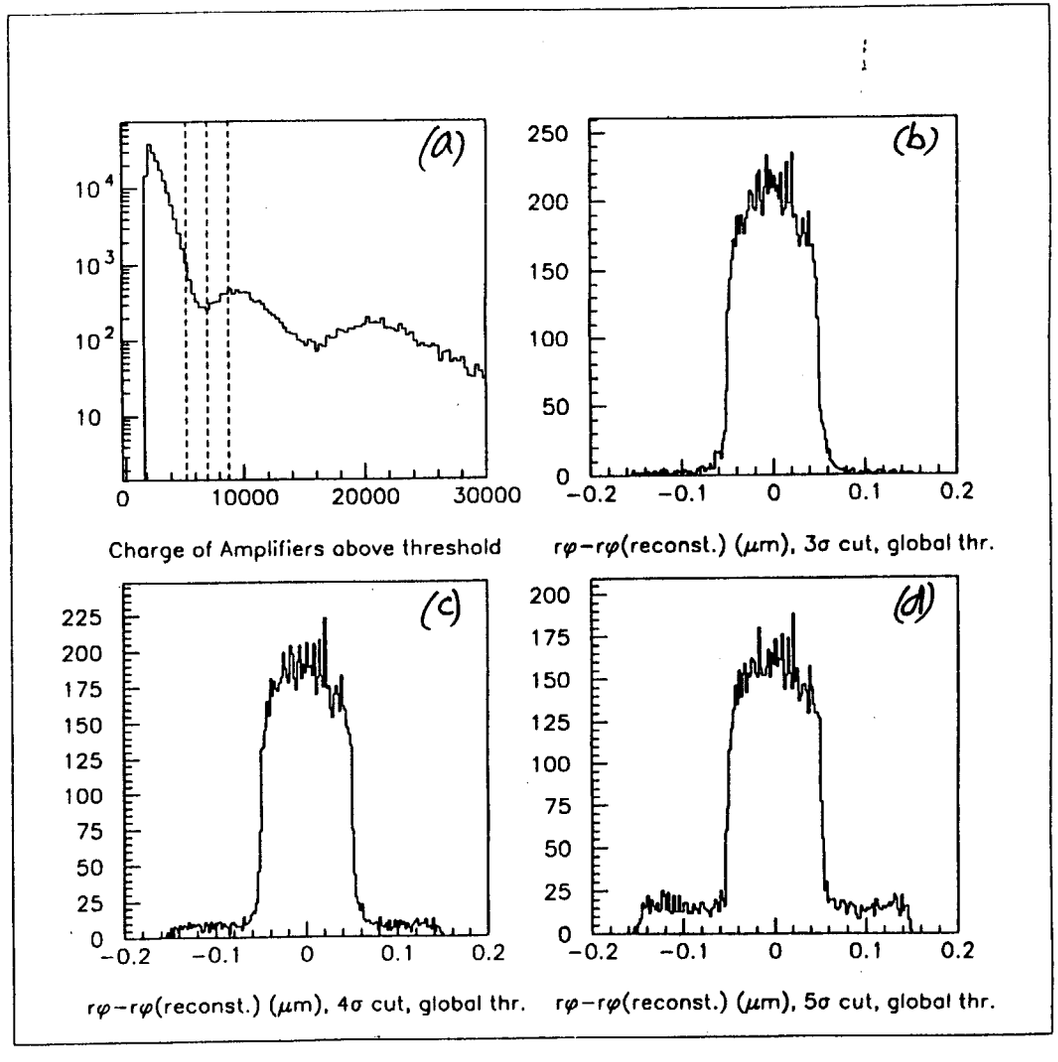

Figure 6. Option B2, Global Threshold

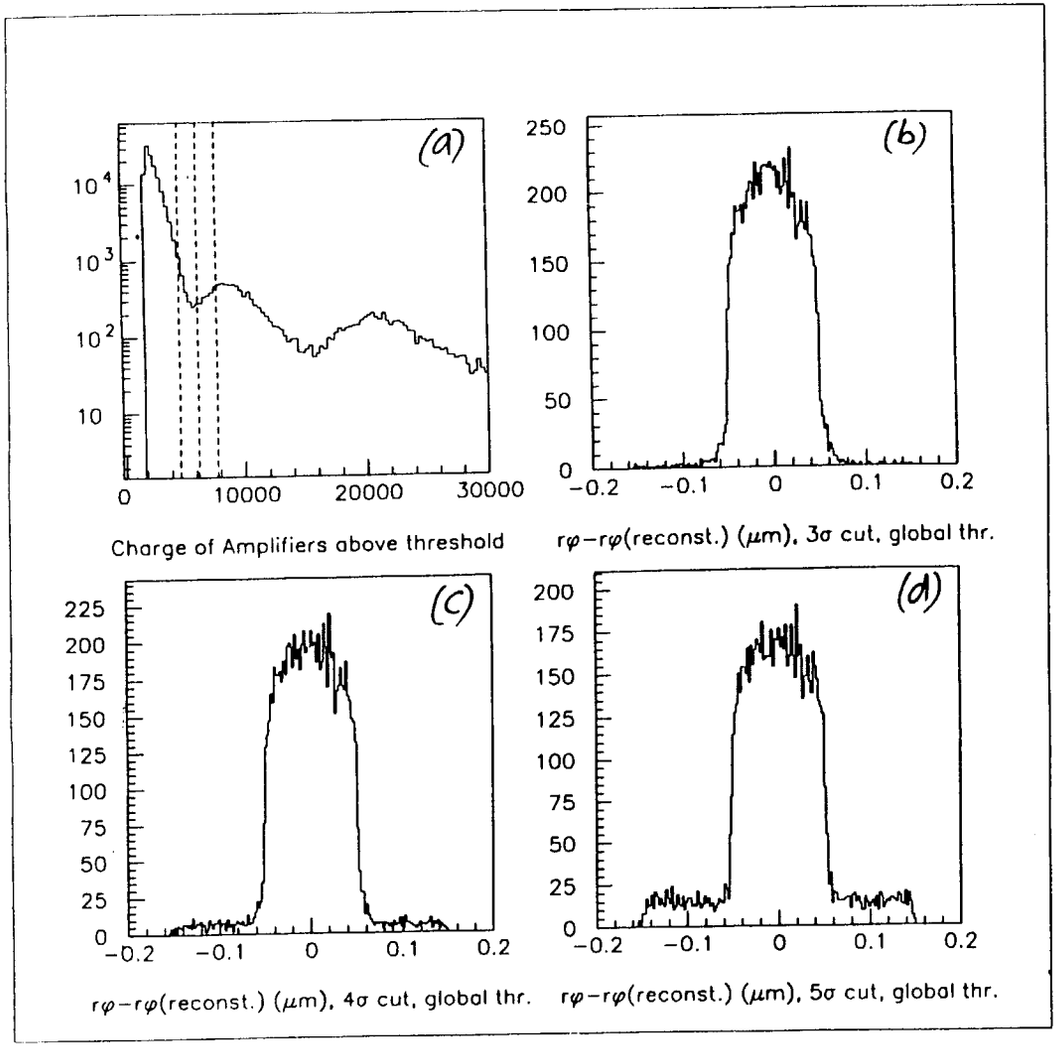

Figure 7. Option B3, Global Threshold

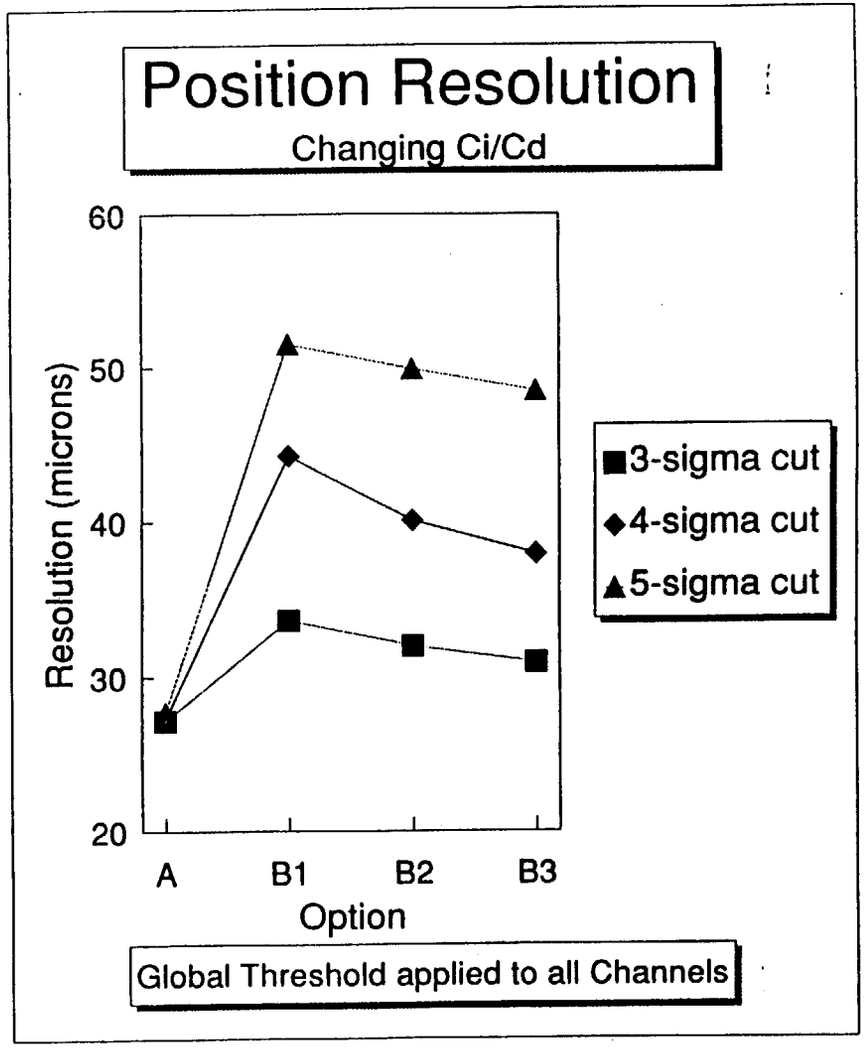

Figure 8. Summary of Resolution Obtained using Global Threshold. Comparison of geometries with different ratios Ci/Cd.

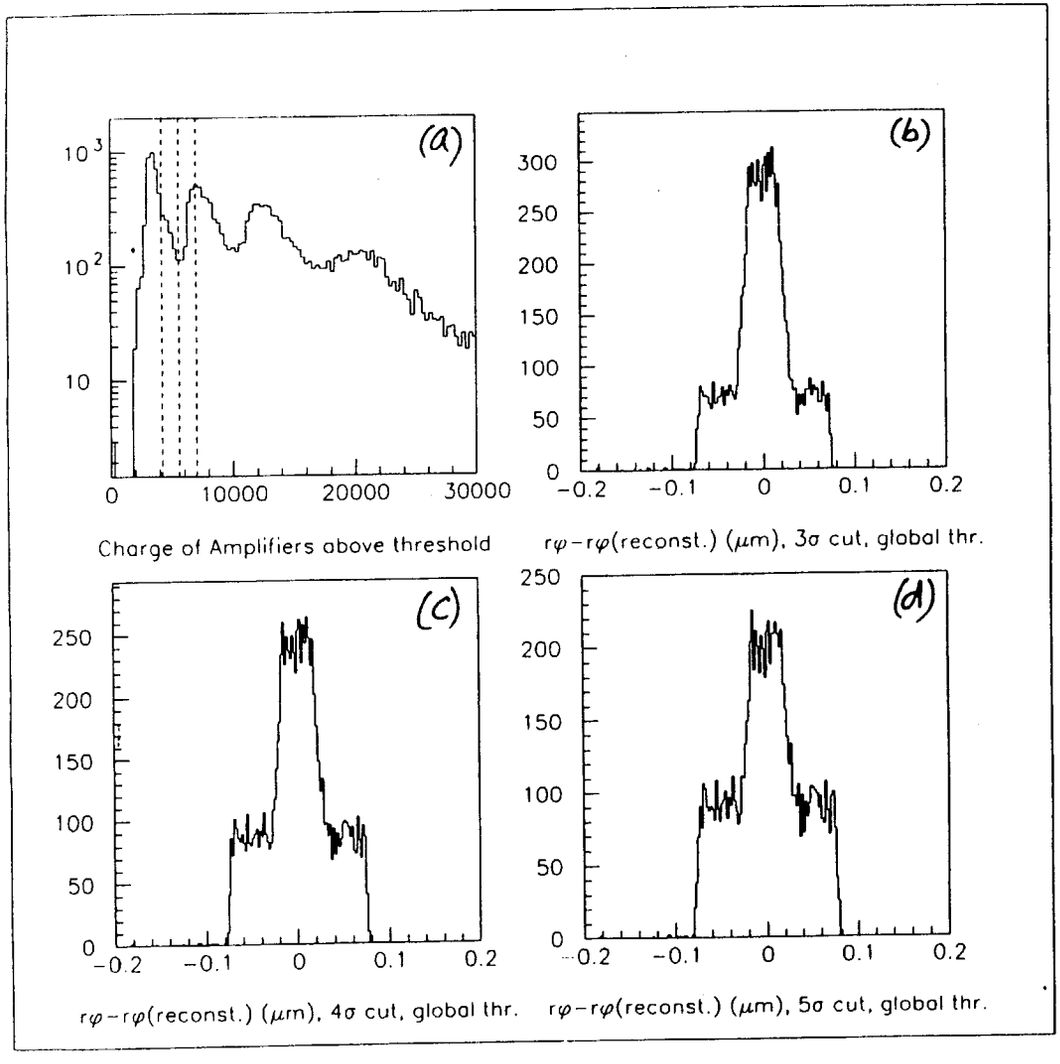

Figure 9. Option B5 with no noise added to amplifiers. Global threshold applied using σ from Option B5, with noise.

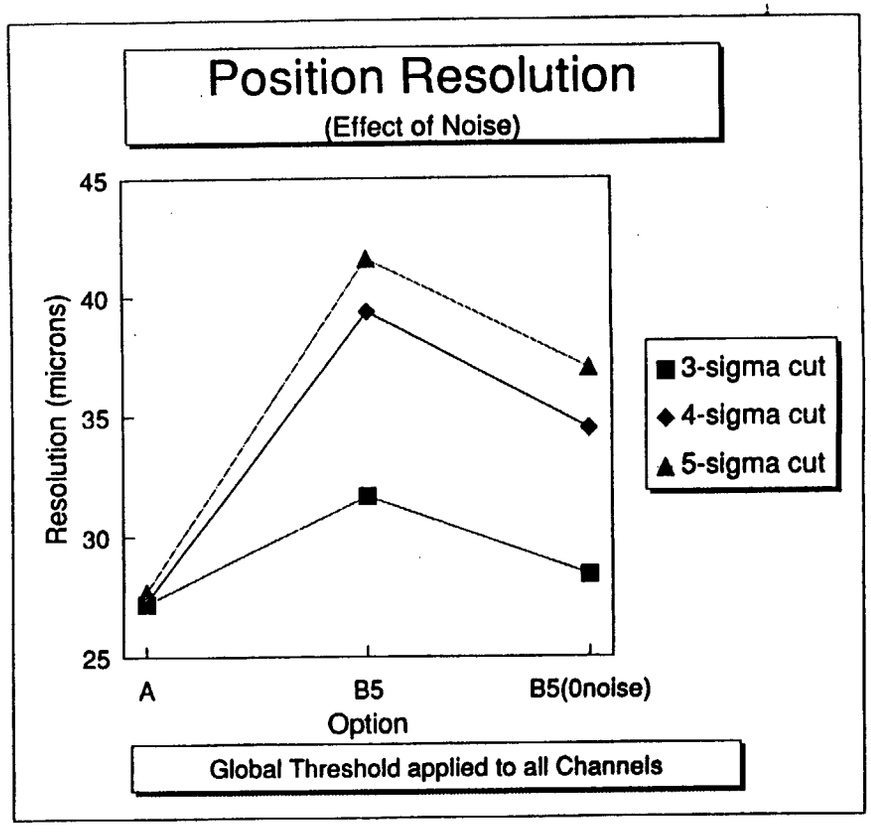

Figure 10. Comparison of resolutions obtained in Option 5, with and without noise added. (Using the same cuts in both cases.)

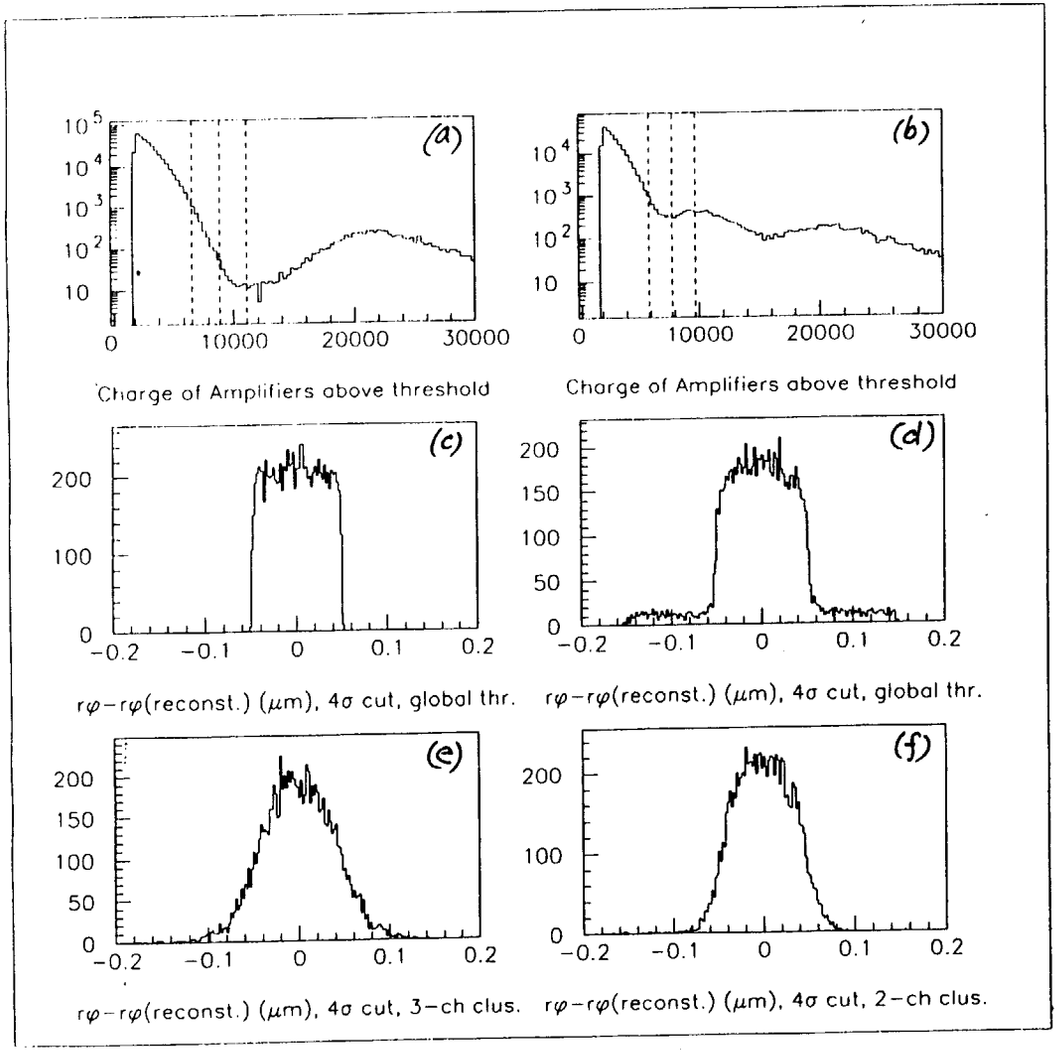

Figure 11. Comparison of resolutions obtained in Option B1 using different clustering metods, with that obtained for Option A.

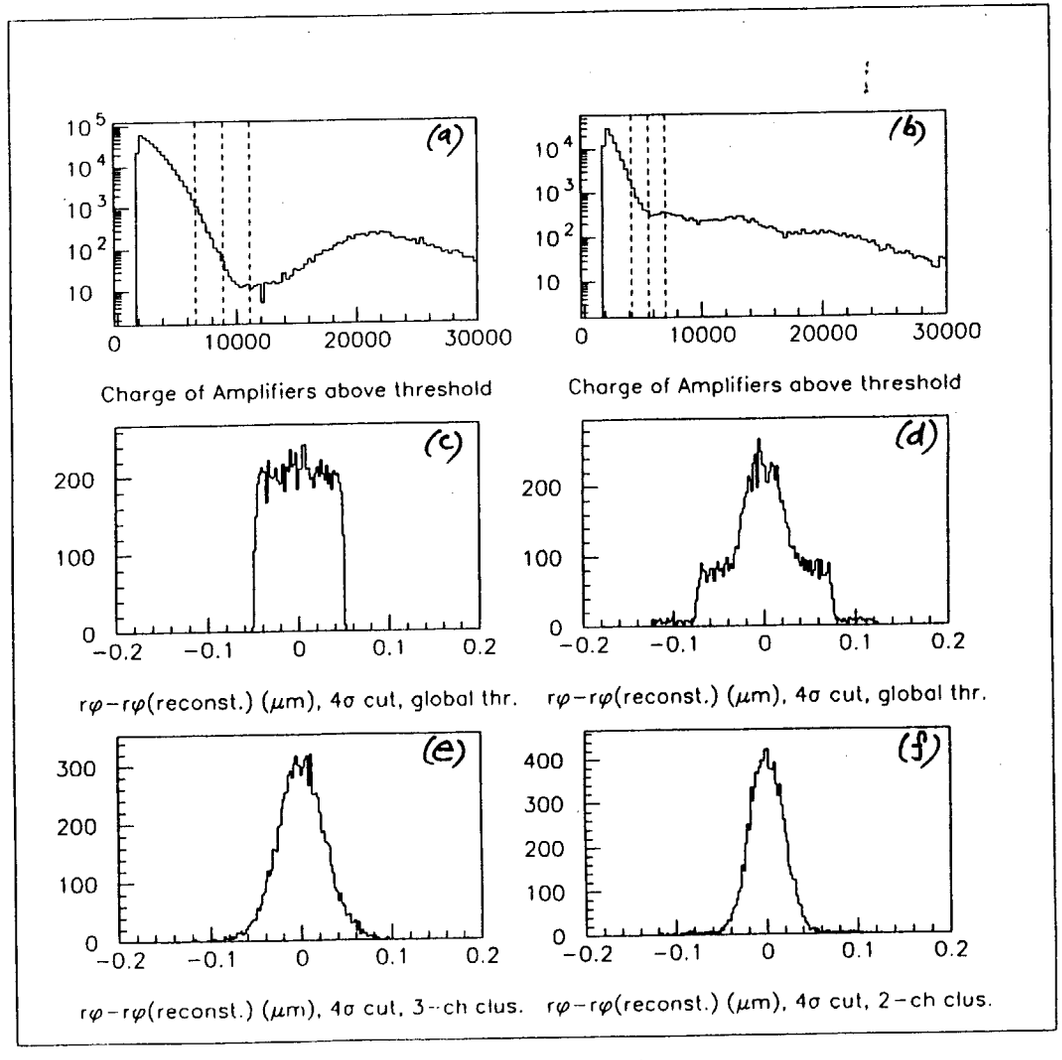

Figure 12. Comparison of resolutions obtained in Option B5 using different clustering metods, with that obtained for Option A.

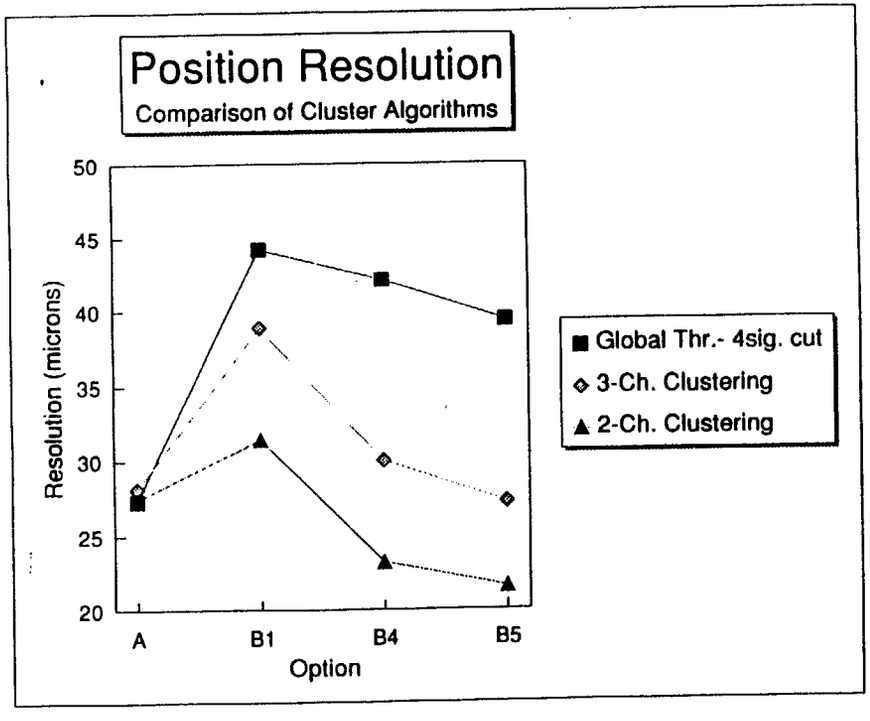

Figure 13. Summary of resolutions obtained with the various cluster algorithms, with 4-σ cut. Comparison of Option A with Options B1, B4 and B5

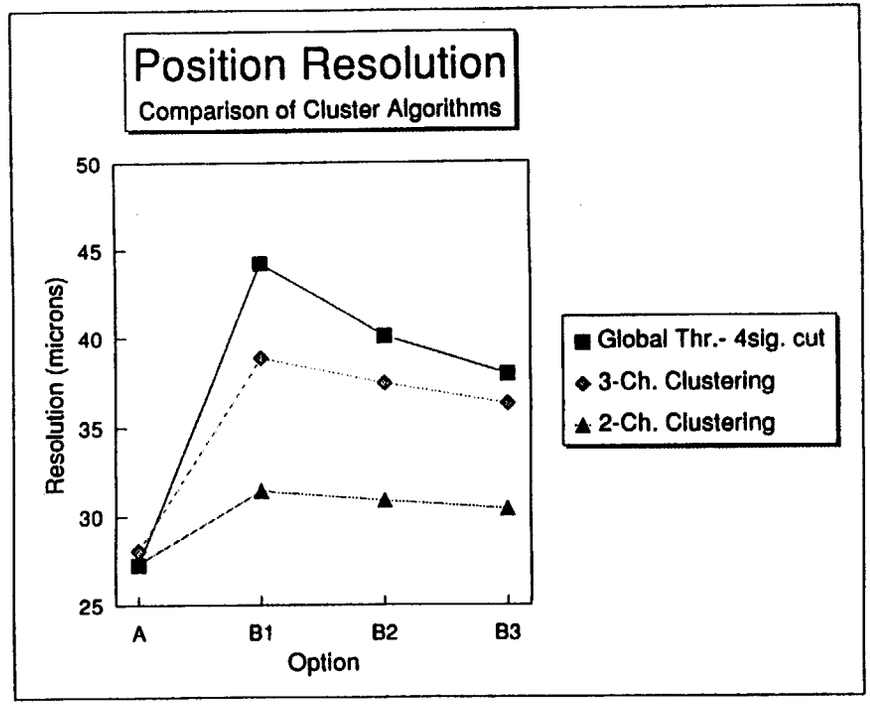

Figure 14. Summary of resolutions obtained with the various cluster algorithms, with 4-σ cut. Comparison of Option A with Options B1, B2 and B3.

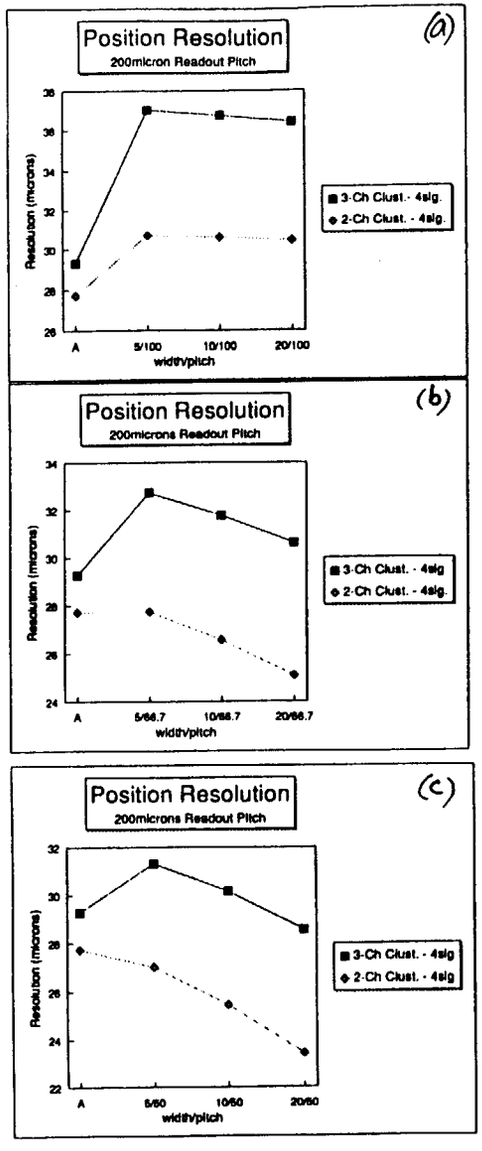

Figure 15. Resolutions obtained for various strip pitches and ratios (width/pitch) for 200μm readout pitch.

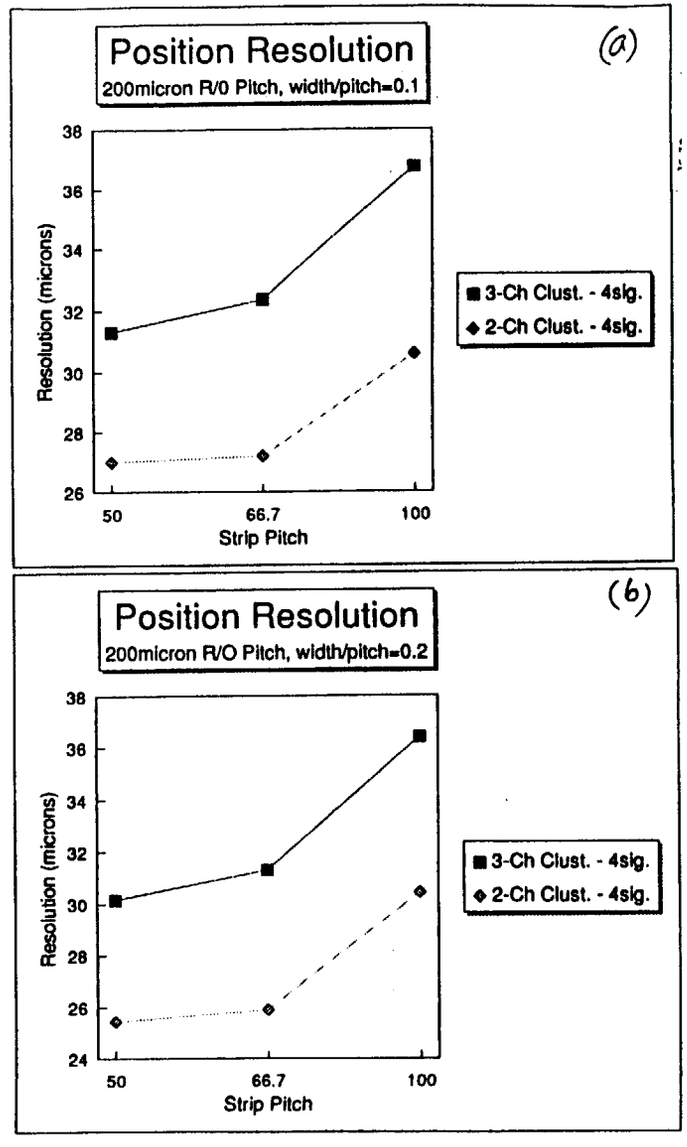

Figure 16. Resolutions obtained for various strip pitches with constant ratios (width/pitch). (200μm readout pitch is assumed.)

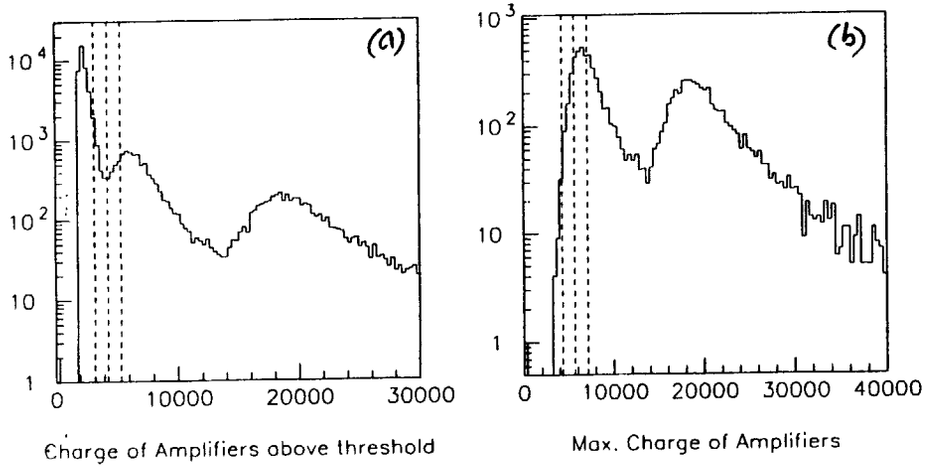

Figure 17. Individual amplifier charge distribution and maximum charge per track for Option C1. Vertical lines indicate 3σ, 4σ and 5σ cuts, respectively.

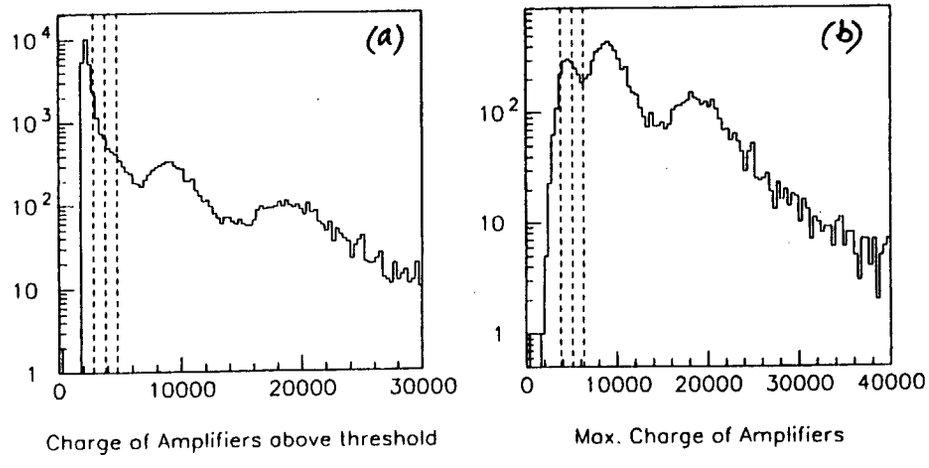

Figure 18. Individual amplifier charge distribution and maximum charge per track for Option C2. Vertical lines indicate 3σ, 4σ and 5σ cuts, respectively.

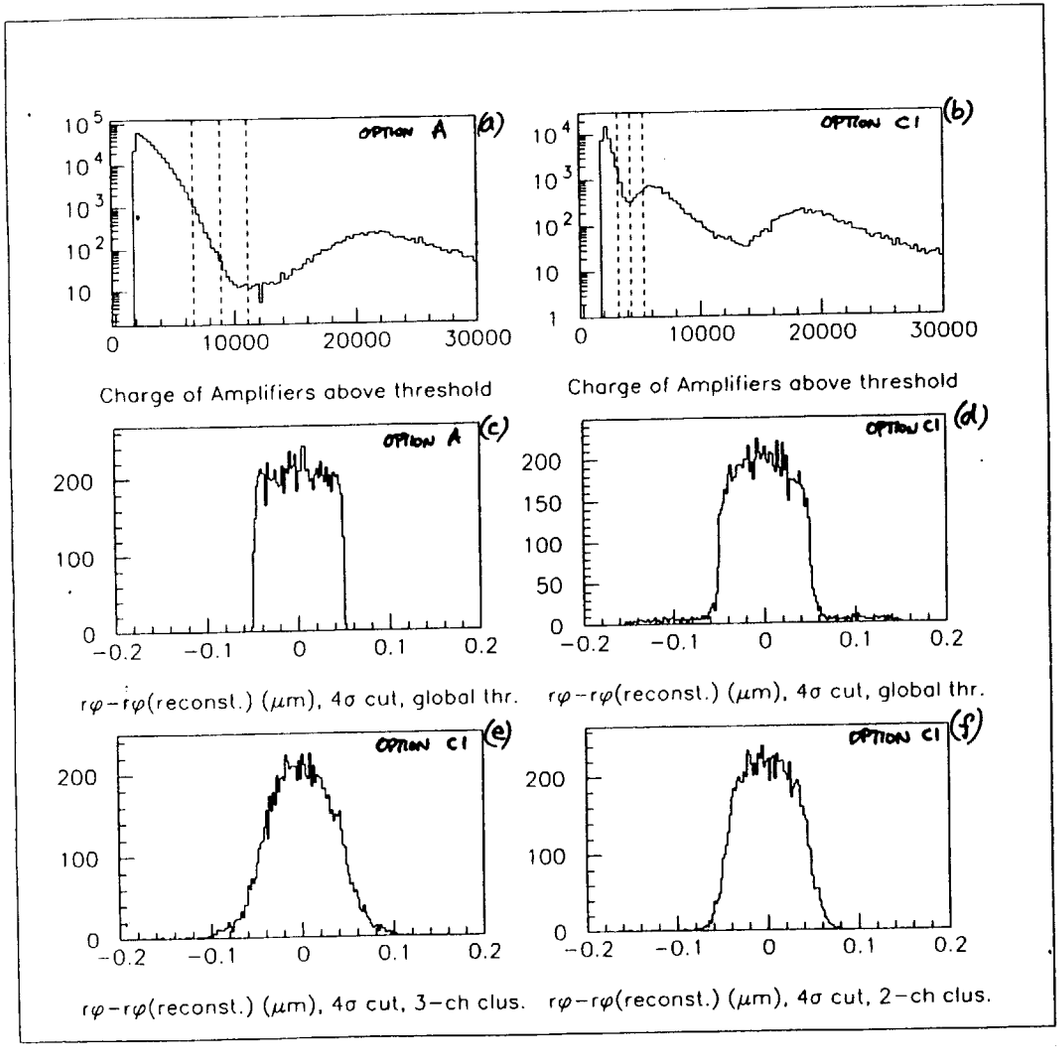

Figure 19. Comparison of resolutions obtained in Option C1 using different clustering metods, with that obtained for Option D.

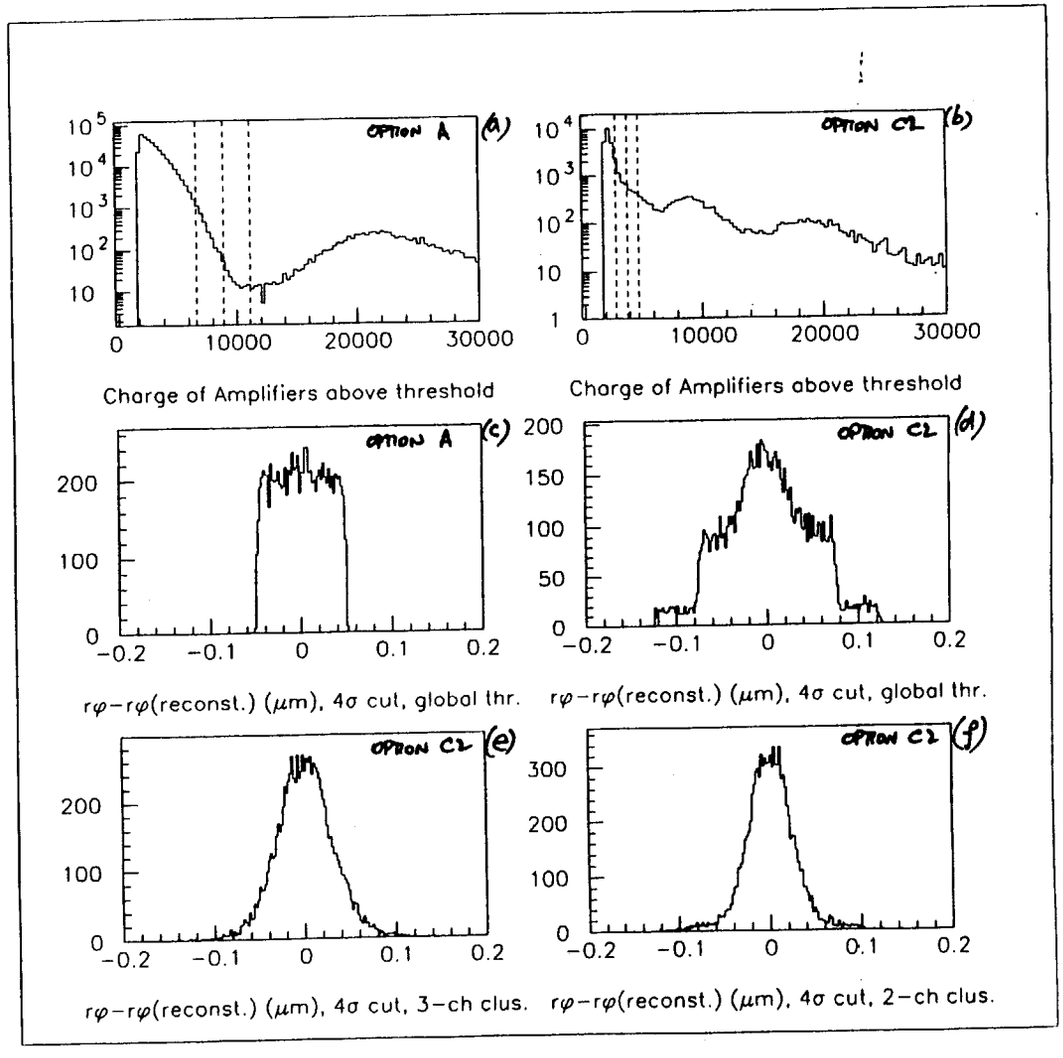

Figure 20. Comparison of resolutions obtained in Option C2 using different clustering metods, with that obtained for Option D.

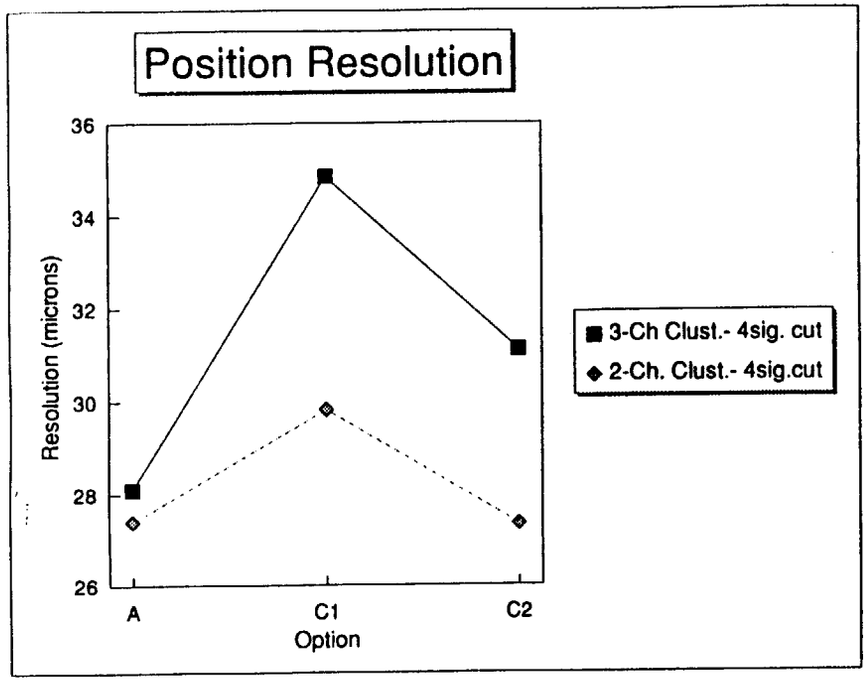

Figure 21.Summary of resolutions obatined with Options C1 and C2, in comparison with Option A, for various cluster algorithms and cuts.

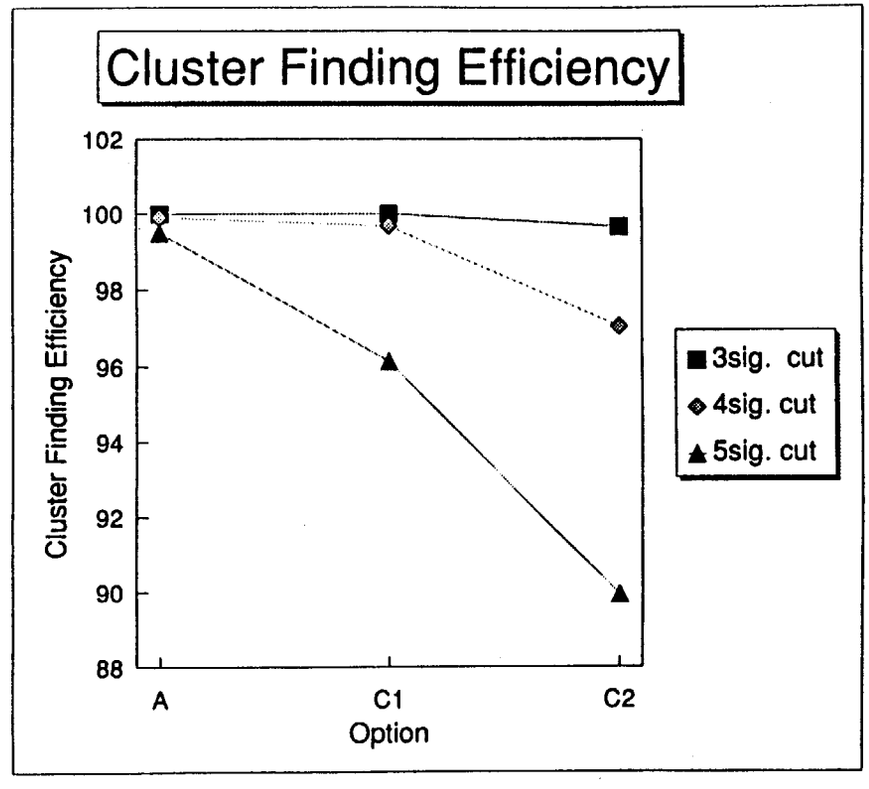

Figure 22. Efficiency for finding clusters using the different cluster algorithms. Comparison of Options C1 and C2 with Option A.

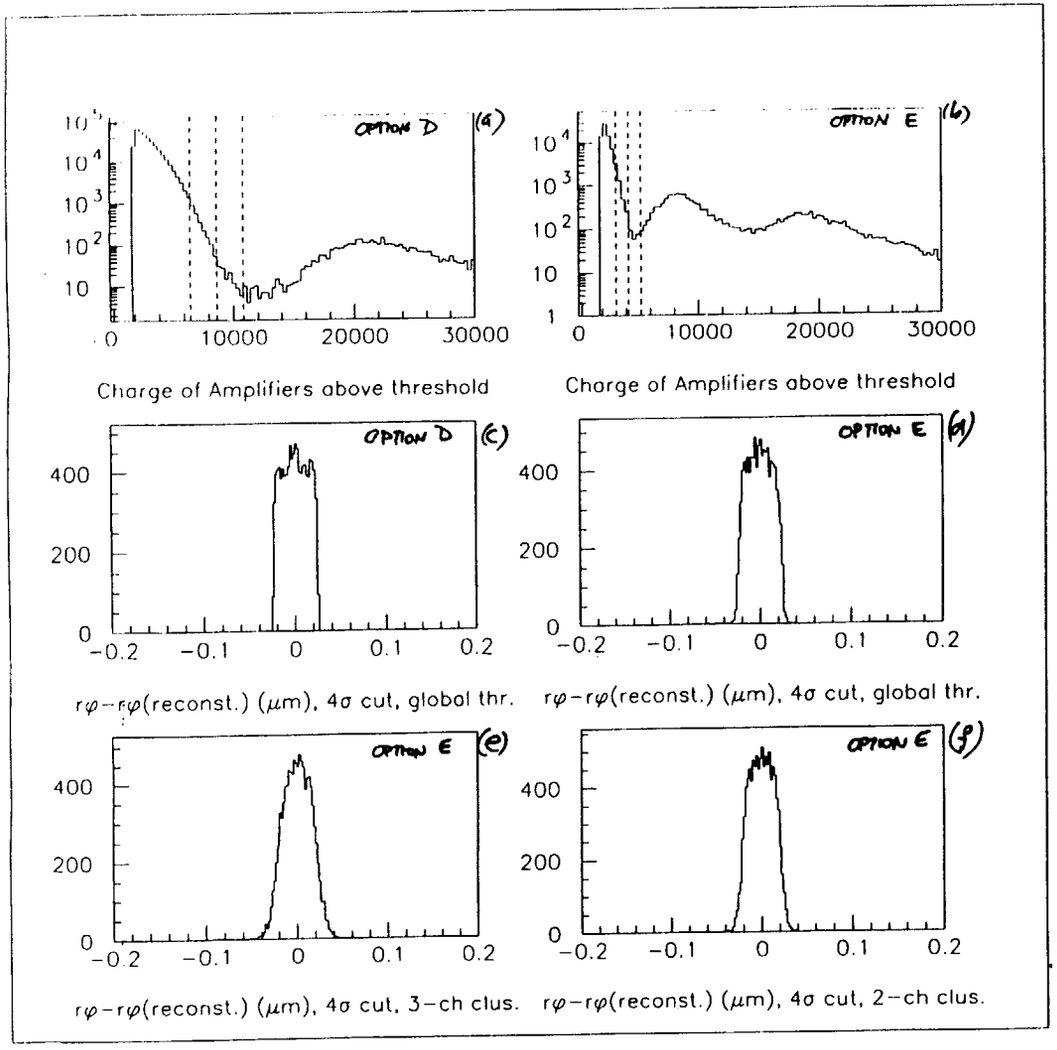

Figure 23. Resolutions obtained for Option E, using various cluster algorithms, with 4-σ cut. compared with Option D

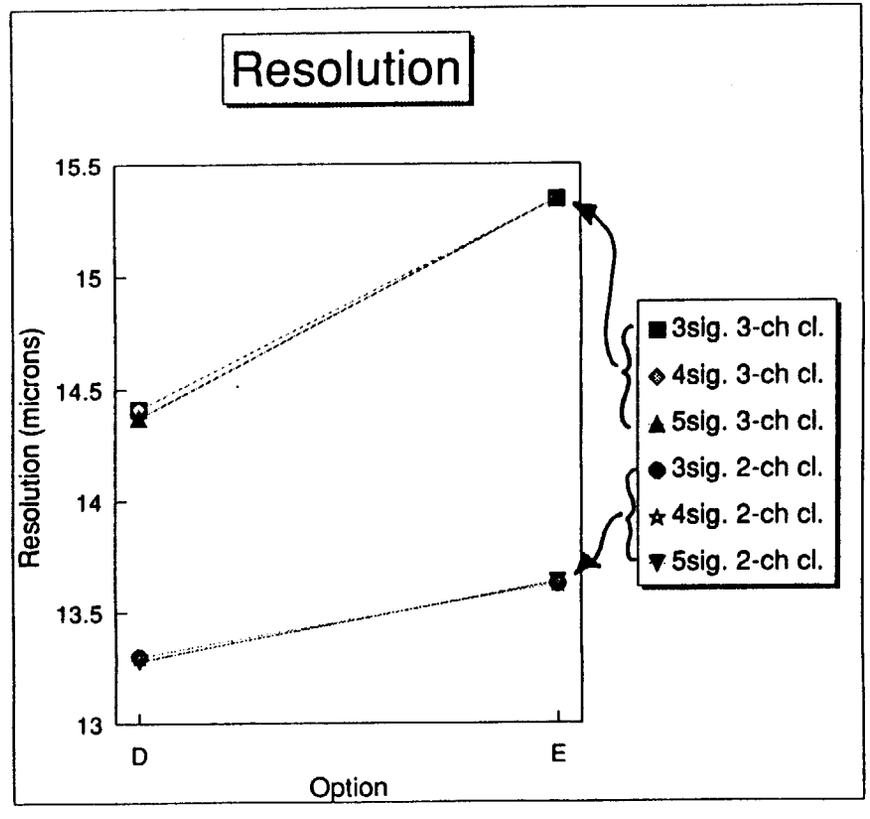

Figure 24. Summary of resolutions obtained from Options D and E.

Appendix:

Load Capacitance and Charge Collection Efficiency in Capacitive Charge Division Readout Applied to the ATLAS Inner Tracker Silicon Detectors

Introduction

Capacitive charge division in segmented silicon detectors has been used successfully in for over a decade[1]. This method maintains the single particle precision corresponding to the detector segmentation without the need to have a readout channel attached to each element. The result is a detector with fewer readout channels to instrument. To date these detectors are characterised by fine pitch, small detector element size with very low noise electronics. They have typically been used as vertex detectors which are by their very nature small in overall dimensions.

In the ATLAS Inner Detector the use of silicon detectors at radii as large as 105cm is being studied. With the large area of silicon thus required and the extremely large number of electronic readout channels, the use of capacitive charge sharing may produce savings in the cost of electronics.

The larger element size, as well as the much higher speed and lower power front-end electronics required for LHC, together with the expected radiation damage to the detectors (resulting in large dark current and hence shot noise) in the LHC environment, mean that the extrapolation from current use to the LHC requires careful consideration. Some issues arising from charge division for use at ATLAS have been discussed elsewhere[2]. This paper is aimed at setting out, with examples, some of the basic characteristics of the method, as appropriate to LHC.

Capacitive charge sharing involves the comparison of related charges and thus requires that good signal to noise be maintained. The parameters affecting this requirement will be addressed in this paper.

Some simple calculations of two of the most important issues affecting the use of capacitive charge sharing in silicon detectors for the LHC are presented: capacitive loading of the front-end electronics and charge loss through the "floating strips" to the detector back-plane. The calculations are illustrative of the inherent limitations in the use of the method.

Total Charge Collection Efficiency

When charge is deposited on an element in a capacitively coupled array of elements the charge will spread to other elements of the array. The proportion of the charge on any element will be given by the ratio of the individual element's capacitance to the total capacitance of the array. Figure A-1 illustrates this point.

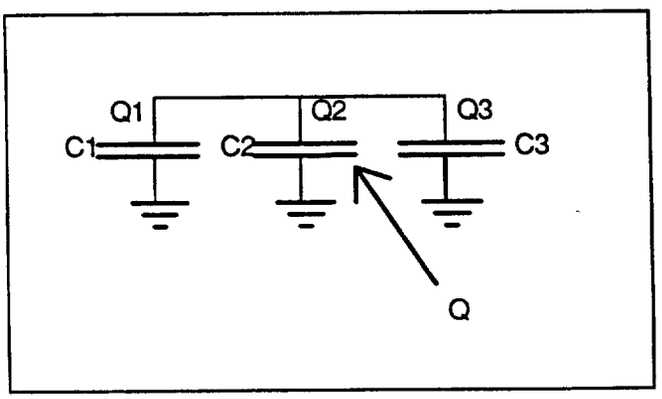

Figure A-1: Charge Sharing

When charge Q is injected on capacitor C2, for example, as the voltage is common across on three capacitors, the charge will distribute across all capacitors in the ratio Q1:Q2:Q3 = C1:C2:C3

where Q1+Q2+Q3=Q

Figure A-2(a) shows an equivalent circuit of a capacitively coupled detector array with "floating strips" between readout strips. Figure A-2(b) shows the circuit used to calculate the charge sharing from the various strips to the amplifier strips.

The calculation commences by assuming charge is deposited on a particular strip within a cell defined by two adjacent readout strips. From this strip, the total capacitance between the strip and each amplifier is calculated, and the charge is divided between the strip and each of the branches between the strip and the adjacent amplifiers (as in figure A-1, above). The charge directed towards each of the amplifiers is similarly divided at each branch encountered between the initial strip and the amplifier. This branching includes the charge division between the readout strip capacitance and the coupling capacitor. The detected charge in each amplifier is assumed to be that fraction of the initial charge which finally ends up on the coupling capacitor. It is assumed that the amplifier inputs are virtual grounds.

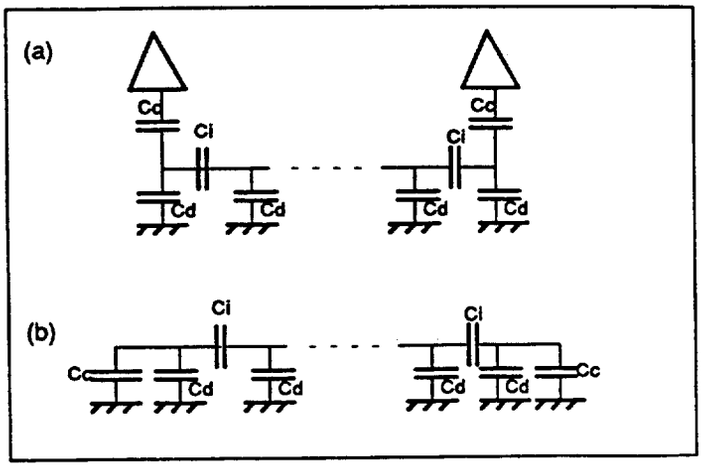

Figure A-2. Equivalent circuit for calculating charge division.

In the limit that the coupling capacitor is large compared with the capacitance on the readout strip practically all the charge reaching the readout node is detected. With large strip capacitance and with the limited values of the coupling capacitor available in silicon detector geometries (typically 100pF), the effect of sharing charge between the coupling capacitor and the readout strip can be significant. For example, with 8.4pF strip capacitance to the backplane(C_d), and 100pF coupling capacitance, a maximum of 92% of the charge is collected. In this regime, DC coupled detectors have the advantage of collecting 100% of the charge.

As the coupling capacitor is large compared with other capacitors and the amplifier input is at ground, charge deposited between two adjacent readout strips does not significantly pass beyond the nearest readout strips into adjacent cells.

The charge which remains on the floating strips is not detected on any amplifier. It is important to maintain the capacitance of the strips to the back plane as small as possible compared with the interstrip and coupling capacitors, to reduce the charge loss.

Figurea A-3(a)-(c) show plots of the charge collection efficiency when the initial charge is deposited on the various strips. The plots shown are for three values of the ratio C_i/C_d (1,5 and 10), where C_i is the interstrip capacitance and C_d is the capacitance of each element to the back plane.. The left most points on these plots correspond to one amplifier in a cell, the right most to the other, whilst in the intermediate points correspond to the initial charge being deposited on the various floating, intermediate strips. The charge collection efficiency in these plots is merely the sum of the charge collected in the two amplifiers of any cell, normalised to the initially deposited charge.

Capacitive Loading of the Front-end Electronics

In current experiments the long shaping times allowed result in a relatively small noise slope as a function of the input capacitance. The high speed required by the 25ns bunch crossing time at LHC, together with the need for low power dissipation, results in preamplifiers with inherently worse noise performance, and steeper noise slopes. The input capacitance must be kept as low as possible.

A typical detector being used at LEP has an element size of 25μm pitch by approximately 10cm length, in 300μm thick silicon, leading to a capacitance to the back plane of C_d=0.08pF/cm. In fact for microstrip detectors, the input capacitance is dominated by the interstrip capacitance with is typically C_i=1.5-2pF per cm of strip length. (In this paper C_i refers to the interstrip capacitance between a pair of "nearest neighbour" strips.)

In contrast, the outer layers of the ATLAS silicon tracker currently under study have an element pitch of 200μm, with up to 12cm length. With these devices, the interstrip capacitance cannot be assumed to dominate over the capacitance of the element to the back plane.

Introducing capacitive charge sharing to such detectors would typically involve the insertion of "floating strips" in the layout, between the readout strips. This reduces the area and hence the capacitance C_d of each element (for fixed readout pitch), but the interstrip capacitance must be kept large compared with C_d if good total charge collection is to be maintained. The inclusion of the intermediate strips modifies the load capacitance, in a way which depends upon the ratio of interstrip to backplane capaciatance, C_i/C_d.

The following figure illustrates the effective circuit used to calculate the input load capacitance for detectors with some number of floating strips between the readout strips.

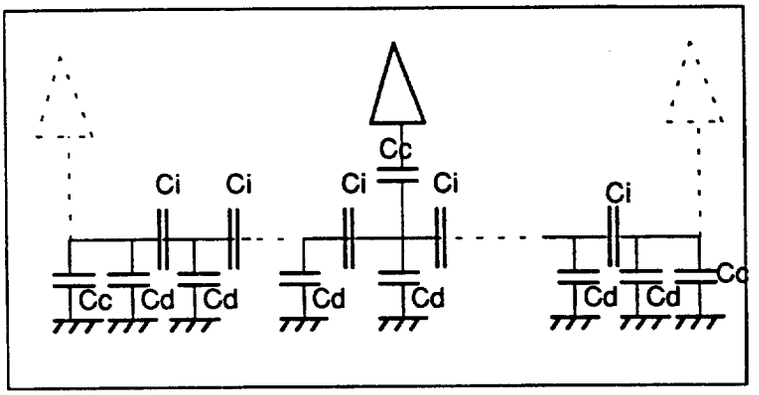

Figure A-4: Capacitive load effective circuit

Note that in order to implement the method the amplifiers must be capacitively, AC-coupled. The coupling capacitor is typically limited to approximately 100pF. This value is assumed below for capacitive charge division examples.

Figure A-5 shows a plot of the total input capacitance. as function of the number of intermediate strips, for various values of the ratio C_i/C_d. The load capacitance is given as a multiple of the backplane capacitance calculated with no intermediate strips.

A uniform element size is assumed for simplicity, and only nearest neighbor interstrip capacitance is considered.

Of note in the plot is that for a given ratio C_i/C_d, the capacitive load decreases with increasing number of floating strips. It will be shown below however, that maintaining a constant value of C_i/C_d is not generally possible.

In the above plots an independent choice of the value of C_i/C_d and the number of floating strips was made to illustrate the effect of these parameters. However, in practice, the interstrip capacitance is related to the detector geometry limiting the choice of the ratio and the number of intermediate strips.

Parametrization of Interstrip Capacitance

In the literature can be found a reasonably consistent set of measurements and calculations of total capacitance and interstrip capacitance, for p-type strips on n-type silicon[3]. The total capacitance on a strip for 300μm thick detectors is given by:

$$C_{total} = [0.8 + 1.4\times(W/P)] \quad pF/cm$$

where W is the strip width and P is the strip pitch.

In order to maintain the simple model of interstrip capacitances indicated in the equivalent circuits in figures A-3 and A-4 the ratio $R = C_i/C_d$ was parametrized to reproduce the above expression for the total capacitance of a strip.

Assuming that the interstrip capacitance is dominated by nearest nighbours, the total capacitance is just given by:

$$C_{total} = C_d\,(1 + 2R),$$

where C_d is the capacitance to the backplane and $R = C_i/C_d$

This equation can be re-written in terms of capacitance per unit length, $c_i=C_i/L$ and $c_d = C_d/L$. The expression for the c_d for a fully depleted detector is then:

$$c_d = \frac{C_d}{L} = \frac{\varepsilon_r\varepsilon_o}{(T/100)}\times(P/100) \quad (pF/cm),\ P \text{ and } T \text{ in } \mu m.$$

$$= 0.351\times(P/100) \quad , \text{for } T = 300\mu m$$

where P is the strip pitch in μm and T is the detector thickness in μm.

Then the resulting expression for the ratio= c_i/c_d is given by:

$$R = 0.5\{((1.4/0.351)\times(100/P)\times(W/P) + (0.8/0.351)\times(100/P) - 1)$$

The relationship obtained between C_i and the detector geometry parameters, W and P, for the thickness T = 300μm, is plotted in figure A-6. It should be pointed out that these fits are based upon the assumption that nearest neighbours strips dominate in the interstrip capacitance. In regions where the ratio $R=C_i/C_d$ becomes large, this assumption becomes less accurate.

This parametrization can be compared with existing data with strip pitch of 50μm and 100μm. Figure A-7 shows this comparison. It is seen that the parametrization gives a good fit to the data for 100μm pitch, but underestimates the slope of the interstrip capacitance as a function of (W/P) for the smaller pitch (50μm), where the values of R are larger. As expected, in this regime, the next to nearest neighbours are contributing significantly to the total capacitance. However, in the region of interest (ratios W/P up to about 0.4), the parametrization is within 25% of the measured interstrip capacitance.

From the figure A-6 it can be seen that there is a strong dependence of the ratio C_i/C_d on the strip pitch. This is mainly due to the use of the ratio (since C_d is directly proportional to the strip pitch), but is also due to an increasing interstrip capacitance with reduced strip pitch.

Figure A-8 shows the load capacitance obtained with the parametrization of the interstrip capacitance, for 100 and 200μm readout pitch, for various strip widths: 5, 10 and 20μm. It is seen that the load capacitance decreases with increasing number of intermediate strips. The slope of this load capacitance depends upon the strip width.

It should be noted that the total capacitance measurements described in the literature will in general vary from the capacitive load calculated here, due to the different availablepaths to ground when the amplifiers are connected to the strips. If the nearest neighbour interstrip

capacitance is dominant, then the total capacitance parametrised above will equal the load capacitance in the case where all strips are readout out. This is because of the virtual ground that nearest neighbour amplifiers offer via C_i. In the case where intermediate strips are used, more than two or more interstrip capacitances, C_i, form a series path to the neighbour readout channel ground, thus reducing the effective capacitance between one readout strip and the virtual ground of its neighbours. This is illustrated below for the case of no intermediate strip and one intermediate strip.

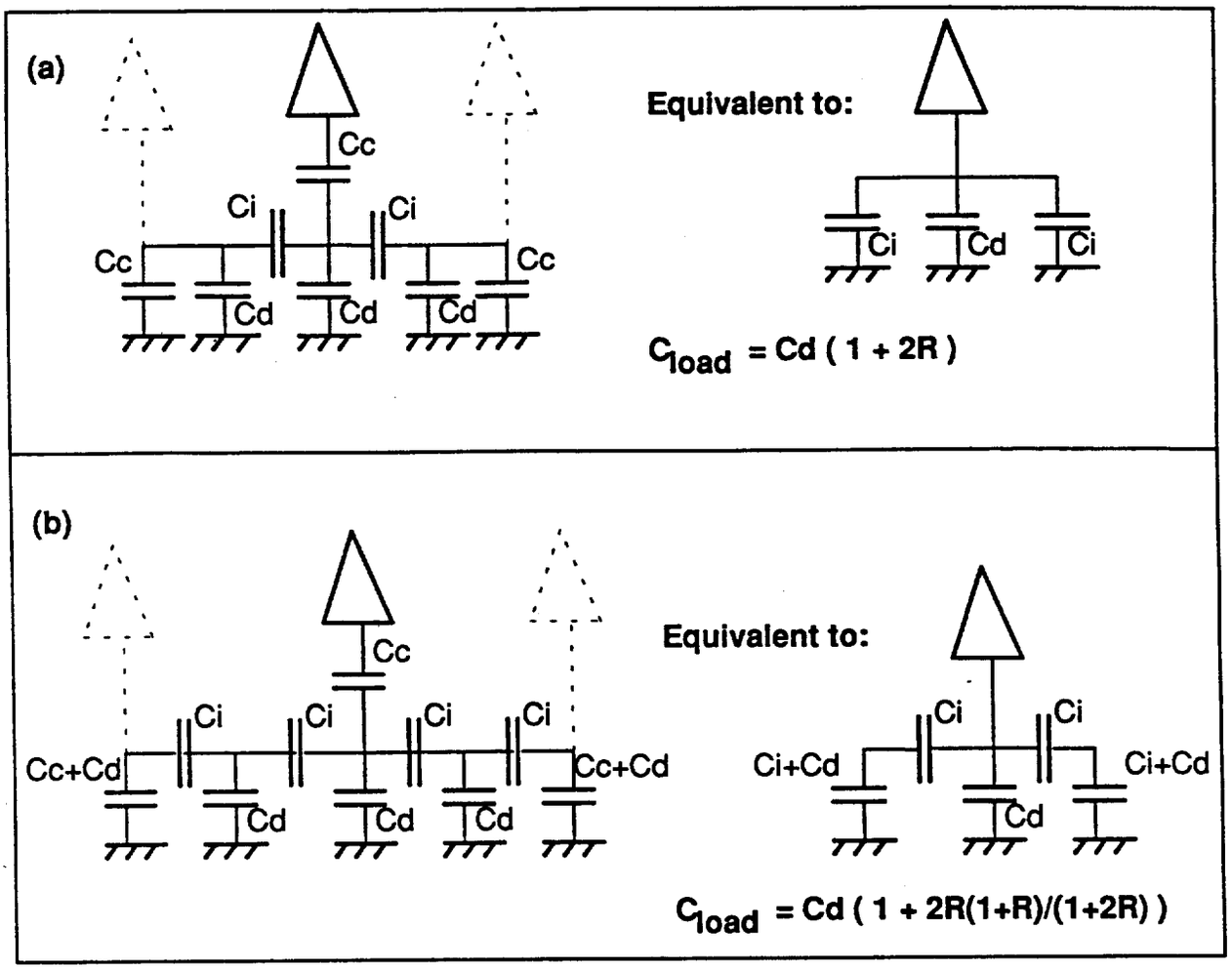

Figure A-9: Illustration of calculation of load capacitance (a)without intermediate strips and (b)with one intermediate strip.

In this model , the load capacitance always decreases with the addition of intermediate strips. If, for example, the between the next-to-nearest neighbours becomes significant, then this situation can change. From figure A-7, it would appear that such a situation occurs at a pitch of 50μm (but is not significant at 100μm). For example, a simple calculation shows that with a next-to-nearest neighbour capacitance of 1/4, which would account for the discrepancy observed in figure A-7(b) the nearest neighbour pitch, then for R>2, the load capacitance with a floating strip is larger than that for the corresponding geometry with all strips readout. Evidently, this effect becomes more important at smaller strips pitches.

Some Example Comparisons

The ramifications of these calculations depend to a large extent on the geometry of the detector layout being considered. To make these considerations more concrete the following examples will be examined (all cases assume 300μm thick detectors).

(A) Simple DC coupled detector.

Strip Length:	12cm
Readout Pitch:	200μm
Strip Pitch:	200μm
Strip Width:	60μm
Number of Floating Strips between amplifiers:	0
Number of Readout Channels:	N

(B) Capacitive Charge Sharing Detector.

Strip Length:	12cm
Readout Pitch:	200μm
Strip Pitch:	(50 - 100)μm
Number of Floating Strips between amplifiers:	(1 - 3)
Strip Widths :	5, 10 or 20μm
Number of Readout Channels:	N

(C) Capacitive Charge Sharing Detector.

Strip Length:	6cm
Readout Pitch:	200μm
Strip Pitch:	(50 - 100)μm
Number of Floating Strips between amplifiers:	(1 - 3)
Strip Widths :	5, 10 or 20μm
Number of Readout Channels:	2N

(D) Simple DC coupled detector.

Strip Length:	12cm
Readout Pitch:	100μm
Strip Pitch:	100μm
Strip Width:	20μm
Number of Floating Strips between amplifiers:	0
Number of Readout Channels:	2N

The results for these selected examples are given in the following tables:

(A)

Number of Floating Strips	C_d (pF)	C_i (pF)	C_{load} (pF)	Maximum Charge Loss (%)
0	8.4	4.0	16.1	0

(B)

Number of Floating Strips	C_d (pF)	Strip Width (μm)	C_i (pF)	C_{load} (pF)	Maximum Charge Loss (%)
1	4.2	5	5.4	11.0	31.9
		10	6.6	12.2	29.4
		20	8.8	14.5	23.8
2	2.8	5	10.0	11.8	25.6
		10	12.6	13.7	22.1
		20	17.9	17.2	17.8
3	2.1	5	15.8	13.0	25.1
		10	21.1	15.6	20.8
		20	31.8	21.1	16.0

(C)

Number of Floating Strips	C_d (pF)	Strip Width (μm)	C_i (pF)	C_{load} (pF)	Maximum Charge Loss (%)
1	2.1	5	2.7	5.5	30.0
		10	3.3	6.1	26.4
		20	4.4	7.3	21.6
2	1.4	5	5.0	5.9	23.8
		10	6.3	6.8	20.2
		20	8.9	8.6	16.2
3	1.05	5	7.9	6.5	23.3
		10	10.6	7.8	18.8
		20	15.9	10.6	14.0

(D)

Number of Floating Strips	C_d (pF)	C_i (pF)	C_{load} (pF)	Maximum Charge Loss (%)
0	4.2	4.0	13.9	0

The acceptable capacitive load in the case of capacitive charge division is expected to be considerably lower than that for the case where all strips are readout out, as precise charge information is required to reconstruct the position of the charge deposition from tracks passing through the detector with high precision.

The optimization of the strip width and number of floating strips depends upon the actual noise slope as a function of the load capacitance. If this slope is steep, then reducing the load, at the expense of charge collection may be the optimum solution.

Discussion and Conclusions

With reasonable estimates of the cell sizes required for the large radius layers of the ATLAS inner detector, the important factors in the application of capacitive charge sharing, are the total capacitive load seen by the front-end electronics and the signal loss to the backplance.

The maximum charge loss increases with the number of floating strips used and decreases with increasing value of the ratio C_i/C_d.

Choosing small values of the ratio C_i/C_d to reduce the load capacitance, leads to higher signal loss to the backplane. Detailed monte carlo studies are necessary to evaluate the optimum choice.

The potential gain in the position resolution with the use of charge division will depend critically on the ability to measure the shared charge in the high capacitive load, high noise regime that is inherent with large element , high readout speed, low power detectors necessary for operation at the LHC.

---

[1] J.B.A. England, et al. Nucl. Instr. and Meth. **185** (1981) 43-47.

[2] Phil Allport, "Silicon Resolution Issues", report to the ATLAS inner detector review panel, November 16, 1993.

[3](a) Yamamoto, K., et al., Nucl. Instr. and Meth. **A326** (1993) 222-227.

(b) Barbaris, E., et al., Talk presented at Int'l Symp. on Dev't of Semiconductor Tracking Detectors, Horishima, Japan, May 22-24, 1993.

(c) Hall, G., et al., Nucl. Instr. and Meth., **A326** (1993) 228-233.

(d) Masciocchi, S., et al., IEEE Trans. Nucl. Sci., **40** (1993), 328.

(e) Kollipara, R., Private communication, February, 1993.

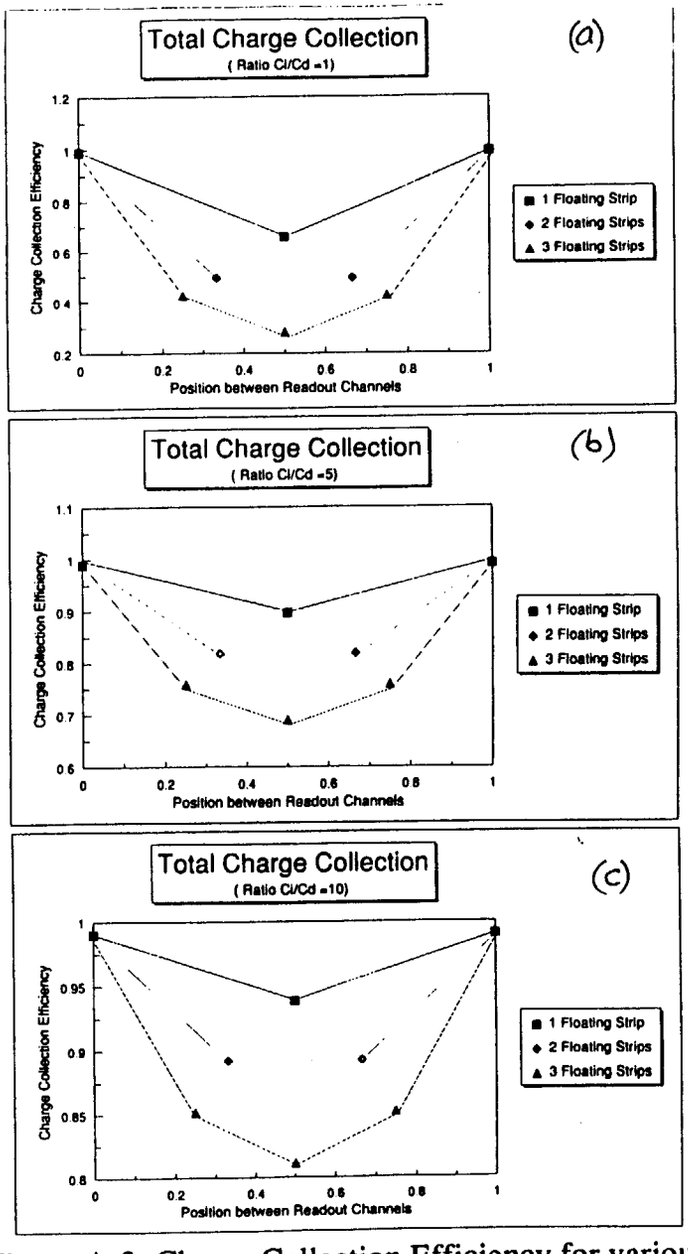

Figure A-3: Charge Collection Efficiency for various numbers of floating strips. Values of Ci/Cd of (a) 1; (b) 5; and (c) 10, are used.

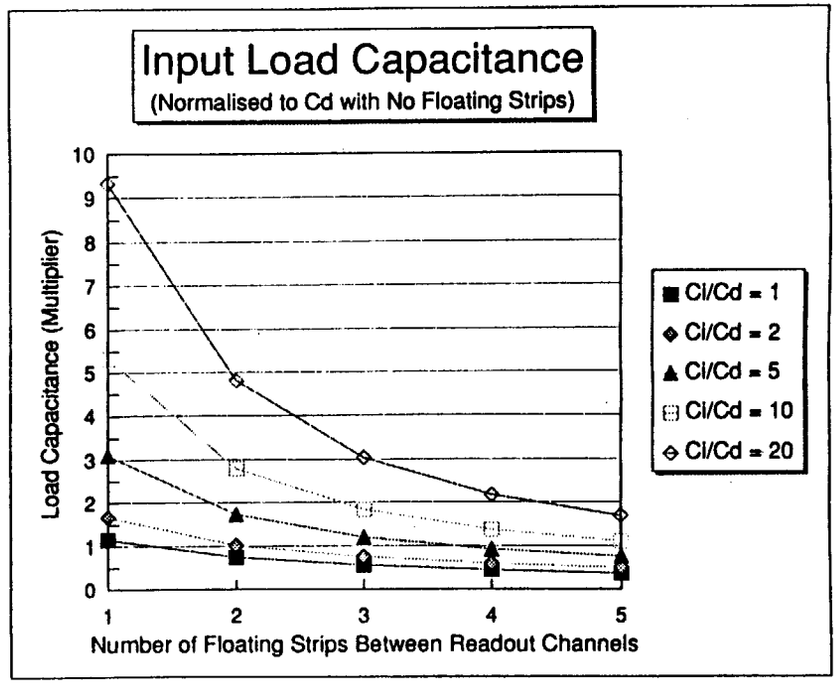

Figure A-5. Input load capacitance for various values of Ci/Cd and different numbers of intermediate strips.

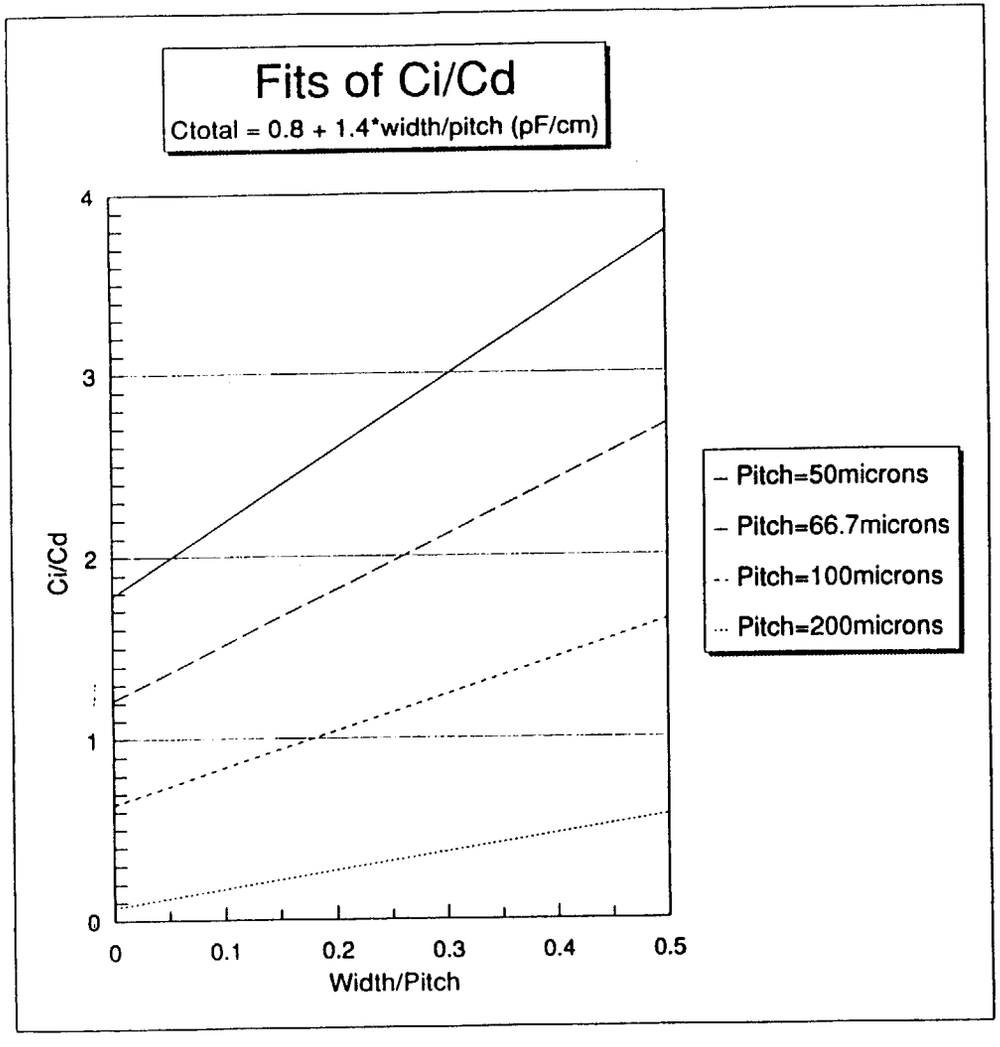

Figure A-6. Fits of the ratio Ci/Cd to the expression
Ctot = 0.8 + 1.4×(width/pitch)
for various strip pitches, as afunction of (width/pitch).

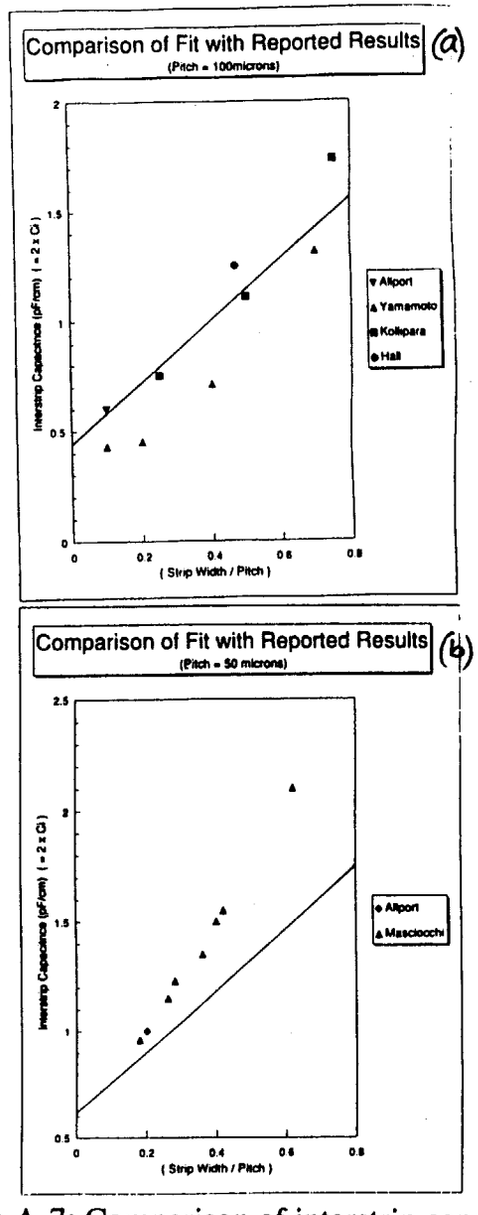

Figure A-7: Comparison of interstrip capacitance calculated from fits to C_i, with measurements and calculations [3].

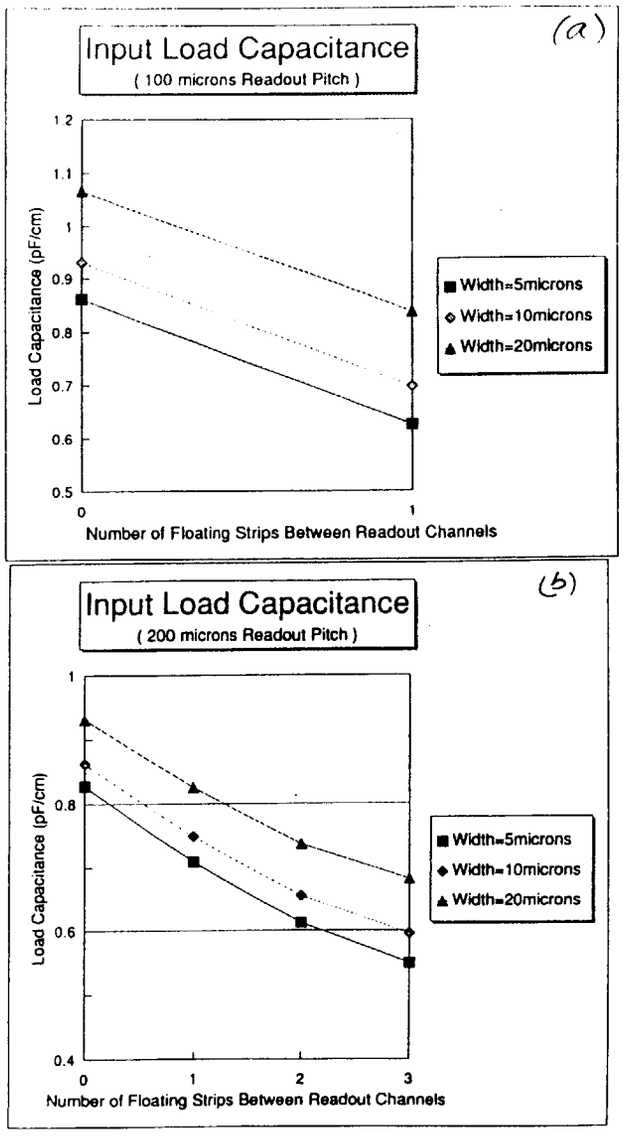

Figure A-8. Input Load Capacitance calculated for various strip widths as function of the number of