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FERMI: a digital Front End and Readout MIcrosystem for high resolution calorimetry

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Abstract

We present a digital solution for the front-end electronics of high resolution calorimeters at future colliders. It is based on analogue signal compression, high speed A/D converters, a fully programmable pipeline and a digital signal processing (DSP) chain with local intelligence and system supervision. This digital solution is aimed at providing maximal front-end processing power by performing waveform analysis using DSP methods.

For the system integration of the multichannel device a multi-chip, Silicon-on-Silicon multi-chip module (MCM) has been adopted. This solution allows a high level of integration of complex analogue and digital functions, with excellent flexibility in mixing technologies for the different functional blocks. This type of multichip integration provides a high degree of reliability and programmability at both the function and the system level, with the additional possibility of customising the microsystem to detector-specific requirements.

For enhanced reliability in high radiation environments, fault tolerance strategies, i.e. redundancy, reconfigurability, majority voting and coding for error detection and correction, are integrated into the design.

1 Introduction

The electronics for signal detection and triggering in experiments at the next generation of colliders will be one of the most complex and challenging systems to be conceived for high energy physics. In particular data volume, speed and complexity of decision processes call for an unprecedented performance in signal identification, data compaction and trigger processing already at the detector level.

For calorimeters operating in the environment of high luminosity machines, powerful signal processing at the front-end level becomes essential. Crucial considerations are the extremely wide dynamic range and bandwidth requirements for the front-end electronics, the high selectivity of the trigger functions, as well as the massive data volume to be transferred from highly granular and hermetic detectors to the subsequent stages of the trigger and readout systems.

These requirements are best met by an early digitisation of the detector information, followed by on-chip digital signal processing and buffering at both the first-level and subsequent decision latencies. A digital approach can concentrate high processing power at the front-end level by means of digital waveform analysis. Minimising analogue circuitry has definite advantages in providing absolutely normalised data, a higher level of reliability with fault tolerance architectures and a high degree of programmability from the very beginning of the data acquisition chain [1].

The FERMI microsystem is a digital multi-channel data acquisition and signal processing module for high-resolution calorimeters, implemented as a Silicon-on-Silicon multichip microsystem [2, 3]. It is designed to perform dynamic range compression, digitisation up to 80 MHz, digital signal processing, trigger functions and buffering of calorimeter data up to and including second-level trigger latency. It is intended to be mounted directly on detectors, along with a controller performing supervision, calibration and other system functions. For applications with high level of radiation and limited accessibility, the design incorporates a high degree of redundancy, fault and radiation tolerance.

Currently, the aim of the project is to produce a microsystem prototype containing all functional blocks integrated in three different types of ASICs. As a continuation, a full multi-FERMI system will be developed. It will include local and remote controllers connected via optical links, interfaces to trigger and readout processes as well

as system features required for integration in actual detectors.

This paper, first in a series of two, describes the architecture and design of the FERMI microsystem. The following paper [4] describes in more detail the digital filter stages and related DSP algorithms. The present paper is organised as follows: the first section gives an overview of the overall architecture and of the design strategies, with emphasis on the fault tolerance aspects. The following three sections describe in detail the individual components of the system. The next section describes the microsystem substrate and related interconnection technologies, together with global system considerations. The last section contains our concluding remarks.

2 The architecture of FERMI

2.1 System overview

FERMI is a multi-channel data acquisition and signal processing module implemented as a Si-on-Si multichip microsystem. The microsystem, realised as a large silicon multi-layer substrate with four metal layers, supports ASICs, components, interconnections and transmission lines.

Fig. 1 contains all major FERMI components in the form of a simplified block diagram. The first prototype will contain nine complete channels.

Input signals, with a dynamic range of 15–16 bits, are compressed and digitised at sampling frequencies up to 80 MHz. The resulting 10-bit data are linearised and expanded to a full 16-bit representation by means of a look-up table containing the inverse of the transfer function of the entire detector-electronic chain. This provides digital data with absolute calibration from each individual channel.

The expanded data from all channels are individually discriminated with independent programmable thresholds. They are then summed and processed in order to provide energy and time information of the event to the first-level trigger process. At this level, flags can be generated identifying possible pile-up conditions for subsequent special processing. Also, the expanded data are stored in a dual-port memory until the decisions from the first- and second-level triggers become available. This storage occurs in memory positions given by an external memory management unit. A time frame, i.e. a sequence of contiguous data samples, is associated with each

event accepted by the first-level trigger. Storage locations containing samples not included in such time frames are returned to the list of free memory. Time frame memory locations are also returned to the free list after having been rejected by the second-level trigger or read out by the data acquisition system.

The I/O function contains provisions for full or filtered readout of time frames. In the latter case the information contained in the time frame is extracted by means of optimised nonlinear digital filtering techniques. A specific feature of the FERMI architecture is its high degree of flexibility, with more than one hundred different programmable parameters controlling its operation. A local microcontroller supervises the operation of the entire system and sets all the programmable configuration parameters.

All the functions described above are implemented into three main blocks:

- the Analog ASIC, containing the analog signal compressor and the A/D converter for each detector channel;
- the Channel ASIC, containing look-up tables (LUT) and main data memories for three channels;
- the Service ASIC, containing the digital filters, the local controller, the clock manager and readout logic common to all channels in the microsystem.

To achieve a high level of reliability, FERMI is being designed with a high degree of fault tolerance, and for later implementations rad-hard technologies are also foreseen.

2.2 Fault tolerance

The FERMI microsystems are intended to be installed directly on the detector structure, in a harsh environment with limited accessibility. System reliability is therefore one of the most important design issues. Massive fault tolerance approaches are needed in order to provide a high degree of reliability and system survival over the operational life of the detector. To this end, both completeness of data (no losses) and credibility (no corruption, masking or aliasing) must be guaranteed.

The fault tolerance strategy adopted for FERMI is a combination of self diagnostics and graceful degradation schemes, since both transient and permanent faults are

to be expected with comparable probabilities. Given the large number of channels and the high data rate, the self diagnostics is implemented in a concurrent and distributed way. Using graceful degradation architectures, the faulty system retains its functionality with a reduced signal processing performance. This has been realised using a centralised control system reconfiguring the architecture on the occurrence of a permanent fault. The hardware fault tolerance solutions implemented in the FERMI architecture use error correction coding, redundancy and reconfigurability as well as residue-number techniques.

For the Look-Up Table and the Memory, concurrent error-detection and correction was chosen, since information stored in these memories is critical for any subsequent operation. In particular, a very strong protection has been devised, where data encoding (Hamming solution) is complemented by the possibility of replacing faulty memory cells by a small associative memory. A novel triple-redundancy scheme has been applied to all otherwise unprotected parts, in order to achieve a homogeneous fault tolerance over the entire system. This grants correction of transient faults without undue redundancy and survival to (a limited number of) multiple faults.

Prior to filtering, the fault tolerance coding is changed from Hamming to a modified residue-number technique. This is to allow for the operations of channel addition, feature extraction, truncation and reformatting of the first-level trigger process, which are not compatible with Hamming coded data.

For the digital filter sections, the solution is based on a redundant structure of multiplier-adder modules [5], thereby allowing concurrent fault detection at the filter level and host-driven reconfiguration of the filter architecture.

3 The Analog ASIC

3.1 Basic architecture

A FERMI microsystem receives analog signals with a dynamic range of about 15–16 bits. State-of-the-art CMOS technology, suitable for rad-hard implementations, allows digitisation at or above the typical LHC crossing frequency of 40 MHz with a resolution of at most 10 bits. This requires dynamic range compression at the analog input level. The corresponding quantisation noise yields only a negligible contribution

to the total detector resolution, provided an appropriate nonlinear transfer function is matched to the energy-dependent resolution of the detector [1].

Each of the channels in a FERMI microsystem has its analog part in the form of an ASIC, containing the dynamic range compressor, the Analog to Digital Converter and a pulse injection circuit. It also contains a local voltage regulator and a DAC-controlled amplifier/servo loop for level shift and baseline control (see Fig. 2). For actual applications, the dynamic compressor and its related auxiliary circuits could be integrated into the analog preamplifier/shaper stages.

3.2 Dynamic compressor

A piecewise linear transfer function was adopted for signal compression, where the input signal is amplified by stages with soft limiting characteristics and different gains.

Tests of the first prototype implemented in the Gennum Ga911 process [6] showed that an architecture of four parallel differential amplifiers generating a piecewise linear response can be matched to almost any existing detector resolution. This prototype had a bandwidth of about 50 MHz and an output noise of 250 μV (to be compared with an ADC LSB of 2 mV), in excess of requirements.

In the final Analog ASIC implementation, the noise figure is improved (180 μV). This new version includes a level shifter and a comparator in the output stage, forming a slow servo loop, thus allowing for improved temperature stability and DC-coupling between compressor and ADC. Furthermore, an on-chip voltage regulator for the compressor improves the power supply noise rejection.

The transfer characteristics of the compressor, shown in Fig. 3, has a channel-to-channel rms spread of less than 1% and good thermal stability (about 0.4 LSB/°C at the break points). The resulting quantisation noise contributes at most 0.3% to the detector fractional resolution at high energies, which matches the asymptotic performance of most current high-performance calorimeters.

3.3 Analog to Digital Converter

The block diagram of the ADC is shown in Fig. 4. It is a Parallel Successive Approximation (PSA) converter consisting of 14 identical Successive Approximation (SA) ADC channels, one common reference voltage generator, a global control pulse gen-

erator and an output register [7]. In this scheme, 4 clock cycles are required for overdrive recovery and autozero of comparators, plus 10 cycles for the conversion.

The SA-ADC used in the PSA-ADC consists of a S/H circuit, a two-step DAC, an auto-zeroed comparator and a shift register. In order to reduce offset differences between different SA-ADCs channels, the S/H circuit is designed without active components, and the coarse and fine reference ladders are common to all channels.

Special design techniques were adopted in order to minimise clock and charge feedthrough during the sampling and autozeroing phases. Table 1 summarises the performance of the first complete PSA-ADC prototype.

A differential nonlinearity plot of a PSA-ADC prototype is shown in Fig. 5.

3.4 Layout of the Analog ASIC

The Analog ASIC contains nine different functions, i.e. pulse injector, compression amplifier, level shifter, feedback amplifier, A/D converter, local voltage regulator, clock buffer and pads. The total size of the chip is 5.6×4.3 mm. The technology chosen for the prototype was AMS 1.2 μm BiCMOS process [8]. Fig. 6 shows the microphotograph of the ASIC.

4 The Channel ASIC

4.1 Basic architecture

Each of the three Channel ASICs in a FERMI microsystem contains three parallel channels deriving their input data from the corresponding ADCs in the Analog ASICs (see Fig. 7). The 10-bit data from the ADCs are transformed by look-up tables (LUT) into a 16-bit corrected and linearised representation. The data are then transferred along two paths: one to the local first-level trigger sum, while the other merges with data from the other two channels to be fed to the data memory at a place determined by the externally provided insert address pointer. An external extract address pointer selects in a similar way a 48-bit memory word, from which a data selector extracts individual 16-bit data words to be transferred to the Service ASIC for subsequent processing.

Each Channel ASIC is also responsible for storing one of three possible flags, one pulse-detect and two pile-up flags. These flags are generated in the Service ASIC and are sent to each channel ASIC. A programmable selector chooses which flag should be included in the data stream fed to the data memory of the ASIC in question.

4.1.1 Look-up table

The look-up table compensates for the nonlinearities of the detector/conversion chain. It can also perform pedestal subtraction and apply corrections for detector nonlinearities. The architecture of the look-up table contains two multiplexers, of which the first one provides, if required, a bypass path around the LUT. The second multiplexer allows programming of any given cell in the LUT via a data register. A monitoring register on the LUT output has been included for diagnostic purposes. Also, digital test patterns for testing the entire subsequent logic can be injected into the LUT.

4.1.2 Data extraction to the first-level trigger

In the Channel ASIC, data intended for the first-level trigger process is thresholded and summed for subsequent processing in the Service ASIC (see below). The channel enable function contains a programmable threshold which can be used to discriminate against individual channel noise. It may also be used to disable malfunctioning channels entirely, in order to exclude them from participating in the trigger summation. This feature allows a precise and programmable tailoring of the contribution of each individual channel to the first-level trigger process.

4.1.3 Data memory

The data memory is realised as two toggling single-port memory banks, operating on alternating odd and even addresses. Additional fault tolerance in the memory function is provided by a small two-cell associative memory, which intercepts the main memory access when it detects an attempt to write into disabled locations. In analogy with the LUT, the data memory block contains registers for injection of diagnostic data at the input as well as a monitor register at the output for testing purposes.

An internal 10 MHz serial link is used to access and control registers and multiplexers throughout the ASIC. The latter are used to inject test data into a number of test points along the data path. Suitably placed spy registers monitor the results as well as the error status of different system functions.

4.2 Fault tolerance

In the Channel ASIC, fault tolerance is achieved by providing each 10- or 16-bit data word with a 5 (respectively 6) bit error correction code (ECC) of Hamming type, allowing single-bit correction and double-bit detection. The 66-bit data (3 channels $\times$ 22 bits) are merged with their corresponding flags, which are stored in three error protected bits. Additional fault protection is achieved by triplicating all fault sensitive logic (shaded in Fig. 7) with a hardware current voting. Further protection is provided by an extra bit in the look-up table containing the address parity. This feature will detect fatal address errors that have escaped the triplicated address decode scheme. All data busses between the different ASICs are ECC protected. For what concerns addressing, single-bit errors will be corrected, double-bit errors will temporarily disable the memory access to prevent overwriting data.

The fault protection of the data for the first-level trigger logic is converted from ECC to a modulo-3 residue code at the input of the first adder stage. This code is convenient for checking arithmetic calculations and will accompany the data throughout the rest of the system.

As mentioned in the previous subsection, a two-port associative memory provides additional fault tolerance to the main memory by backing up possibly faulty storage locations.

The Channel ASIC contains also status registers that collect all error signals generated within the ASIC, one for fatal errors and one for non-fatal errors, each with a mask register so as to disable individual error bits as required. Errors are reported to the Local Micro Controller (see below) through interrupt signals, one for each status register.

4.3 Layout of the Channel ASIC

For verification purposes prior to implementation, the VHDL code describing the Channel ASIC was first synthesised into Field Programmable Gate Arrays. The equivalence of the final ASIC layout and of the VHDL specification of the Channel ASIC was then investigated by extensive simulations with test vectors.

The layout consists of four different parts, i.e. memories, control logic, clock buffers and pads. The memories are of the static-RAM type with six transistors in each cell. This solution was chosen because of its robustness. In order to achieve the required access time, the memory array is split into two halves. In the prototype, the organisation of each half is 64 rows $\times$ 22 bits $\times$ 8 columns for the lookup tables and 64 rows $\times$ 69 bits $\times$ 4 columns for the data memory. Each data word has a hard coded parity bit which reflects its address parity. Since the chip has three look-up tables and one data memory, this yields a total of 12.6 kbytes of RAM and 448 bytes of ROM.

The control logic is divided into four parts. Three of the parts are identical since they controls one look-up table each, the fourth block controls the data memory. To maximise flexibility these blocks were designed with standard cell technology, where some of the crucial parts are triplicated.

A microphotograph of the Channel ASIC is shown in Fig. 8.

The total size of the chip is 17.1×10.9 mm and the chip has approximately 930 000 transistors. The technology chosen for the first implementation was the AMS 1.0 μm CMOS process.

5 The Service ASIC

5.1 Basic architecture

The Service ASIC, common to all channels in a FERMI microsystem, contains several functional blocks performing a variety of control and monitoring tasks (see Fig. 9). It contains a PLL-based clock manager, data extraction circuits in the form of digital filters providing energy and time information to the first-level trigger process, and additional digital filters processing data for the second-level trigger and final readout. Also, it contains a programmable Local Micro-Controller (LMC) managing

initialisation, calibration and monitoring of the entire FERMI system. The LMC also provides the interface between the individual FERMIs and their external system environment, in the form of a multi-FERMI board under the supervision of a FERMI Board Controller (FBC).

5.1.1 Clock manager

The clock manager is a timing unit which ensures the synchronisation of all the devices within a FERMI module, relating it to the overall external timing of the experiment. It receives the clock from the FBC and control information through the FERMI serial link. A delay generator is built around a voltage controlled ring oscillator, made of 16 differential stages, phase locked to the external system clock reference. By means of an additional fine delay, the clock phase within each FERMI can be adjusted with an accuracy of 98 ps. This fine resolution allows an accurate setting of the sampling phase with respect to the input signal.

For diagnostic purposes, a programmable clock burst control enables freezing the system at any given state.

5.1.2 Read-out controller

The read-out controller contains the circuitry required to read an event from the data memory and present it at the I/O port. Each event is stored as a time frame in the memory and can be presented at the outputs either as a sequence of unprocessed data or in the form of one value per channel, as determined by the second-level digital filters.

The readout operation is initiated by the external FBC downloading address pointers referring to the memory locations which contain the data for the requested event. When the pointers are being downloaded a readout mode is also selected. If a filtered readout is requested, data is routed through the second-level filters, otherwise it is sent directly to the output register. The readout sequence is asynchronous with respect to the external circuitry, with the output register implemented as a two-slot FIFO. This allows sychronisation of internal and external transfer processes.

As discussed above, for each event a set of flags is also stored in memory. Since these flags are generated by the first-level feature extraction circuits after data has

been stored in the memory, the flags of an event will not be stored in the corresponding time frame. Therefore, an additional pointer must be provided to select the word containing the flags. During readout, this word is read before the individual samples, so that its content can affect the operation of the second-level filter.

5.1.3 Local Micro Controller

A FERMI microsystem contains 137 programmable registers controlling system configuration, parameter settings (e.g. thresholds, filter coefficients) and for diagnostic and test purposes.

The LMC controls the above parameters and deals with error interrupts. It is a custom circuit built around a 16-bit CPU embedded in the Service ASIC. Externally, it is connected, as a slave, to the FERMI Board Controller by a serial link. Internally, it is connected as a master to the four digital ASICs on the FERMI module with another serial link. Both serial links are clocked synchronously at 10 MHz.

Under normal operating conditions, the FBC loads a task into the LMC memory, which then executes it. In a backup operating mode, the FBC connects directly to the ASICs, bypassing the LMC. An assembly language with instructions specific to the operations of the LMC has been developed.

5.2 Feature extraction

The feature extraction functions of FERMI consist of two different digital filter stages. The structures of the filters implemented in the first FERMI prototype were chosen after a systematic evaluation of more than twenty different architectures. We give below a brief description of the two filter stages. Details on their architecture and performance are given in the following paper [4].

5.2.1 Filter $F1$

Filter $F1$ is designed to identify a signal, providing accurate timing information and energy information for the first-level trigger process. It operates on the sum of all FERMI channels, while the individual channel data are stored in the data memory. These data are later transferred to filter $F2$ if validated by the first-level trigger process.

Filter $F1$ consists of two parallel finite impulse response (FIR) filters, each with five elementary stages (plus one for redundancy), and a three-point maximum finder. The energy extraction FIR is optimised to extract the energy in the presence of several artefacts. Typically it is an averaging operator with a relatively wide response on pulses in the time domain to suppress electronics noise and sample timing jitter. The timing extraction FIR produces a sharp maximum for each pulse even if partially overlapping with another one. This subfilter is close to a deconvolution operator which has a narrow response in the time domain and a lower amplitude resolution due to the higher noise gain. Because of the sample timing jitter, this filter is combined with the maximum finder, as the sharpness of the response deteriorates with changing sampling position.

Filter $F1$ provides the first-level trigger process with error-free 11-bit data and the Channel ASICs with three flags, i.e. peak detection and two different pile-up flags.

5.2.2 Filter $F2$

Filter $F2$ is designed to measure with high precision the signal amplitude of the time frames validated by the first-level trigger by extracting the entire waveform information. It takes as input the time frame data and the corresponding flags for each individual channel. If required, the whole time frame data can be read out without filtering for full external processing of the waveform structure.

The architecture of filter $F2$ contains three parallel FIR filters and an order statistics (OS) operator. Compared to a single FIR filter, the FIR-OS filter structure [9] offers more robustness against the different artefacts in the acquired data. Time frames from all FERMI channels are processed independently using the same filter.

The performance of this filter was evaluated by means of simulated data including all known sources of artefacts, i.e. electronics noise, pile-up noise, sampling jitter, quantisation noise and finite arithmetic effects. It matches a calorimeter resolution with a scaling term of 0.03 and a constant term of 0.005. It is also able to produce a fairly accurate output even in the case of pulse overlaps not detected by filter $F1$.

5.3 Fault tolerance

In the Service ASIC, the fault tolerance part of the architecture follows the same approach as in the Channel ASIC. It incorporates several techniques, such as error correction code (ECC) of Hamming type and triplication of all fault sensitive logic with hardware current voting. All data busses between the different ASICs are ECC protected. Single-bit errors will be corrected, double-bit errors will be flagged.

The fault protection of the feature extraction hardware is based on the modulo-3 residue code. In addition, the digital filters for both first- and second-level feature extraction have a redundant, reconfigurable architecture which allows complete replacement of faulty cells. Furthermore, if more than one cell in each filter becomes faulty, a graceful performance degradation is ensured.

As for the Channel ASIC, the Service ASIC contains also status registers that collect all error signals generated within the ASIC, one for fatal errors and one for non-fatal errors, each with a mask register so as to disable individual error bits as required. Errors are reported to the LMC through interrupt signals, one for each status register.

5.4 Layout of the Service ASIC

The equivalence of the ASIC layout and the VHDL specification of the Service ASIC was verified by extensive simulations with test vectors.

The layout of the Service ASIC, currently consisting of three individual circuits, is shown in Figs. 10–12. The sizes are 35 mm^2 for the LMC, 26 mm^2 for the readout controller and 59 mm^2 for the filters. The technology chosen for the prototype run is ES2 0.7 μm CMOS process [10].

6 The Microsystem

6.1 Substrate

The FERMI microsystem is implemented as a thin-film Multi-Chip Module (MCM-D) on a silicon substrate with four metal layers [11]. All ASICs are flip-chip bonded to the substrate, which provides high-density interconnections by integrated transmis-

sion lines. The flip-chip bonding technique, as used in the FERMI MCM, is more performant and reliable than conventional wire-bonding. Furthermore, the parasitics associated with a flip-chip bump are much smaller than with wire-bonding by more than a factor 20. Also it allows connections to be optimally placed across the surface of the ASICs, thus simplifying the interconnection patterns.

The MCM solution provides the proper environment for high-density, low-level applications in terms of noise and isolation properties, with cross talk levels lower than -80 dB. Also, the MCM approach offers unprecedented levels of package density and integrated connectivity, thus providing a higher level of reliability. In the FERMI case, 13 ASICs (possibly more) are interconnected on a surface of a few cm^2 by over 1500 transmission lines. In addition, further reliability is provided by the inherent match of mechanical and thermal properties between the ASICs and the Si carrier.

A preliminary floorplan of the FERMI microsystem has been made specifying the placement of the nine Analog ASICs, the three Channel ASICs and the Service ASICs together with required decoupling capacitors, as shown in Fig. 13. The prototype microsystem will have an area of 50×50 mm^2 and 200 external I/O connections.

6.2 Global system considerations

In actual applications, a number of FERMIs will be mounted on a board, with external circuitry providing the following functions:

- local first-level trigger: combining data from several FERMIs into one trigger-cell value, transmitted to the global first-level trigger process;
- local second-level trigger: reading data from several FERMIs and transmitting them to the second-level trigger process;
- address generator: generating new addresses at each system clock, pointing at free storage locations for the sampled input data, and generating the pointers required for readout;
- controller: initialising, controlling and supervising the FERMIs.

These functions must be extremely fault tolerant, since any failure will seriously reduce the functionality of the entire system. For a board containing 30 to 40 FERMIs,

a few two-way optical links with 1 Gbit/s bandwidth are sufficient for communication with the external environment.

7 Conclusions

The development of multichip microsystems, integrating VLSI sub-micron ASICs into a higher level of complexity, allows to conceive a new generation of fast digital electronics for high energy physics experiments. The ensuing level of signal processing power which becomes available can address in a novel way the acquisition and processing challenges of experiments at the next generation of high energy colliders.

New digital front-end architectures can provide superior selectivity in event selection, as well as the capability to extract the complete information contained in the full waveform structure of each event. They also provide a new level of reliability, both from the point of view of high-density monolithic interconnections and as a practical and affordable application of powerful fault tolerance architectures.

We have described a digital solution for front-end acquisition and processing of calorimetric data. It is realised as a multichannel MCM unit performing real time digitisation, data storage and complete feature extraction on continuously sampled data at clock frequencies exceeding 40 MHz, to be extended to 80 MHz. Extensive fault tolerance architectures have been incorporated in the design. System aspects are being studied in view of the integration of FERMI into actual experiments.

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References

[1] V.G. Goggi and B. Lofstedt: "Digital Front-end Electronics for Calorimetry at LHC," Proc. ECFA Large Hadron Collider Workshop, CERN 90–10, ECFA 90–133, **3** (1990) 190.

[2] A. Dell'Acqua *et al.*: "A Digital Front-end and Readout Microsystem for Calorimetry at LHC," *IEEE Trans. on Nuclear Science*, **40** (1993) 516.

[3] A. Dell'Acqua *et al.*: "A Digital Front-end and Readout Microsystem for Calorimetry at LHC," *Nuclear Instruments and Methods in Physics Research*, **A344** (1994) 180.

[4] R. Benetta *et al.*: "'Optimized digital feature extraction in the FERMI microsystem," submitted to *Nuclear Instruments and Methods in Physics Research.*

[5] A. Dell'Acqua *et. al.*: "System level policies for fault tolerance issues in the FERMI Project," in *Proc. IEEE Int. Workshop on Defect and Fault Tolerance in VLSI Systems,* 1993, pp. 1–8.

[6] Gennum Corporation, P.O. Box 489, Station A, Burlington, Ontario, L7R 3Y3, Canada.

[7] C. Svensson, J. Yuan: "A 10-bit 5 MS/s succesive approximation ADC cell used in a 70 MS/s ADC array in 1.2μm CMOS," *IEEE Journal on Solid State Circuits and Systems*, **29** (1994) 866.

[8] Austria Mikro Systeme International, Schloss Premstätten, A-8141 Unterpremstätten, Austria.

[9] S. J. Inkinen and J. Niittylahti, "Trainable FIR – order statistic hybrid filters," submitted to *IEEE Trans. on Circuits and Systems–II: Analog and Digital Signal Processing*, April 1993.

[10] ES2, Zone Industrielle, F-13106 Rousset, CEDEX, France.

[11] S.F. Gong, *et al.*: "Investigation of high-speed pulse transmission in MCM-D," *IEEE Trans. on Components, Hybrids and Manufacturing Technology*, **16** (1993) 735.

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10 Layout of the service ASIC: LMC 27
11 Layout of the service ASIC: readout controller 28
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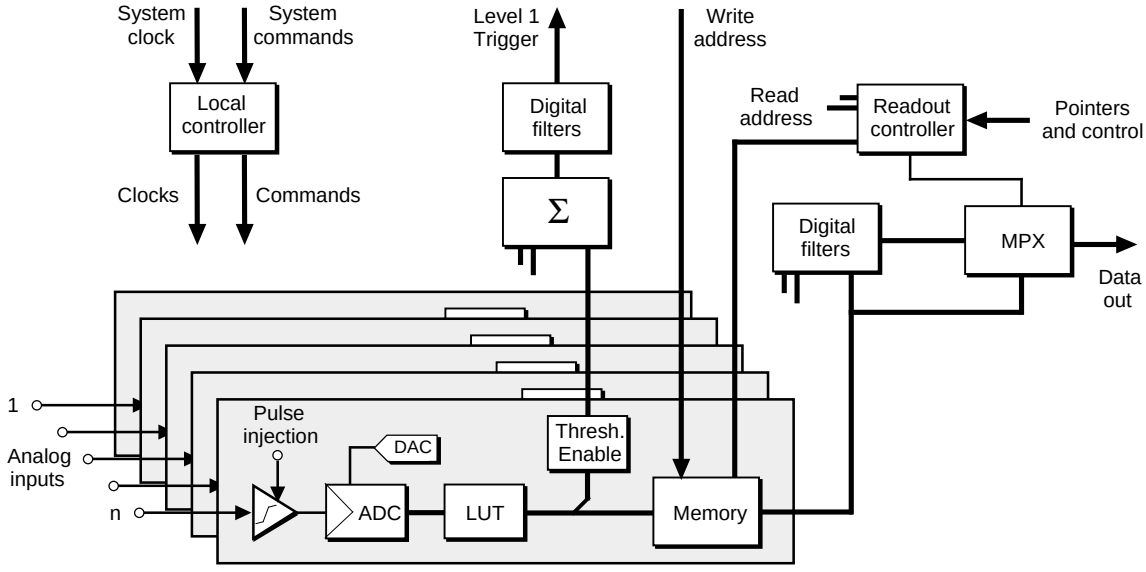
13 Preliminary floorplan of the microsystem substrate 30

Figure 1


System clock
System commands
Local controller
Clocks
Commands
Level 1 Trigger
Digital filters
Σ
Write address
Read address
Readout controller
Pointers and control
Digital filters
MPX
Data out
1
Analog inputs
n
Pulse injection
DAC
ADC
LUT
Thresh. Enable
Memory

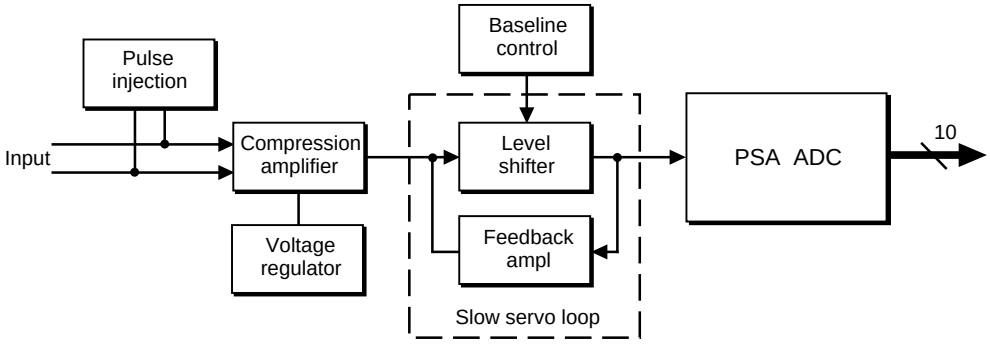
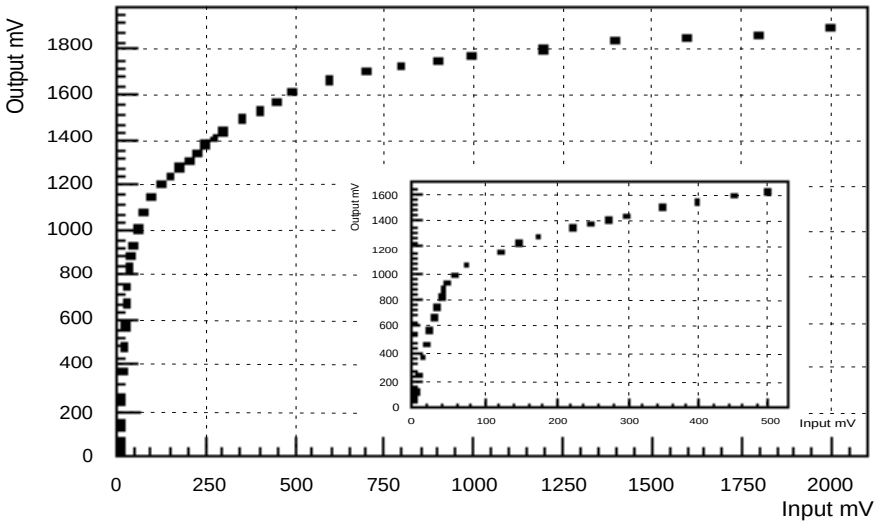
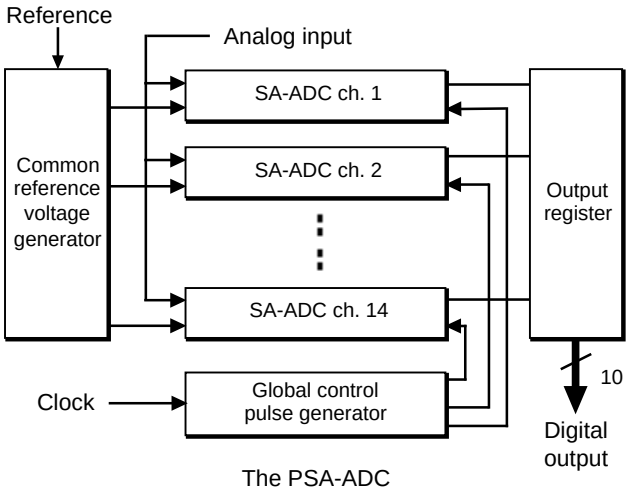
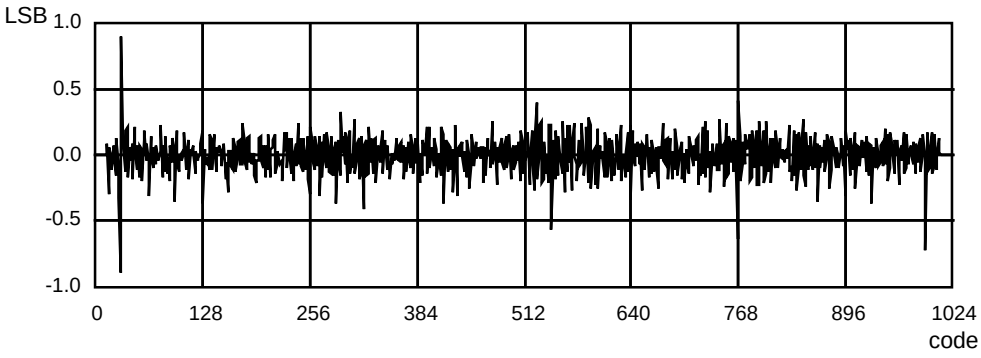

Baseline control
Pulse injection
Input
Compression amplifier
Level shifter
PSA ADC
10
Voltage regulator
Feedback ampl
Slow servo loop

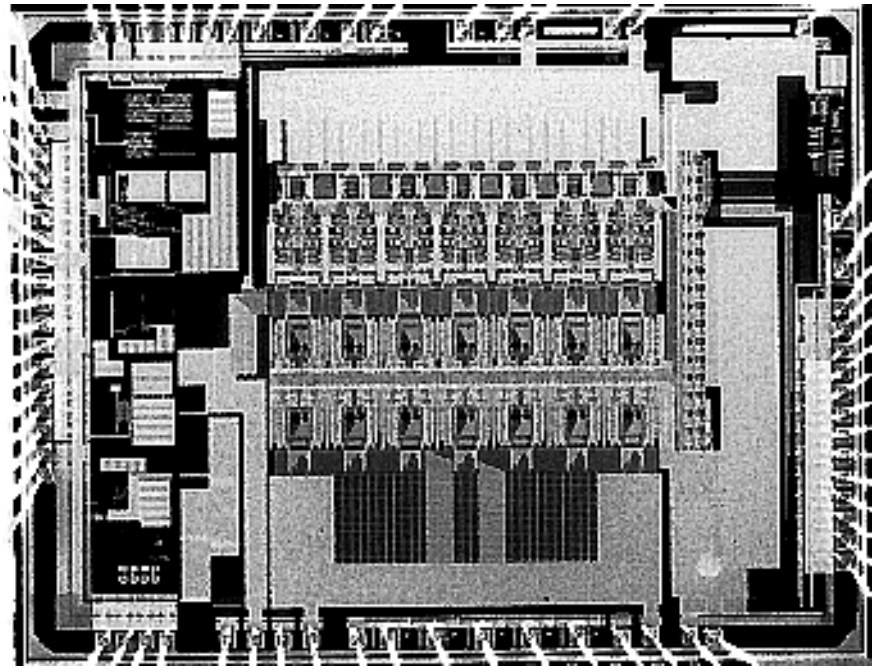
Figure 3

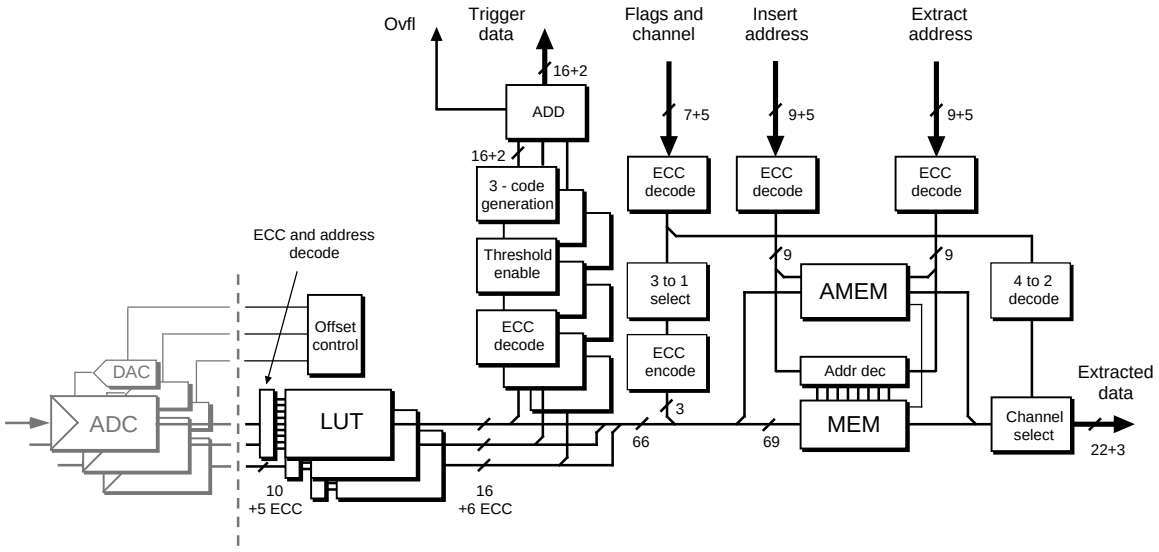

Output mV
1800
1600
1400
1200
1000
800
600
400
200
0
0
250
500
750
1000
1250
1500
1750
2000
Input mV
Output mV
1600
1400
1200
1000
800
600
400
200
0
0
100
200
300
400
500
Input mV

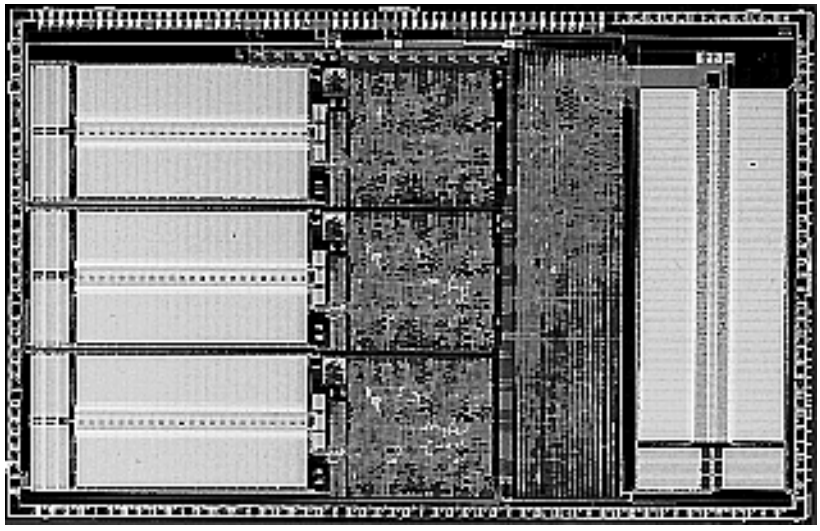

Reference
Analog input
SA-ADC ch. 1
SA-ADC ch. 2
SA-ADC ch. 14
Common reference voltage generator
Output register
10
Clock
Global control pulse generator
Digital output

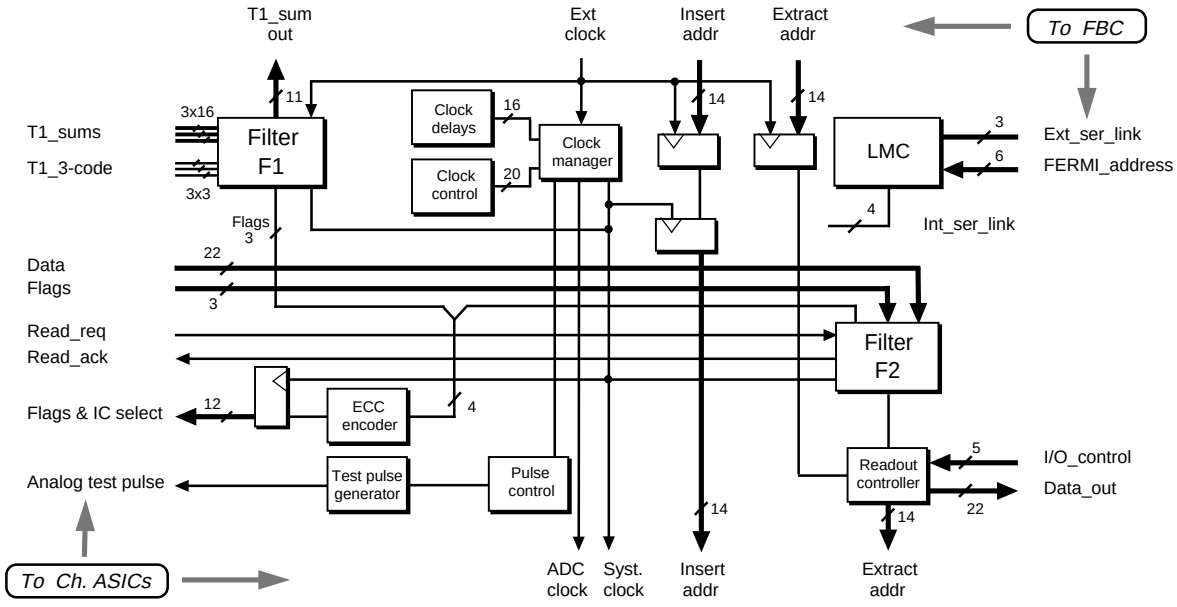
The PSA-ADC

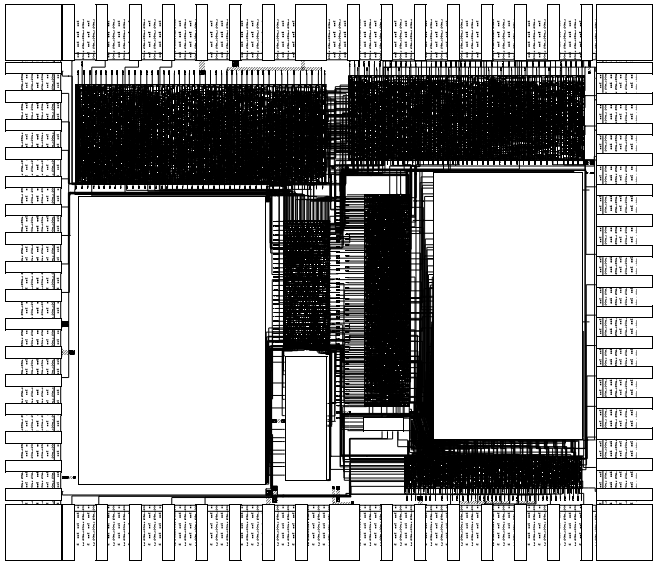

LSB
1.0
0.5
0.0
-0.5
-1.0
0
128
256
384
512
640
768
896
1024
code




Ovfl
Trigger data
Flags and channel
Insert address
Extract address
16+2
ADD
7+5
9+5
9+5
16+2
3 - code generation
ECC decode
ECC decode
ECC decode
ECC and address decode
Threshold enable
9
9
3 to 1 select
AMEM
4 to 2 decode
Offset control
ECC decode
ECC encode
Addr dec
Extracted data
DAC
ADC
LUT
3
MEM
Channel select
66
69
22+3
10
+5 ECC
16
+6 ECC




T1_sum out
Ext clock
Insert addr
Extract addr
To FBC
T1_sums
T1_3-code
3x16
3x3
Filter F1
11
Clock delays
16
Clock control
20
Clock manager
14
14
LMC
3
6
Ext_ser_link
FERMI_address
4
Int_ser_link
Flags 3
Data
Flags
22
3
Read_req
Read_ack
Filter F2
Flags & IC select
12
ECC encoder
4
Analog test pulse
Test pulse generator
Pulse control
Readout controller
5
I/O_control
Data_out
22
14
14
To Ch. ASICs
ADC clock
Syst. clock
Insert addr
Extract addr



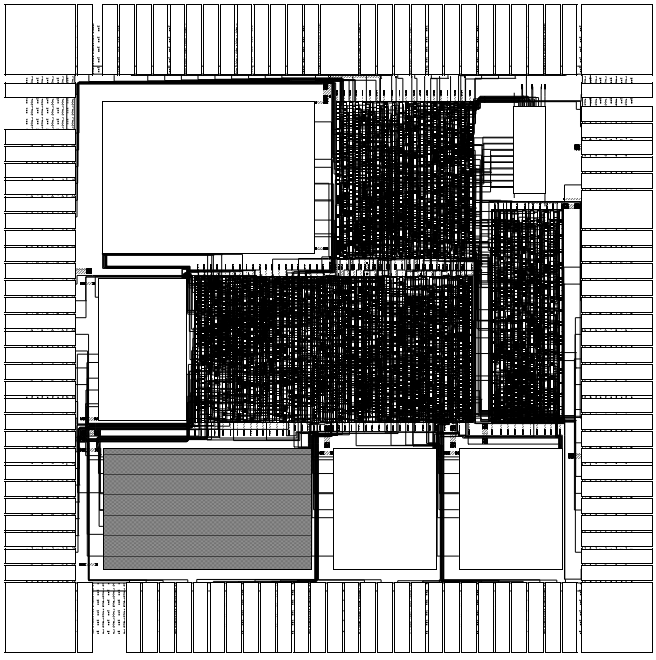


Figure 12