Total Ionizing Dose Effects in a Xilinx FPGA

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We have measured the effects of total ionizing dose on four Xilinx XC4036XL FPGAs. The FPGAs were irradiated at a dose rate of about 0.5 krad/hr. An average total dose of (40 ± 2) krad(Si) was absorbed before the power supply current began to increase and (60 ± 3) krad(Si) was absorbed before the first error occured.

1 Introduction

We have studied the effects of gamma radiation on a field programmable gate array (FPGA). Four XC4036XL-1HQ240C FPGAs from Xilinx were irradiated with a cobalt-60 source.

The XC4036XL consists of an array of configurable logic blocks, which are connected by programmable interconnects, and surrounded by I/O blocks. The configurable logic blocks offer up to a total 36,000 logic gates or up to about 41,000 bits of RAM. The logic and RAM are programmed using additional static configuration memory cells. The FPGA is a low voltage (3.3 V) SRAM design in a 0.35 μm CMOS process. The speed grade of the chip we tested was -1 [1].

The FPGA die was housed in a HQ240C package. This is a 240-pin plastic-molded surface-mount quad flat-pack. The body thickness is 3.4 mm and there is an embedded metal heat slug at bottom of the package.

The dose rate due to ionizing particles at the location of the LAr barrel calorimeter front-end boards has been estimated to be 2 krad/yr. Including a safety factor of four, the dose rate requirement is 8 krad/yr [2]. For the nominal 10 year period, front-end electronics must operate up to a total absorbed dose of 80 krad.

2 Experiment Setup and Dosimetry

A small printed circuit (PC) test board was built. The FPGA was mounted in a socket which was soldered to the PC board. The heat sink on the package was not used. The PC board contained the FPGA, socket, a 40 MHz oscillator, switches, connectors, and a small number of passive components.

The FPGA was configured with the circuit that was used (and is currently being used) to control the switched capacitor arrays on the front-end boards for the module-0 LAr electromagnetic calorimeters [3]. Configuration circuit downloading and monitoring were performed over the parallel port of a personal computer [4]. A description of the error

checking can also be found in reference [4]. The circuit was clocked at 40 MHz. A pulser provided the triggers at a rate of about 10-20 kHz.

A detailed description of the geometry of the radiation test setup can be found elsewhere [5]. The PC board was placed into a rectangular lead enclosure with an aperture. The aperture allowed a direct line of sight from the cobalt-60 source to the FPGA, while the lead provided adequate shielding of the other board components from the radiation source. Inside the lead enclosure, the PC board was positioned within an aluminum box which also contained an aperture to allow a direct line of sight from the source to the FPGA. The aluminum shielded against low-energy bremsstrahlung photons produced by electrons scattering off of the high density lead. The aluminum box also provided a rigid structure to ensure a well defined alignment of the FPGA, dosimeters, and source. This alignment was particularly important since the dosimeters were periodically removed to measure their optical density, and the PC board was removed and replaced during annealing cycles.

The dose rate was determined using Fricke (ferrous sulfate) dosimetry [6]. The procedure for determining the dose rates in the dosimeters and then interpolating to the dose rate in the FPGA silicon die is explained in a previous note [7].

The absorbed dose is different for different materials. We corrected the absorbed dose by calculating the ratio of the energy absorption coefficients, μ_{en}/ρ, in ferrous sulfate (standard Fricke) solution and silicon [8]. For gamma rays from cobalt-60 (average energy 1.25 MeV) the correction to the absorbed dose is

$$\frac{(\mu_{en}/\rho)_{\mathrm{Si}}}{(\mu_{en}/\rho)_{\text{ferrous sulfate}}} = \frac{2.652 \times 10^{-2}}{2.955 \times 10^{-2}} = 0.90. \tag{1}$$

The difference between this correction for Si and SiO_2 is less than 0.4%.

3 Test Procedure

The following test procedure was applied to all four FPGA chips. The FPGA was operated and monitored for about one day prior to irradiation to ensure proper operation. During the first irradiation period, the FPGA was operated continuously without reconfiguration of the circuit, or removing the clock or trigger. The power supply voltage and current were monitored about every three hours. During large changes in the power supply current and during errors, the monitoring of the voltage and current were more frequent. The error register, in the circuit loaded in the FPGA, was monitored continuously by computer control [4]. All errors were time-stamped and automatically recorded in a log file. Alarm messages and status logs were emailed to the experimenters.

After the first error occured, irradiation of the FPGA was continued so as to determine the type and frequency of the errors. When the errors were continuous, the radiation source was removed but the chip was kept under bias. The PC board was then removed from the radiation zone and placed into an oven for two weeks at 50°C. During this time the power supply voltage and current, and oven temperature were monitored. The chip remained under bias in the oven but the configuration circuit was not loaded. If the

configuration circuit is loaded while at 50°C, a large current is drawn and continuous errors occur.

After two weeks of annealing, the PC board was removed from the oven to ambient temperature and the configuration circuit was reloaded. The system was then placed back into the radiation zone and operated for an additional day before the source was activated again. The FPGA was irradiated a second time until continuous errors occured once more.

4 Results

Figure 1 shows the power supply current versus accumulated dose during the first irradiation period. The current began to increase after an average total absorbed dose of (40 ± 2) krad(Si) and the first error occurred after an average total absorbed dose of (60 ± 3) krad(Si). The average absorbed dose values are the weighted means of the absorbed doses for the four chips and the errors are the deviations of the three measurements from the weighted means.

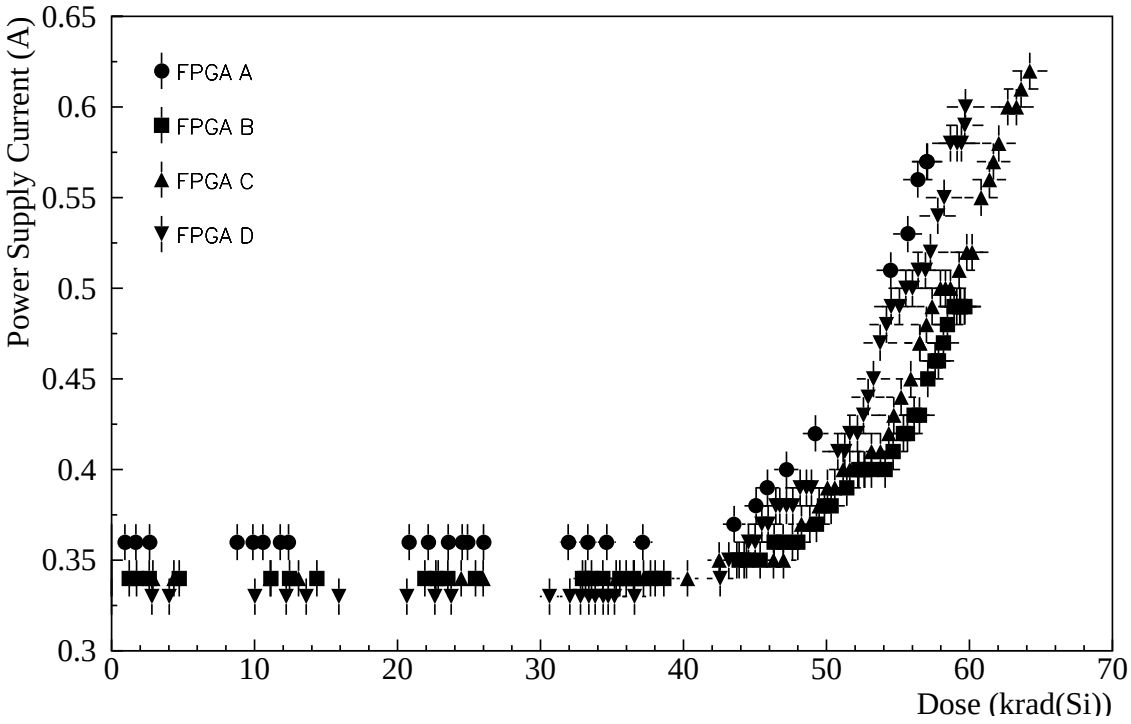

Figure 1: Power supply current versus accumulated dose for FPGA A (circles), FPGA B (squares), FPGA C (triangles), and FPGA D (inverted triangles).

Table 1 shows the results of irradiating the FPGAs until the first errors occured. The first error in the dose rate is due to the error in the determination of the dose rate in the Fricke dosimeters. The second error is an estimate of the error due to the interpolation of the dose rate measured in the dosimeters to the position of the FPGA die. The error in

the integrated time of irradiation is due to the accuracy of measuring the times (±30 s) during which the source was removed during dosimetry measurements. The uncorrected total dose is the dose before applying the material correction in equation 1.

Measurement	*FPGA A*	*FPGA B*	*FPGA C*	*FPGA D*
Uncorrected dose rate (rad/hr)	$536 \pm 2 \pm 9$	$537 \pm 4 \pm 9$	$543 \pm 3 \pm 9$	$497 \pm 6 \pm 8$
Results until the power supply current increased				
Integrated irradiation time (hr)	83.63 ± 0.03	85.43 ± 0.03	84.70 ± 0.03	83.35 ± 0.02
Uncorrected total dose (krad)	$44.8 \pm 0.2 \pm 0.8$	$45.8 \pm 0.3 \pm 0.7$	$46.0 \pm 0.3 \pm 0.7$	$41.4 \pm 0.5 \pm 0.7$
Total absorbed dose (krad(Si))	$40.3 \pm 0.2 \pm 0.6$	$41.3 \pm 0.3 \pm 0.7$	$41.3 \pm 0.3 \pm 0.7$	$37.3 \pm 0.4 \pm 0.6$
Results until the first error occured				
Integrated irradiation time (hr)	117.26 ± 0.03	122.10 ± 0.04	131.54 ± 0.04	132.87 ± 0.03
Uncorrected total dose (krad)	$62.9 \pm 0.3 \pm 1.0$	$65.5 \pm 0.4 \pm 1.0$	$71.4 \pm 0.5 \pm 1.1$	$66.0 \pm 0.8 \pm 1.1$
Total absorbed dose (krad(Si))	$56.6 \pm 0.2 \pm 0.9$	$59.0 \pm 0.4 \pm 0.9$	$64.3 \pm 0.4 \pm 1.0$	$59.4 \pm 0.7 \pm 0.9$

Table 1: Results from the irradiation of the four FPGA chips.

Address sequence errors were the only type of error observed in these tests. This error is flagged when the SCA capacitor addresses have gone out of sequence. Each time an error of this type is detected, the error is cleared by a circuit reset without reloading the configuration circuit.

Figure 2 shows the total number of address sequence errors versus time since the first error occured. After the first error, there appears to be a period of low error rate, followed by a high error rate period, and soon afterwards, continuous errors. The FPGAs received an average additional absorbed dose of about 0.6 krad(Si) during the error period.

Figure 3 shows the power supply current versus time during a two week annealing period at (50 ± 2)°C. The discontinuity in the current for FPGA C after 3.5 days occured during a period in which the chip was removed from the oven for about 30 min. We have no explanation for the increase in the current on the last day of annealing.

During the second irradiation period the FPGAs received an average additional dose of about 5.5 krad(Si), giving an average total absorbed dose during the entire test of approximately 65.8 krad(Si).

Figure 4 shows the power supply current versus time for the entire test. During periods of irradiation (current increasing) the configuration circuit was loaded. During periods of annealing (current decreasing) the configuration circuit was not loaded but the chips were still kept under bias. It should be noticed that the FPGA draws more current when the configuration circuit is loaded and running, independent of radiation effects. When the FPGA was configured a second time for irradiation, the current drawn was immediately higher than for a non-irradiated FPGA.

5 Summary and Discussion

The FPGAs were irradiated with a dose rate of $(476 \pm 2 \pm 8)$ rad(Si)/hr. The current increased after an absorbed dose of about 40 krad(Si). This increase was probably due to

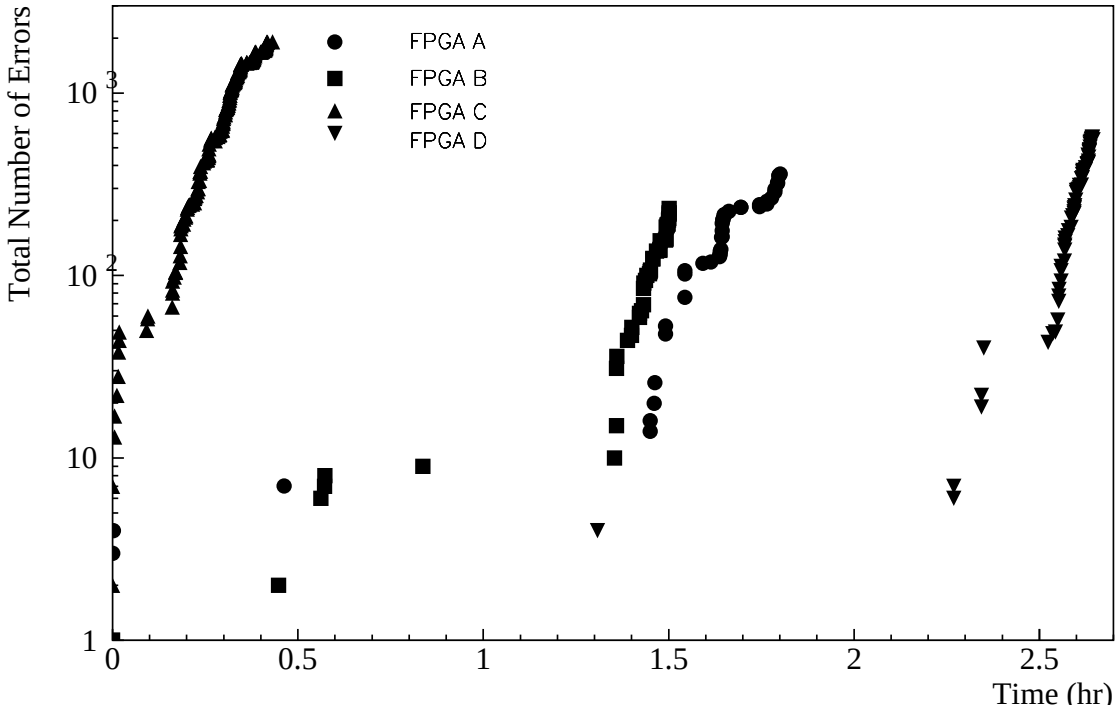

Figure 2: Total number of address sequence errors versus time after the first error occured for FPGA A (circles), FPGA B (squares), FPGA C (triangles), and FPGA D (inverted triangles).

the onset of leakage currents. The first errors occurred after an absorbed dose of about 60 krad(Si). These were soft errors which were reset without reloading the configuration circuit.

A second period of radiation after annealing showed a similar operating behavior to the first irradiation period. The current increased during irradiation and dropped slowly during annealing. A previous test [9] showed that the current still remained substantially high after about four months of self-annealing.

We believe that leakage currents increased until a logic failure occurred. All attempts to download the configuration circuit were successful and hence there was no indication of a failure with the SRAM configuration switches. After irradiation, we looked for increased skew and a change in rise time of the output address signals. No evidence was found for any change and hence the radiation damage did not appear to effect the I/O blocks of the FPGA.

The error rates and annealing behaviors of FPGA C and FPGA D were somewhat different than those of FPGA A and FPGA B. The date code for FPGA C was different, and hence was probably from a different production lot, from that of FPGAs A and B. FPGA D had a third date code, and was probably from yet another production lot. Nevertheless, all four FPGAs behaved similarly during the first irradiation period.

If dose rate effects are negligible for CMOS devices below dose rates of 0.5 krad/hr [10], we could expect Xilinx FPGAs to survive total dose damage for about ten years. This

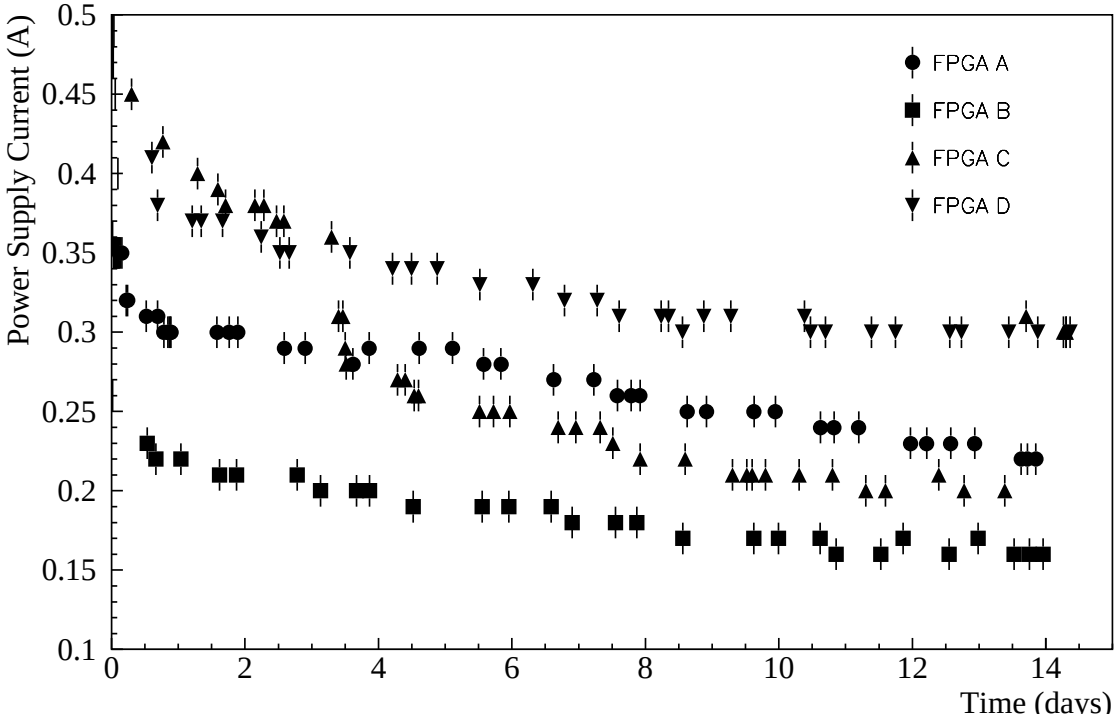

Figure 3: Power supply current versus time during annealing for FPGA A (circles), FPGA B (squares), FPGA C (triangles), and FPGA D (inverted triangles).

prediction allows for a safety factor of about two.

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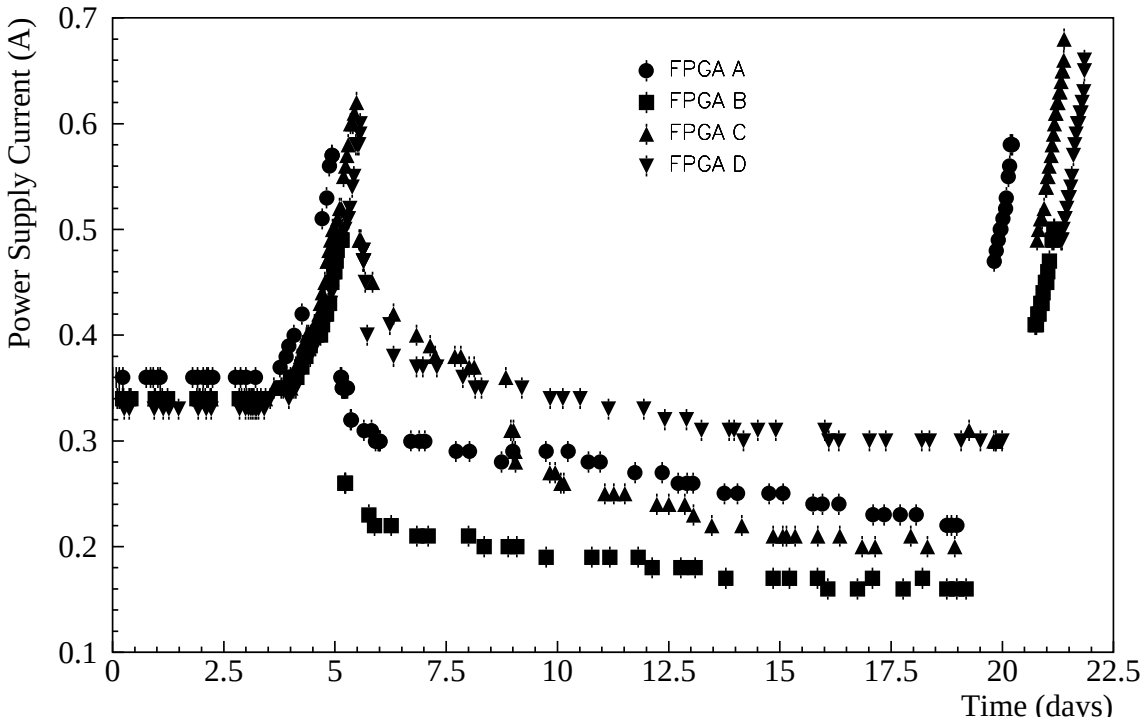

Figure 4: Power supply current versus time during the entire test for FPGA A (circles), FPGA B (squares), FPGA C (triangles), and FPGA D (inverted triangles).

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