	Electrical Tests of SCT Hybrids and Modules

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Electrical Tests of SCT Hybrids and Modules

Abstract

This document aims to describe each of the electrical (readout) tests of SCT hybrids and modules that will be performed during production. A number of test sequences designed to simplify the task at hand are also presented.

The methodology of each test and the subsequent analysis of its data are outlined. A number of possible defect types that can be identified by each test is given, and a table of values to be recorded in the ATLAS SCT production database is defined. In each case an example is included of the ASCII file output by the analysis software and designed to be read into the production database.

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3.23b	2002-12-19		Revisit reformation to ATLAS ID Note. Add test table for Stream Delay test.
3.30	2003-01-06		Numerous corrections and format changes, mostly to the new sections of the text. Also provide separate documentation for the "Warm" and "Cold" hybrid tests.
3.32	2003-01-07		Revise "Acceptance" description for 3PG and RC tests to match what is implemented in SCTDAQ release 3.32
3.34	2003-01-22		Add description of correction for "8fC effect" to the Response Curve definition; Revised description of defects for FullBypassTest; Make reference to developmental algorithm in NO test section; Replace most DB examples by recent ones.
3.37	2003-03-13		Add notes to RedundancyTest noting that the test is automatically skipped when running all modules with SELECT=1; Corrected table of cuts for the 3PG and RC tests; Notes about DB comment generation; Document EndCapHLTT.cpp
3.38	2003-03-19		Raise PARTBONDED cut to 800 ENC; list all channels masked by 3PG test; channels are not masked by the ResponseCurve test.

Table of Contents

1 Introduction

The ATLAS SemiConductor Tracker (SCT) will be composed of a mosaic of 4088 silicon microstrip detector modules: 2112 barrel modules mounted on four cylinders and 1976 end-cap modules mounted on eighteen disks. For the purposes of detector module assembly the SCT collaboration is organised into a number of clusters. As an essential part of the production, thorough Quality Assurance (QA) procedures have been defined for use by the barrel [1] and end-cap [2] communities. Within each cluster, assembly tasks and QA responsibilities are distributed between the member institutes and universities.

This note describes the electrical measurements performed on the detector modules during production. Under the QA scheme, such tests are performed at many points in the production sequence. A basic set of tests has been defined, from which two standard test sequences have been drawn. The short sequence (ConfirmationTest) is optimised for fast execution, focusing on detecting failures that might occur on detector modules. The long sequence (CharacterisationTest) gives a more complete characterisation of the module, to detect more subtle deviations from the specification and provide a reference data set for macro assembly of detector modules onto barrels and end-cap disks.

In addition to this, three long-term tests have been devised. These are performed to provoke infant mortality and to demonstrate the long-term stability of each detector module under nominal operating conditions. The test sequences are designed to monitor failures that might occur and to track the evolution of certain critical parameters.

Electrical tests are performed using the SCTDAQ system as described in Section 2. The results of each test may be uploaded into the SCT Production Database [3], used to trace components, store results from QA procedures and register actions performed on modules during the production. The interaction between SCTDAQ and SCTDB is also outlined in Section 2.

2 *System Overview*

2.1 **The electrical characteristics of the SCT detector module**

An SCT module comprises two planes of silicon microstrip detectors glued back to back. Small angle stereo geometry is used to provide positional information in two dimensions, an angle of 40 mrad being engineered between the axes of the two sides. The barrel module uses two pairs of rectangular detectors with parallel strips to give an active strip length of approximately 12cm. Three designs of different radial geometries are used in the end-cap region: inner, middle and outer modules.

A module is read out by 12 ABCD3TA ASICs [4] mounted on a copper/kapton hybrid circuit. Manufactured in the radiation hard DMILL process [5], each chip provides sparsified binary readout of 128 detector channels. The amplified and shaped input signal is compared to a programmable threshold having two components: a single 8-bit DAC applied across the whole chip, and a channel specific 4-bit DAC designed to compensate for channel-to-channel variations. The resulting hit pattern is transferred into a binary pipeline, 132 cells deep. Upon receipt of a Level 1 Accept (L1A) trigger, the pipeline output is transferred into a de-randomising buffer that can store up to 8 events.

The first chip on each side of the module, designated as the master chip, is responsible for the electrical transmission of data to the read-out system. Within the module a token passing scheme is used to control the transfer of data to the master chip for onward transmission. This scheme incorporates several redundancy options such that, should any single chip fail, the remaining chips can still be read out.

In ATLAS, an optical scheme will be used to communicate with SCT detector modules. In the barrel region the conversion between the optical and electrical domains takes place entirely off the module, hence a full production test of a barrel module may be performed using simple LVDS clock and command signals. In the end-cap module, some components of the optical link are mounted directly on the hybrid leaving the PIN diode receiver and VCSEL diode transmitters to be added by means of an "opto plug-in". To perform a complete functional test of an end-cap module one needs to use an opto plug-in or an electrical simulation thereof. For production testing it is proposed to do the latter.

2.2 *The SCTDAQ system*

During production testing, a set of custom VME modules is used to read out the detector modules. A schematic diagram of the readout system is shown in Figure 1. The CLOAC MASTER module provides the system wide 40.08MHz clock and generates fast commands such as L1A. Fast commands may be generated in response to an external trigger source or as a burst comprising a specified number of triggers at a designated frequency, however for the majority of the electrical tests performed during module production individual triggers are generated in response to VME commands. SLOG distributes the clock and fast command signals generated by CLOAC to up to 12 detector modules. It also generates the slow command data needed to configure the detector modules. MuSTARD receives data from up to 6 detector modules, or 12 data streams, decodes the events and creates histograms the data. Individual events may be transferred to the host computer if more detailed analysis is required. Each SCTLV module provides low voltage power for two detector modules and reads out the NTC thermistors mounted upon the SCT modules. The companion module SCTHV provides detector bias for four detector modules at up to 500V.

The VME crate is interfaced to a PC running Windows NT/2k/XP or Linux, by means of National Instruments' PC-MXI-2-VME interface set[1]. SCT module configuration and data acquisition is performed by the SCTDAQ software package [6]. Static libraries written in C handle the basic communication with the VME boards. Higher level functions are implemented in a small number of C++ classes, linked with the static libraries and some libraries of the ROOT framework [7], to form a shared library.
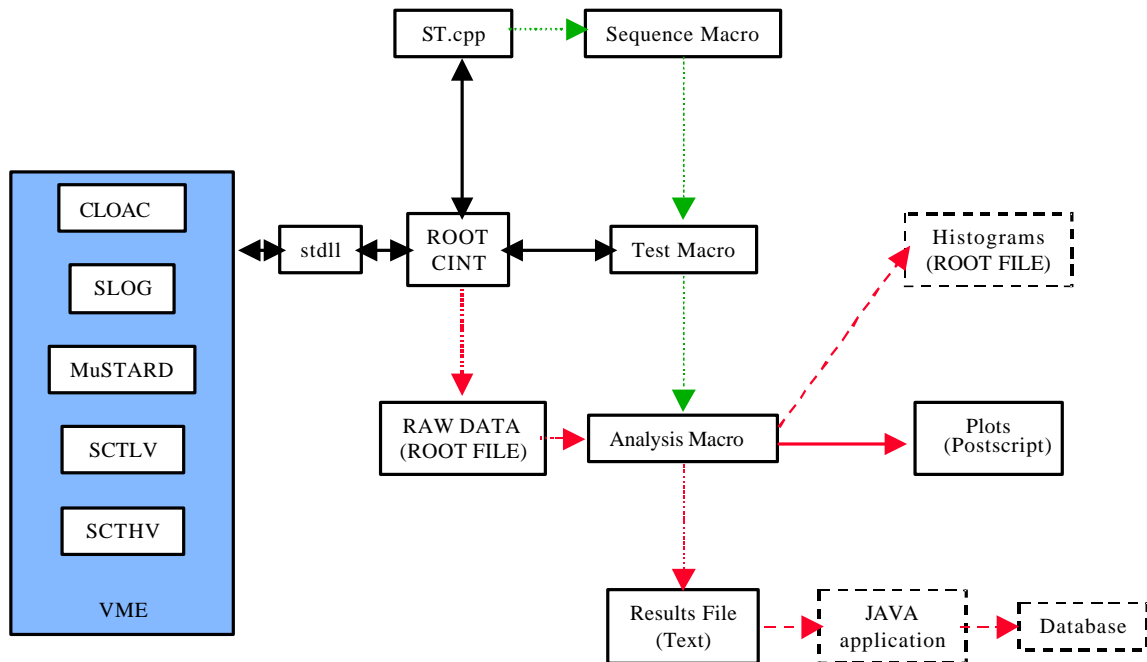
Figure 1: Schematic showing SCTDAQ system

Within ROOT, the system is started by running an interpreted macro that calls upon the functions of the shared library to initialise the VME boards and configure the SCT detector modules to their default operating conditions. Simple tests and configuration changes may be performed directly from the CINT console. Each electrical test has been implemented in the form of a discrete ROOT macro which may be run by pressing a button within the menu system, by running an overall "sequence macro" or by direct user input at the command prompt. At the end of each scan a ROOT file is generated which contains the scan data for each module, records of error and event counters and some module configuration and DCS information.

Analysis of the raw data from each test is performed by a separate root macro that appends results to a text file, one per hybrid or module per day, such that the results of each test in the sequence are kept together in one file. The Java application jSCTDAQ [8], called by the ROOT macro DBUpload.cpp, is used to prepare the data for upload directly into the SCT production database. Many tests also generate results in the form of plots within a postscript file. These may be stored on web server of a cluster's own choice, in which case a link to each plot can be placed into the database entry for the corresponding test. In future the software may be revised to keep a number of the derived histograms for each module together in a separate root file.

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[1] Under Linux, Carlos Lacasta has ported SCTDAQ for use with the BIT3 interface. Similarly John Hill has ported SCTDAQ for use with any single board computer supported by the ATLAS ONLINE VME driver. Although the modifications needed to support these versions have been incorporated into the main SCTDAQ source code, persons wishing to use these platforms are advised to contact the respective author of that port if system specific help is required.

2.3 Test results and the SCT Database

The following table is reproduced from the list of SCT Database table definitions [9].

TESTS: General Details of Tests on Items

Column Name	Type	Description
SER_NO	Long int	Atlas serial no. of item
TEST_NO	Long int	ID no. of test
RUN_NO	Char(80)	Data taking run no.
TEST_NAME	Char(20)	Name of test
TEST_DATE	Date	Date of test
LOCN_NAME	Char(50)	Location of test
INITLS	Char(4)	Initials of user
PASS	Boolean	Passed unconditionally?
PROBLEM	Boolean	Problems encountered?
SUBSYST	Char(1)	Subsystem code
LAST_MOD	Date	Date record last updated
OWNER	Char(30)	Owner institute of the record
Primary Key:	TEST_NO	
Foreign Key:	SER_NO	ITEMS(SER_NO)
Foreign Key:	TEST_NAME	TEST_DESCR(TEST_NAME)
Foreign Key:	LOCN_NAME	LOCNS(LOCN_NAME)
Foreign Key:	INITLS	PERSONS(INITLS)

For each electrical test performed upon a hybrid or module an instance of the above object will be added to the database, hence the serial number, run number, location and tester are always recorded.

Digital tests will set the "PASS" field to "NO" if more than a specified number of defects are found: many of the analogue tests do not make use of this field. The "PROBLEM" field is not used by the electrical test software and is set to "NO" in all cases. The remaining fields shown in the above table are for internal use by the database.

Information specific to each electrical test is recorded in one or more data tables, defect objects and/or raw data files, all of which are linked to the relevant instance of the basic test object described above.

A number of utility tables have been designed to store information that it is desired to record for a number of tests, such as monitored DCS parameters. This has greatly simplified the definition of the tables needed to store the results of each specific test, since all common factors have been removed. The definitions of the utility tables can be found in appendix 1.

In addition to the utility tables, a table has been designed to record the results of each test. These tables are defined in appendix 2. There is a direct link to each table from the relevant section of the text. The list of defects that may be identified by each test are detailed in the test and summarised in appendix 3.

Additional configuration information or more detailed results may be stored in the form of (ASCII) raw data. A list of all database tables specific to the electrical testing of hybrids and modules, showing their implementation status, can be found in appendix 4.

3 Sequences and Optional Extras

3.1 Purpose of the Test Sequences

The electrical measurements performed as part of detector module Quality Assurance are drawn from a pool comprising around 13 component tests. Each test has been designed to determine a certain set of parameters and/or to identify a number of specific defects or failure modes. The full set of measurements demonstrates the complete functionality of a module and provides measurements of all electrical parameters judged important to monitor module quality. Used in conjunction with the SCT database query tool, this information can be used to track points of failure and to evaluate yield statistics. As all measurements and actions performed on a detector module will be registered in the database, failures can be correlated with steps of the assembly and QA sequence.

As mentioned previously, the individual digital and analogue tests described in sections 5 and 6 have been grouped into two test sequences which may be used as part of three long-term tests. The Characterisation Test is outlined in section 3.3 and the Confirmation Test is described in section 3.4. The three long-term tests are outlined in section 3.5 and detailed in section 7. Several tests have been defined which are not part of the standard sequences, since their application is dependent upon the device under test (e.g. IV Curve) or upon the state of the set-up (e.g. Stream Delay Test): these tests are outlined in section 3.2 and detailed in section 4. Finally, section 3.7 gives references to other module test activities that, although beyond the scope of this document, form part of our QA procedures on a sampling basis.

3.2 Standalone Tests – not included in the standard test sequences

The following tests do not apply in all scenarios, hence they have been omitted from the characterisation and confirmation sequences. It is left to the user to run them manually as required by means of the menu system.

- IVCurve.cpp

    This test records the leakage current as a function of the applied detector bias. The bias voltage is increased in discrete steps of typically 25 volts until the requested upper limit is reached. At each step of the voltage ramp the leakage current is measured and the data is stored as a text file for upload to the SCT database and shown graphically as an IV curve.

- StreamDelay.cpp

    Stream Delay is a parameter internal to MuSTARD that adjusts the relative phase between each input data stream (from a detector module) and the system clock. It should be set such that the data is sampled well away from the transition regions. Its value is dominated by system considerations such as cable length; hence this test is usually performed only when setting up a readout system[2]. The stream delay settings should then be copied into the system configuration file such that they are used each time the system is started. It is not necessary to run this test before each test sequence.

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[2] Very rarely, the PHOS4 QUAD delay chips used on MuSTARD may lock incorrectly to the system clock at startup. Under such circumstances each step of its 4 Stream Delay registers will not be equal to the design value of 1nS but ~0.6nS (if the PHOS4 is in "FAST" mode) or ~1.8nS (if it is in "SLOW" mode). If this has happened, the stream delay settings in the configuration file may or may not yield usable sampling of the received data. See section 4.2.4 for a more detailed discussion of these effects.

- Opto Functionality Tests (not yet implemented)

  This measurement will be used to verify the functionality of the optical link components that are mounted on the end-cap hybrid. It does not apply to barrel hybrid or modules.

3.3   CharacterisationTest.cpp

The Characterisation Sequence aims to verify the basic digital functionality of a hybrid or module, and to fully characterise its analogue performance. The results will be used to determine whether a module is of sufficient quality to be used in ATLAS, and will also serve as a reference data set for subsequent measurements at macro assembly sites. The menu system contains a button to start the sequence, which comprises the following tests:

3.3.1   Digital Tests:

- HardReset.cpp

  The module/hybrid is clocked and the power is switched on. Using an oscilloscope connected to monitor points provided on the MuSTARD front panel, the operator must verify that each datalink responds with CLK/2 and that, after the chips have been configured, the clock feedthrough signal stops. The analogue and digital currents are then recorded. Finally Hard Reset is issued to bring back the CLK/2 signal. This test verifies that the Clock, Command and Hard Reset signals are received correctly, that the chips can be configured and that the current consumption is reasonable. The test will identify modules/hybrids with severe failures and/or cases where devices have been connected incorrectly. Every module must pass this test without error. This is the only test that would normally require operator intervention.

- RedundancyTest.cpp

  The chips are configured to return the contents of the Mask Register and a burst of triggers is issued for each of the Primary and Redundant Clock and Command options. Prior to each event, a different bit pattern is loaded in the Mask Register such that consecutive events are not the same. By comparing the received data with expectation it is verified that both the Primary and Redundant Clock and Command signals are received correctly and that the top address bit of each chip changes as the Clock/Command source is varied, as specified in the module design. This test will identify modules/hybrids with faulty command reception or addressing errors. Modules/hybrids with such defects would be considered to have failed pending further investigation and possible rework.

- FullBypassTest.cpp

  A trigger burst is recorded with the module/hybrid programmed to each of a number of different configurations, sufficient to exercise all data/token passing links between the chips. In each case the chips are configured to return the contents of the Mask Register such that the expected data is accurately known. The test is repeated across a range of digital supply voltages to determine the minimum value of the digital supply voltage needed for the correct functionality of each of the data/token passing links. Any link that did not work at the nominal supply voltage of 4.0V, which could not be identified as being due to a missing wirebond and subsequently repaired, would cause a module/hybrid to be rejected.

- PipelineTest.cpp

  For this test, a Soft Reset command is sent to reset the pipeline followed a certain number of clock periods later by a Pulse Input Register command and L1A trigger. In this way, a known pattern is injected into a given location in the pipeline. By varying the distance between the Soft Reset and Pulse Input Register commands it can be verified that each of the eleven blocks within the pipeline is free of defects. The pipeline is scanned twice: once with all channels enabled to identify dead cells and dead channels; once with all channels disabled to identify stuck cells and stuck channels. Modules/hybrids with a large number of dead or stuck cells or channels will be rejected.

3.3.2 Analogue Tests:

- StrobeDelay.cpp

  This scan is performed to determine the correct Strobe Delay setting, corresponding to the timing of the charge injection pulse, to be used during the Analogue Tests.

- ThreePointGain.cpp (untrimmed)

  Threshold scans are taken for three injected charges to facilitate a quick measurement of gain, noise and the discriminator offset. Pathological channels are categorised as FAULTY if the defect would result in the channel having a reduced but non-zero detection efficiency in ATLAS, or as LOST if the defect would result in the channel having zero efficiency:

    Lost: Dead, Stuck, Unbonded or Noisy channels

    Faulty: Inefficient, Low Gain or Partially Bonded channels

  Modules/hybrids having any chips with abnormal gain or high noise will be rejected and put aside for potential rework, as will those with large numbers of pathological channels.

- TrimRange.cpp

  For each of the four possible TrimRange settings, a series of Threshold scans are performed for a subset of the sixteen possible TrimDAC settings, all with 1fC injected charge. For each TrimRange setting a straight line is fitted to the data for each channel to characterise the TrimDAC response and to determine the TrimDAC slope. The number of trimmable channels and the spread of the resultant trimmed thresholds are also recorded. The optimised TrimDAC settings and a list of (untrimmable and noisy) channels to be masked are produced for use in the subsequent analogue tests. The chips used to build modules will have been selected such that all channels may be trimmed using TrimRange 0 or 1. Modules for which less than 99% of the channels meet this specification will be rejected and put aside for potential rework, as will those where a particular TrimRange has a slope other than that expected.

- ResponseCurve.cpp

  Threshold scans are performed for a series of input charges and, for each channel, an appropriate function is fitted to the resulting response curve. From this the Gain, Noise and discriminator Offset are extracted. The parameters from the fit are stored since they describe the correspondence between the Threshold, in mV, and input charge, in fC. The categorisation of pathological channels is repeated as described for the Three Point Gain measurement. Modules/hybrids with a large number of pathological channels will be rejected.

- NO.cpp

  A high statistics Threshold scan is performed at the nominal ATLAS trigger rate of 100kHz, without any injected charge, to determine the Noise Occupancy of each channel as a function of Threshold. The analogue and digital current consumption as a function of Threshold is recorded.

  Channels with high Noise Occupancy will be added to the list of masked (lost) channels.

- Timewalk.cpp

  This test performs a series of Strobe Delay scans with the Threshold set to 1 fC, varying the input charge from 1.25 to 10 fC. In each case a fit is made to the rising edge of the pulse to determine the Strobe Delay value needed to obtain 50% occupancy. The Timewalk is defined as the time variation in the crossing of a threshold of 1fC over a signal range of 1.25 to 10.0fC. This parameter is calculated and recorded.

3.4 *ConfirmationTest.cpp*

The Confirmation Sequence aims to verify, as quickly as possible, that the performance of a hybrid or module has not deteriorated, perhaps as a result of handling or shipping. The test sequence is a sub-set of the Characterisation Sequence described in Section 3.3.

The digital tests that are part of this sequence are chosen to help identify damaged wirebonds and the analogue tests, whilst sufficient to demonstrate that the basic performance is as expected, avoid the more time consuming tasks such as trimming or a measurement of the noise occupancy. The menu system contains a button to start the sequence, which comprises the following tests:

3.4.1 Digital Tests:

- HardReset.cpp
- RedundancyTest.cpp
- FullBypassTest.cpp
- PipelineTest.cpp

3.4.2 Analogue Tests:

- StrobeDelay.cpp
- ThreePointGain.cpp (trimmed or untrimmed, as appropriate)

3.5 *Long-term tests*

Three long-term tests with electrical readout are performed as part of the Barrel Hybrid/Module Quality Assurance scheme:

- HybridLTT.cpp

  The hybrid is operated at an elevated temperature to provoke infant mortality of its components, notably the ASICs. Initially the duration of the test will be 90 hours, however this time may be adjusted in response to production experience. Voltages, currents, temperatures and noise occupancy are monitored throughout the test. This test sequence must be performed on every readout hybrid before it may be accepted for use in a detector module.

- HybridColdTest.cpp

  Running at the nominal ATLAS SCT operating temperature, each hybrid is tested to demonstrate its correct, stable operation at low temperature. Initially the duration of this test will be 10 hours, however this time may be adjusted in response to production experience. Voltages, currents, temperatures and noise occupancy are monitored throughout the test. This test sequence must also be performed on every readout hybrid before it may be accepted for use in a detector module.

- ModuleLTT.cpp

  Running at the nominal ATLAS SCT operating temperature, each module is tested to demonstrate its correct, stable operation at low temperature, including the stability of the leakage current in the silicon sensors. Initially the duration of this test will be 24 hours, however this time may be adjusted in response to production experience. Voltages, currents, temperatures and noise occupancy are monitored throughout the test. This test sequence must be performed on every module before it may be accepted for use in ATLAS.

3.6   EndCapHLTT.cpp

This sequence provides the full test sequence needed to test endcap hybrids at those institutes responsible for hybrid burn in. The macro is designed for use with a climate chamber of chiller that has been independently programmed to give the correct temperature sequence, and the user should start both sequences at the same time to ensure that the two remain in step. It is intended that the sequence be left running with minimal manual intervention.

The test comprises five parts:

1. A characterisation sequence, run WARM (~55 ^{O}C).
2. A long term test of duration (90 hours - length of step 1), again run WARM (~55 ^{O}C). The test sequence will abort if and hybrid temperature exceeds 60 ^{O}C.
3. A "long term test" of 1.5 hours duration. Currents and temperatures are monitored as the hybrids are taken down in temperature ready for the next test. The timing includes a generous allowance for the system to reach thermal equilibrium. The test sequence will abort if any hybrid temperature exceeds 60 ^{O}C.
4. A characterisation sequence, run COLD (~0C).
5. LTT for (4 hours – duration of step 4). The test sequence will abort if any hybrid temperature exceeds 30 ^{O}C, as may be expected at the end of the test.

If any test should abort, the power is turned off and the sequence will be ended.

3.7   Other Electrical Tests

In addition to the tests performed on every SCT detector module, some modules will be subjected to extra tests. The number of the modules to be tested in this way is strongly dependent upon the resources available and a different fraction will be set for each of the tests. The following investigations are planned to be part of our Quality Assurance scheme on a batch-sampling basis:

- Laser Efficiency Scan (not yet implemented)
- Beta Source Scan (implemented by Pavel Reznicek of Charles University, Prague [10])
- Beam Tests (SPS – H8 beam line [11])
- Proton Irradiations (PS - T7 beam line [12])

3.8   The Format of the Results File

Results from each test are appended to a file **sctvar\results*serialnumber*_YYYYMMDD.txt**.
For example:

sctvar\results\20220170100016_20010821.txt

The following tag is used to indicate the start of a new section, corresponding to a new test:

```
#
%NewTest
```

This is followed by a section containing information stored in the basic test entity:

```
#
SERIAL NUMBER : 20220170100016
TEST MADE BY  : pwp
LOCATION NAME : RAL
Run number    : 256-11
TEST_DATE     : 09/08/2001
PASSED            : YES
PROBLEM       : NO
```

Next comes a section describing the IP name of the host computer, the software version number and the time of the test, corresponding to the utility table TSTDAQINFO:

```
#
%DAQ_INFO
#
#HOST
"HEPNTW124"
#VERSION
"3.11"
#DUT
"Barrel Module"
#TIME
"18:15:18"
```

The next section gives the monitored DCS values, corresponding to the utility table TSTDCSINFO:

```
#
%DCS_INFO
#
#T0   T1
25.5  26.3
#VDET IDET
350   1.220
#VCC  Icc
3.500 790
#VDD  IDD
4.00  535
#TIME_POWERED
.
```

Depending upon the test which has been executed, there may now follow a section giving details of the number of scans used to make a measurement and the corresponding fixed parameter used for each of those scans. This information is stored in the utility table TSTSCANINFO. The following example lists the number of scans and charges used to make a three point gain measurement:

```
#
%SCAN_INFO
#
#POINT TYPE
"QCAL (fC)"
#N_POINTS
3
#POINTS
1.50  2.00   2.50   .      .      .      .      .
.      .      .      .      .      .      .      .
```

The actual results of the test are summarised in the following section, corresponding to the table specific to that test. By way of an example, here is the format used to list the results of the StrobeDelay test:

```
%StrobeDelay
#
#DELAY
#M0 S1  S2  S3  S4  E5
-1  -1  -1  -1  16  17
#
#M8 S9  S10 S11 S12 E13
17  15  16  16  16  18
#
```

A list of defects is generated if any defects were found by the test. The types of defect that are identified by each test are described in the corresponding section of this document and summarised in appendix 3. Each defect is prefaced by the tag "%Defect".

Here is a list of defects found by the StrobeDelay test:

```
%Defect
DEFECT NAME   : SD_LO
FIRST CHANNEL : 0
LAST CHANNEL  : 127
#
%Defect
DEFECT NAME   : SD_HI
FIRST CHANNEL : 128
LAST CHANNEL  : 255
#
#
#2 defects found
#
```

Now we list any raw data files which are to be associated with the test[3].

```
%TEST Rawdata
FILENAME      : D:\sctvar\results\20220170100016_rc_246-12.txt
```

There are two other types of valid SCT production database objects that may be generated by the electrical test software. Comments may be added to the results file in the event that an error occurred during the test. This is done by the Long Term Test: if the test should be stopped before the scheduled end, the reason for its failure will be stated in the form of a comment.

```
%Comment
COMMENT         : Test failed due to High Voltage Trip
```

Finally, at the discretion of the user, any PS files generated by a test may be listed such that they will appear in the SCT production database in the form of web links.

```
%Web link
DESCRIPTION   : Plots (postscript)
URL           : http://my.server/~mydir/myscript.pl?file=filename.ps
```

This is intended such that a database user can have direct access to the plots, however this requires that each test site or cluster chooses to store its plots on a publicly accessible web server, and provides a suitable

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[3] Although only one file of up to 32k may be uploaded to the SCT DB, the java upload application will create a zip file containing one or more raw data files and then upload this to the SCT DB.

script to locate and return the requested plot. This functionality must be enabled by the user, who does so by editing the value of the parameter WEB_KEY in the file sctdaq/macros/parameters.h.

Further examples are given throughout the remainder of the document.

4 *Description of Standalone Tests*

4.1 *IVCurve.cpp*

This test has been designed for users of the SCTHV high voltage power supply module. Those without access to this module may wish to perform a similar test using other hardware. If the results are stored in the same format, they may still be uploaded to the database.

4.1.1 Method

A menu is presented from which a number of options for the IV curve may be selected:

```
Record IVCurve to which upper voltage:
    0 - don't bother
    1 - 200V in 10V steps, 10s wait, end at 200V
    2 - 350V in 19V steps, 10s wait, end to 200V
    3 - 500V in 10V steps, 10s wait, end to 200V (estimate 13min 40sec)
    4 - 500V in 25V steps, 08s wait, end at 200V (estimate 04min 25sec)
    5 - 500V in 25V steps, 04s wait, end at 200V (estimate 03min 05sec)
    6 - 500V in 25V steps, 04s wait, ramp down and SWITCH OFF HV
    7 - 200V in 25V steps, 04s wait, end at 200V
    8 - 350V in 25V steps, 04s wait, end to 200V
        (Time estimates assume that ramp rate 2 is selected.)
```

For the initial production test of each SCT module, option 4 is recommended. Option 6 is provided for users wishing to demonstrate that an SCT hybrid may withstand the full bias voltage of 500V. It is recommended that the number of times for which the module bias is taken to 500V should be kept as low as is possible: to this end options 7 and 8 have been provided. A firmware current limit of 100 μA, set high to allow for charging currents, is imposed throughout the sequence. If this limit is exceeded, the voltage will trip off. Once the requested voltage has been reached, the current is recorded after the desired setting (wait) time has elapsed. In addition, should a module draw more than 10 μA current after the alloted settling time, the voltage applied to that module will not be raised further.

At any point during the test, the user may push the ABORT button to cancel the test and ramp down the high voltage. If the STOP button is pressed the high voltage will ramp directly to the chosen end point, typically 200V. During production testing this test would usually be performed before the chip bias has been applied but there may be exceptions to this rule, hence it is necessary to record the voltages supplied to, and the currents drawn by, the hybrid. This is achieved by sampling all monitored DCS parameters when the bias voltage has reached its highest point. The information is recorded within an instance of the database table TSTDCSINFO.

4.1.2 Analysis

If a current drawn by a module exceeds the lower limit of 10μA, the defect IV_LIMIT is recorded. If the high voltage supply connected to a module trips off, the defect IV_TRIP is recorded.

4.1.3 Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures
TSTMODIV: leakage currents at 150V and 350V

DEFECTS:

Defect	First Channel	Last Channel
IV_LIMIT	0	1535
IV_TRIP	0	1535

RAW DATA:

IV_DATA (mandatory)

4.1.4 Acceptance

In the event that there should be a High Voltage Trip during the test the PASS field will be set to "NO", otherwise the PASS field will be set to "YES". The database reporting structure should also provide the possibility to set stricter acceptance cuts on the range of acceptable detector bias current values, and to compare values against the sum of the currents drawn by the four detectors before assembly into a module.

4.1.5 Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:10:41"
#
%DCS_INFO
#
#T0    T1
20.0   20.0
#VDET  IDET
500    0.943
#VCC   ICC
0.00    10
#VDD   IDD
0.00    30
#TIME_POWERED
.
#
%DetModIV
#
TEMPERATURE   : 20.0
I LEAK 150    : 0.482
I LEAK 350    : 0.779
#I LEAK 500   : 0.943
#No defects found!
#
%TEST Rawdata
FILENAME      : D:\sctvar\results\20220330200011_iv_20030121_171041.txt
%Web link
DESCRIPTION   : Plots (postscript)
```

URL   :
http://hepunx.rl.ac.uk/atlassct/cgibin/getfile.pl?file=20220330200011_IVCurve_20030121_171041.ps
#

4.2   StreamDelay.cpp

The hybrid or module is configured as described below to return the pattern stored in the mask register, chosen to give 100% occupancy. The stream delay setting is varied to determine the region(s) where data may not be received correctly.

4.2.1   Method

<table>
<tr><td rowspan="20">SETTINGS</td><td rowspan="7">Configuration</td><td>Master/Slave/End</td><td>M</td><td>S</td><td>S</td><td>S</td><td>S</td><td>E</td><td>M</td><td>S</td><td>S</td><td>S</td><td>S</td><td>E</td></tr>
<tr><td>Edge Detect</td><td colspan="12" align="right">OFF</td></tr>
<tr><td>Data Compression</td><td colspan="12" align="right">X1X</td></tr>
<tr><td>Mode</td><td colspan="12" align="right">MASK + Data Taking Mode</td></tr>
<tr><td>Select</td><td colspan="12" align="right">0</td></tr>
<tr><td>Masked Channels</td><td colspan="12" align="right">None</td></tr>
<tr><td rowspan="8">DACs</td><td>Ipreamp</td><td colspan="12" align="right">220μA</td></tr>
<tr><td>Ishaper</td><td colspan="12" align="right">30μA</td></tr>
<tr><td>Threshold DAC</td><td colspan="12" align="right">500mV</td></tr>
<tr><td>Calibration DAC</td><td colspan="12" align="right">10mV (1.0fC)</td></tr>
<tr><td>Delay Register</td><td colspan="12" align="right">-</td></tr>
<tr><td>TrimRange</td><td colspan="12" align="right">0</td></tr>
<tr><td>TrimDAC</td><td colspan="12" align="right">0</td></tr>
<tr><td rowspan="2">TRIGGER</td><td>Sequence</td><td colspan="12" align="right">Full Configuration
+ Soft Reset
+ 129 BCO delay + L1A</td></tr>
<tr><td>Frequency</td><td colspan="12" align="right">-</td></tr>
<tr><td>LOOPS</td><td>Stream Delay</td><td colspan="12" align="right">0 - 24</td></tr>
<tr><td>nTriggers</td><td></td><td colspan="12" align="right">100</td></tr>
</table>

4.2.2   Analysis

When data is received correctly, MuSTARD will decode full occupancy for all channels. When the Stream Delay is set such that MuSTARD samples the data too close to the rising or falling edge of the bit-stream, the data will not be decoded correctly and the occupancy will fall to zero. The edges of the region with zero occupancy are fitted to identify the forbidden values of the Stream Delay. The optimal value of the delay is chosen as being 12 stream delay steps (approximately 12 ns) away from the centre of the forbidden region.

4.2.3   Database

Since the optimal Stream Delay setting is a property of the readout system rather than the module, the results of this test will not be entered in the SCT database. However, the test occurs as an entry in the results file.

4.2.4   **Hardware Notes**

Very rarely, the PHOS4 QUAD delay chips used on MuSTARD may lock incorrectly to the system clock at startup. Under such circumstances each step of its 4 Stream Delay registers will not be equal to the design value of 1nS but ~0.6nS (if the PHOS4 is in "FAST" mode) or ~1.8nS (if it is in "SLOW" mode). If this has happened, the stream delay settings in the configuration file may or may not yield usable sampling of the received data.

To check the operation of the 3 PHOS4 chips in the MuSTARD, perform a Stream Delay scan and observe that the transition regions occur at the expected delay settings. Note that in "SLOW" mode there will be 2 narrow transition regions, while in "FAST" mode there may be no transition region, or a single region that is shifted and wider than expected. Note also that any such effects occur in blocks of 4 streams: it is possible (but very rare) that streams [0:3] are "FAST", [4:7] are "SLOW", and [8:11] "NORMAL". Power cycling the VME crate usually cures the problem.

A hardware and firmware fix for these effects has been found, but there are no plans to implement it for the many MuSTARDs in use throughout the Atlas community, in view of the disruption that would be incurred, and because it does not appear to be a serious problem. Any MuSTARD found to be particularly susceptible to this problem can have its PHOS4 chips replaced. Contact Maurice Goodrick for further information.

5 *Description of Digital Tests*

5.1 *HardReset.cpp*

5.1.1 Method

- The power is cycled such that all chips return to the power on condition. With the aid of an oscilloscope and following the guidance given by the software, the user must verify that each Master chip outputs clock divided by 2. Once this has been completed the currents I_{cc} and I_{dd} are recorded (ICC_NOCONFIG, IDD_NOCONFIG).

- A series of configuration commands is issued to set the clock feedthrough bit high and to program all DACs to nominal values as shown in the table below. The user is prompted to confirm that output of clock/2 by each Master chip has stopped. The currents I_{cc} and I_{dd} drawn in this configuration are recorded within an instance of the TSTDCSINFO table.

- The HARD RESET signal is issued. The user is prompted to check that once more each master chip outputs clock/2.

- The clock is momentarily turned off, and the analogue and digital currents I_{cc} and I_{dd} are recorded (ICC_NOCLOCK, IDD_NOCLOCK).

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E
		Edge Detect												ON
		Data Compression												01X
		Mode											Data Taking Mode
		Select												0
		Masked Channels												None
	DACs	Ipreamp												220µA
		Ishaper												30µA
		Threshold DAC												100mV
		Calibration DAC											10mV (1.0fC)
		Delay Register												-
		TrimRange												0
		TrimDAC												0

5.1.2 Analysis

If either datalink should fail to output the clock/2 signal upon power up, that will be recorded as the defect HR_NOCLK. If clock/2 output does not cease upon transmission of the configuration sequence, the defect HR_NOCON is recorded. Finally, if clock/2 does not return after the HARD RESET signal, that is recorded as the defect HR_NORST.

5.1.3 Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information

TSTDCSINFO: monitored voltages, currents and temperatures

TSTHYBRESET: digital and analogue currents when not configured or when clock interrupted

DEFECTS:

Defect	First Channel	Last Channel
HR_NOCLK	Link * 768	((Link+1) *768) -1
HR_NOCON	Link * 768	((Link+1) *768) -1
HR_NORST	Link * 768	((Link+1) *768) -1

5.1.4 Acceptance

None of the defects found by this test are allowable on production modules, hence the "PASS" field will be set to "NO" if any defects are found. The database reporting structure should also provide the possibility to set acceptance cuts on the range of allowable current values Icc and Idd in each of the three cases.

5.1.5 Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:16:02"
#
%DCS_INFO
#
#T0    T1
27.0   27.0
#VDET  IDET
200    0.543
#VCC   ICC
3.50    950
#VDD   IDD
4.00    490
#TIME_POWERED
.
#
%HardReset
#
#NOCONFIG     ICC     IDD
        80     490
#NOCLOCK      ICC     IDD
       950     220
#No defects found!
```

5.2 RedundancyTest.cpp

The hybrid or module is configured as described below by use of each clock/command pair. Since this test also aims to check the integrity of command reception, one of a number of defined mask patterns is written to each chip prior to each L1A trigger. Consecutive events use different mask patterns.

Note that this test is skipped automatically if SELECT is set to 1 for all devices under test. This is consistent with the use of test sequences to test endcap hybrids/modules when optical readout (or emulation thereof) is not available.

5.2.1   Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E
		Edge Detect												OFF
		Data Compression												X1X
		Mode								MASK + Data Taking Mode				
		Select												(variable)
		Masked Channels								(variable) - SEE BELOW				
	DACs	Ipreamp												220µA
		Ishaper												30µA
		Threshold DAC												500mV
		Calibration DAC												10mV (1.0fC)
		Delay Register												-
		TrimRange												0
		TrimDAC												0
	TRIGGER	Sequence								Full Configuration + Soft Reset + 129 BCO delay + L1A				
		Frequency												-
SCANS	LOOPS	1 – SELECT												0,1
		2 – MASK								Mask #1, #2				
	nTriggers													100

The mask patterns to be used are as follows:

1. a sequence of 010101…01
2. a sequence of 101010…10

Soft Reset is issued a specified number of BCOs before each L1A to ensure that each event is shifted through the same cells of the pipeline. In this way any channel affected by a dead cell in the pipeline can only have zero occupancy, and any difference in the occupancy of a channel for each setting of SELECT must have been caused by addressing or command reception errors.

5.2.2   Analysis

Each channel is categorised according to occupancy as follows:

nhits $_0$ (select = 0)	nhits $_1$ (select = 1)	
50	50	Good channel
100	100	Stuck channel
0	0	Dead channel (not yet able to resolve if pipeline or mask defect)
50	0 or 100	ID4 addressing error when select = 1
0 or 100	50	ID4 addressing error when select = 0
50	$0 < n < 100$	Command reception is not reliable when select = 1
$0 < n < 100$	50	Command reception is not reliable when select = 0
other	other	Command reception is never reliable

During the second stage of the analysis the numbers of channels of each chip which fall into each of the above categories is tallied leading to the categorisation of each chip as shown below. All failures are recorded as defects.

```
IF ((nch_good>120) AND (remainder STUCK OR DEAD))
     PASS code 0
ELSE IF (nch_addressing_error_0>120)
     FAIL code 1 (defect CLK_ADDR0)
ELSE IF (nch_addressing_error_1>120)
     FAIL code 2 (defect CLK_ADDR1)
ELSE IF (nch_command_error_0>120)
     FAIL code 3 (defect CLK_COM0)
ELSE IF (nch_command_error_1>120)
     FAIL code 4 (defect CLK_COM1)
ELSE FAIL code 5 (defect CLK_ERROR)
```

5.2.3   Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information

TSTDCSINFO: monitored voltages, currents and temperatures

DEFECTS:

Defect	First Channel	Last Channel
CLK_ADDR0	Chip * 128	((Chip+1) * 128) -1
CLK_ADDR1	Chip * 128	((Chip+1) * 128) -1
CLK_COM0	Chip * 128	((Chip+1) * 128) -1
CLK_COM1	Chip * 128	((Chip+1) * 128) -1
CLK_ERROR	Chip * 128	((Chip+1) * 128) -1

5.2.4 Acceptance

None of the defects found by this test are allowable on production modules, hence the "PASS" field will be set to "NO" if any defects are found.

5.2.5 Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533-7
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:18:07"
#
%DCS_INFO
#
#T0     T1
27.0    28.0
#VDET   IDET
200.0   0.84
#VCC    ICC
3.50    950
#VDD    IDD
4.00    500
#TIME_POWERED
.
.
#
%RedundancyTest
#
#RedundancyTest Summary - not for the database
#chip pass good stuck dead adr0 adr1 com0 com1 com
# 0  1  128    0    0    0    0    0    0    0
# 1  1  128    0    0    0    0    0    0    0
# 2  1  128    0    0    0    0    0    0    0
# 3  1  128    0    0    0    0    0    0    0
# 4  1  128    0    0    0    0    0    0    0
# 5  1  128    0    0    0    0    0    0    0
# 6  1  128    0    0    0    0    0    0    0
# 7  1  128    0    0    0    0    0    0    0
# 8  1  128    0    0    0    0    0    0    0
# 9  1  128    0    0    0    0    0    0    0
#10  1  128    0    0    0    0    0    0    0
#11  1  128    0    0    0    0    0    0    0
#No defects found!
```

5.3   *FullBypassTest.cpp*

The module is programmed to each possible configuration with regard to the routing of token and data between the chips. Since the irradiation programme has shown that different chips can have different susceptibilities to radiation damage effects with regard to the token passing, this test is performed over a range of digital voltages, Vdd. In this way the minimum value of Vdd required for the correct operation of each bypass link can be determined, and any inherent difference in the performance of the various links is known upon production.

The number of configurations to be tested is greater for forward hybrids than for barrel hybrids since more redundancy links have been implemented in the forward design.

5.3.1   Method

SETTINGS	Configuration	Master/Slave/End	(variable) SEE BELOW
		Edge Detect	OFF
		Data Compression	X1X
		Mode	MASK + Data Taking Mode
		Select	0
		Masked Channels	None
	DACs	Ipreamp	220μA
		Ishaper	30μA
		Threshold DAC	500mV
		Calibration DAC	10mV (1.0fC)
		Delay Register	-
		TrimRange	0
		TrimDAC	0
	TRIGGER	Sequence	L1A
		Frequency	-
SCANS	LOOPS	1 – Vdd	4.0, 3.9, 3.8, 3.7, 3.6, 3.5
		2 – Configuration	Barrel hybrid or module: cases 0 – 35 Forward hybrid or module: cases 0 – 62
	nTriggers		100

5.3.2   Analysis

For each configuration, the number of dead channels of each chip is tallied. Chips having more than 120 dead channels are considered to have returned no data, otherwise they are considered to have returned good data. This matrix is then compared with expectation to determine the minimum value of Vdd needed for the correct operation of each bypass link.

A PASS is recorded if all token/data links function correctly at 4.0V. A PROBLEM is recorded if any token/data links fail at lower voltages. Any token/data link that fails will be recorded as a DEFECT, irrespective of the voltage at which this occurs. Each defect will be accompanied by a database comment giving more information about the defect.

Vdd_min will be recorded as 10.0V in the case where a token/data link is not functional at 4.0V. If a link cannot be tested due to a failure elsewhere in the chain, Vdd_min will be recorded as 0V.

5.3.3 Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information

TSTDCSINFO: monitored voltages, currents and temperatures

TSTHYBBPASS: minimum Vdd required for operation of each token/bypass link

DEFECTS:

Defect	First Chan	Last Chan
TOKEN	Chip * 128	((Chip+1) * 128) -1
RTOKEN	Chip * 128	((Chip+1) * 128) -1

5.3.4 Acceptance

A global "PASS" will be recorded if no defects are found.

5.3.5 Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533-1
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:18:00"
#
%DCS_INFO
#
#T0    T1
27.0   28.0
#VDET  IDET
200.0  0.84
#VCC   ICC
3.52   930
#VDD   IDD
3.50   440
#TIME_POWERED
.
```

```
#
%FullBypassTest
#
#NConfigs  37
#Vdd = 4.0 - 3.5
#
#Vmin
#token  r_tkn   token   r_tkn
#M0             S1
3.50    3.50   3.50    3.50
#
#S2             S3
3.50    3.50   3.50    3.50
#
#S4             E5
3.50    0.00   0.00    3.50
#
#M8             S9
3.50    3.50   3.50    3.50
#
#S10            S11
3.50    3.50   3.50    3.50
#
#S12            E13
3.50    0.00   0.00    3.50
#
#Comment
#M0             S1
"Minimal tested"      "Minimal tested"       "Minimal tested"       "Minimal tested"
#S2             S3
"Minimal tested"      "Minimal tested"       "Minimal tested"       "Minimal tested"
#S4             E5
"Minimal tested"       "Not Tested"   "Not Tested"   "Minimal tested"
#M8             S9
"Minimal tested"      "Minimal tested"       "Minimal tested"       "Minimal tested"
#S10            S11
"Minimal tested"      "Minimal tested"       "Minimal tested"       "Minimal tested"
#S12            E13
"Minimal tested"       "Not Tested"   "Not Tested"   "Minimal tested"
#No defects found!
```

5.4   *PipelineTest.cpp*

The cells of the ABCD3T pipeline are tested in order to identify any cells which may permanently output zero (dead) or one (stuck). (Although the pipeline has already been tested during wafer probing, failures have been seen to occur during the burn in period.) The pulse input register facility is also tested.

5.4.1 Method

		Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E
SETTINGS	Configuration	Edge Detect												OFF
		Data Compression												X1X
		Mode										Data Taking Mode		
		Select												0
		Masked Channels												None
	DACs	Ipreamp												220μA
		Ishaper												30μA
		Threshold DAC												500mV
		Calibration DAC											10mV (1.0fC)	
		Delay Register												-
		TrimRange												0
		TrimDAC												0
	TRIGGER	Sequence							Soft Reset + n BCO delay + Pulse Input Register Command + 129 BCO delay + L1A					
		Frequency												-
SCANS	LOOPS	1 – MASK											Mask #0, #3	
		2 – n BCO delay									150 to 161, step size = 1			
	nTriggers													100

The mask patterns to be used are as follows:

    0.   no channels masked (to identify dead cells)

    3.   all channels masked (to identify stuck cells)

5.4.2 Analysis

The number of channels that return data for each scanpoint is tallied – corresponding to the number of good channels. If for a given channel all 12 cells are found to be dead or stuck, then a defect type of DEAD[4] or STUCK is recorded. If for any channel the number of dead cells or stuck cells is greater than zero but less than 12, each individual defect is noted as either type DEADCELL or STUCKCELL.

5.4.3 Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information

TSTDCSINFO: monitored voltages, currents and temperatures

TSTHYBPIPE: the number of good pipeline cells in each chip

DEFECTS:

---

[4] In the event that this test finds a channel to be dead, a fault in the mask register would be one possible cause. In combination with the data set from the Redundancy Test it would be possible to identify dead cells in the mask register – but this has not yet been implemented.

Defect	First Chan	Last Chan
DEAD	CHANNEL	CHANNEL
STUCK	CHANNEL	CHANNEL
DEADCELL	CHANNEL	CHANNEL
STUCKCELL	CHANNEL	CHANNEL

5.4.4 Acceptance

A chip is considered to have passed if no more than 2 channels are found to have defects. The "PASS" field is set to "YES" only if all 12 chips are found to have passed.

5.4.5 Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533-8
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:18:12"
#
%DCS_INFO
#
#T0    T1
28.0   28.0
#VDET  IDET
200.0  0.85
#VCC   ICC
3.50   940
#VDD   IDD
4.00   500
#TIME_POWERED
.
#
%PipelineTest
#
#NGOOD
#M0 S1  S2  S3  S4  E5
128 128 128 128 128 128
#
#M8 S9  S10 S11 S12 E13
128 128 128 128 128 128
#
#No defects found!
```

6   *Description of Analogue Tests*

6.1   *StrobeDelay.cpp*

This test aims to establish the optimum setting of the delay register for each chip, to be used during all subsequent analogue tests. The size of each delay step is known to vary as a function of temperature, hence the strobe delay setting must always be re-optimised each time a device is operated at a different temperature. Sufficient time must always be allowed for the powered, configured hybrid or module to reached thermal equilibrium with its surroundings before this test may be undertaken.

Running with Edge Detect ON, compression 01X, a 4.0fC signal is injected for a threshold of 2.0fC. A functional fit is made to both the rising and falling edges to give the points at which 50% efficiency is achieved. The operating point is chosen to be 25% of the distance between these two points with reference to the rising edge of the strobe delay peak, which corresponds to the falling edge of the signal. By setting the timing some distance behind this edge, good efficiency can be ensured even for small signals. (This method gives answers in close agreement with a point 20% of the way along the plateau for a module of typically 1450 ENC noise.)

6.1.1   Method

The macro first performs a threshold scan with 2fC injected charge and set the threshold of each chip in accordance with the calculated mean VT50 values. Next the actual delay scan is performed as described below:

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E
		Edge Detect												ON
		Data Compression												01X
		Mode										Data Taking Mode		
		Select												0
		Masked Channels												None
	DACs	Ipreamp												220μA
		Ishaper												30μA
		Threshold DAC												(2.0fC)
		Calibration DAC											40mV (4.0fC)	
		Delay Register												(scanned)
		TrimRange												0
		TrimDAC												0
	TRIGGER	Sequence						Calibration Pulse + 131 BCO delay + L1A						
		Frequency												-
SCANS	LOOPS	1 – Delay							0 to 63, step size = 1					
	nTriggers													1000

6.1.2 **Analysis**

The analysis as described below is repeated for each chip in turn.

An error function is fitted to the rising edge of a strobe delay peak, corresponding to the falling edge of the signal. Similarly a complementary error function is fitted to the falling edge, corresponding to the rising edge of the signal. The width of the strobe delay peak is now known and the strobe delay register is set to a point 25% of the distance between the two edges, such that the electronics remain efficient for smaller signals.

If the fit to the rising edge of the strobe delay peak returns a value below the permitted minimum of 0 or the fit to the falling edge returns a value above the permitted minimum of 35, the defect SD_LO is recorded. Similarly if the fit to the falling edge of the strobe delay peak returns a value above the permitted maximum of 28 or the fit to the falling edge returns a value above the permitted maximum of 63, the defect SD_HI is recorded.

6.1.3 **Database**

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information

TSTDCSINFO: monitored voltages, currents and temperatures

TSTHYBDELAY: Strobe delay setting for each chip

DEFECTS:

Defect	First Channel	Last Channel
SD_LO	Chip * 128	((Chip+1) * 128) -1
SD_HI	Chip * 128	((Chip+1) * 128) -1

6.1.4 **Acceptance**

None of the defects found by this test are allowable on production modules, hence the "PASS" field will be set to "NO" if any defects were found. The database reporting structure should also provide the possibility to set acceptance cuts on the range of delay values.

6.1.5 **Sample Output from the Results File**

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533-11
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:20:12"
#
%DCS_INFO
#
#T0    T1
28.0   29.0
#VDET  IDET
200.0  0.90
#VCC   ICC
3.50   940
#VDD   IDD
4.00   500
#TIME_POWERED
.
#
%StrobeDelay
#
#DELAY
#M0 S1  S2  S3  S4  E5
12 12 13 12 12 13
#
#M8 S9  S10 S11 S12 E13
13 14 12 13 13 14
#
#No defects found!
```

6.2 *ThreePointGain.cpp*

Threshold scans are taken for three injected charges to facilitate a quick measurement of gain and noise and to give an estimation of the discriminator offset. Notably in the case of a module, threshold scans taken with small charges (<1.5fC) yield s-curves which are distorted at low thresholds due to noise occupancy. Fitting the complementary error function to such an s-curve, the noise is under estimated. For this reason, it is best to make noise measurements with injected charges of 1.5fC or more.

6.2.1 Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E
		Edge Detect	OFF											
		Data Compression	X1X											
		Mode	Data Taking Mode											
		Select	0											
		Masked Channels	None											
	DACs	Ipreamp	220µA											
		Ishaper	30µA											
		Threshold DAC	(scanned)											
		Calibration DAC	(variable)											
		Delay Register	(optimised)											
		TrimRange	0											
		TrimDAC	(trimmed or untrimmed as appropriate)											
	TRIGGER	Sequence	Calibration Pulse + 131 BCO delay + L1A											
		Frequency	-											
SCANS	LOOPS	1 – Qinj	1.50fC, 2.00fC, 2.50fC											
		2 – THRESHOLD	Ranges and step sizes to be determined											
		3 – CAL LINE	0, 1, 2, 3											
	nTriggers		1000											

6.2.2 Analysis

A complementary error function is fitted to each threshold scan to yield values of VT50 and output noise for each channel. A straight line is fitted to each set of three VT50 points to determine the gain and offset of each channel. The input noise can now be calculated by dividing the output noise measured at 2fC by the calculated gain.

Anomalous channels are categorised as follows:

Defect	Condition	Default value of cut
DEAD	No output	-
STUCK	Continuous output	-
LO_GAIN	Gain < (0.75 * mean_chip_gain)	-
HI_GAIN	Gain > (1.25 * mean_chip_gain)	-
LO_OFFSET	Offset < **MIN_OFFSET**	-100 (mV)
HI_OFFSET	Offset > **MAX_OFFSET**	120 (mV)
UNBONDED	Noise < **BONDED_NOISE**	800 (ENC)
PARTBONDED	Noise < **MIN_INNSE**	1100 (ENC)
NOISY	Noise > (1.15 * mean_chip_noise)	-
INEFFICIENT	Maximum efficiency <100%	(not yet implemented)

Channels with the following defects are now masked at the end of a ThreePointGain test to reduce the probability of problems related to these defects being carried over to subsequent tests:

- low gain (< 0.75 * chip_mean_gain) + high noise (> 1.15 * chip_mean_noise)
- DEAD
- STUCK
- high offset (>120mV)
- *very low gain* (< 0.3 * chip_mean_gain)

In each case a DB comment is written to the results file.

6.2.3 Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures
TSTSCANINFO: number of scan points and corresponding charge values
TSTHYBRC: response curve, gain, noise and offset information

DEFECTS**:**

Defect	First Channel	Last Channel
DEAD	First Channel	Last Channel
STUCK	First Channel	Last Channel
LO_GAIN	First Channel	Last Channel
HI_GAIN	First Channel	Last Channel
LO_OFFSET	First Channel	Last Channel
HI_OFFSET	First Channel	Last Channel
UNBONDED	First Channel	Last Channel
PARTBONDED	First Channel	Last Channel
NOISY	First Channel	Last Channel
INEFF	First Channel	Last Channel

RAW DATA:
CHANNEL_DATA (mandatory)

6.2.4 Acceptance

The "PASS" field is set to "NO" if one or more of the following criteria is fulfilled:

- A single chip is DEAD, STUCK or INEFFICIENT
- A single chip has gain < 0 or gain > 100
- More than 8 consecutive bad strips
- More than 15 bad strips in total

In each case the reason why the test has failed is stated in the results file in the form of a DB comment.

The database reporting structure must provide the possibility to set additional acceptance cuts on the mean and rms of VT50, gain, offset and noise, together with cuts on the maximum number of allowable channel defects falling into each of the following two categories:

A) LOST   DEAD, STUCK, UNBONDED, NOISY
B) FAULTY   LO_GAIN, HI_GAIN, LO_OFFSET, HI_OFFSET,
                PARTBONDED, INEFFICIENT

6.2.5 Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533-12
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:22:42"
#
%DCS_INFO
#
#T0     T1
28.0    29.0
#VDET   IDET
200.0   0.90
#VCC    ICC
3.50    940
#VDD    IDD
4.02    490
#TIME_POWERED
.
#
#
%SCAN_INFO
#
#POINT_TYPE
"QCAL (fC)"
#N_POINTS
3
#POINTS
1.50    2.00    2.50    .       .       .       .       .
.       .       .       .       .       .       .       .
#
```

```
#
%ThreePointGain
#
#Loop A - Fit
#       func    p0      p1      p2
#M0
        4       15.13   55.08   0.00
#S1
        4       16.14   54.84   0.00
#S2
        4       16.01   56.02   0.00
#S3
        4       14.53   56.10   0.00
#S4
        4       17.24   54.46   0.00
#E5
        4       14.52   54.45   0.00
#M8
        4       14.94   54.47   0.00
#S9
        4       15.60   56.08   0.00
#S10
        4       9.32    54.01   0.00
#S11
        4       12.07   53.46   0.00
#S12
        4       14.33   54.10   0.00
#E13
        4       15.33   55.88   0.00
#
#Loop B - Gain, Offset, Noise at 2.00fC
#       vt50    rms     gain    rms     offset  rms     outnse  innse   rms
#M0
        124.9   8.57    55.1    1.21    15.7    8.36    13.20   1499    33
#S1
        125.5   9.71    54.8    1.14    17.0    9.27    13.57   1546    37
#S2
        128.1   8.89    56.0    1.44    16.3    7.16    13.40   1495    35
#S3
        126.2   7.75    56.1    1.21    14.9    6.86    13.58   1513    33
#S4
        125.7   7.67    54.5    1.21    17.4    7.27    13.42   1540    31
#E5
        123.4   6.49    54.4    1.16    14.7    5.99    13.03   1496    42
#M8
        123.8   7.12    54.5    1.17    15.1    6.23    13.34   1531    35
#S9
        127.5   8.20    56.1    1.18    16.1    7.33    13.65   1522    32
#S10
        117.3   7.93    54.0    1.22    10.9    5.77    12.89   1493    37
#S11
        118.7   8.35    53.5    1.19    13.2    6.62    13.16   1539    38
#S12
        122.2   7.68    54.1    1.28    14.7    7.27    13.40   1548    32
#E13
        126.8   7.15    55.9    1.14    15.6    6.27    13.45   1505    34
#
#Loop C - Comment
#M0 S1  S2  S3  S4  E5
"OK"    "OK"    "OK"    "OK"    "OK"    "OK"
#M8 S9  S10 S11 S12 E13
"OK"    "OK"    "OK"    "OK"    "OK"    "OK"
```

```
#BadChannelSummary - not for the database
#  at 2.00fC
#           lost   dodgy   dead   stuck   ineff   unbon   lo_gn   hi_gn   lo_off  hi_off  partbon hi_nse
#Chip  0:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip  1:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip  2:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip  3:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip  4:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip  5:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip  6:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip  7:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip  8:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip  9:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip 10:      0       0      0       0       0       0       0       0       0       0       0       0
#Chip 11:      0       0      0       0       0       0       0       0       0       0       0       0
#Link  0:      0       0      0       0       0       0       0       0       0       0       0       0
#Link  1:      0       0      0       0       0       0       0       0       0       0       0       0
#Link  2:      0       0      0       0       0       0       0       0       0       0       0       0
#No defects found!
#
%TEST Rawdata
FILENAME      : D:\sctvar\results\20220330200011_RC_533_12.txt
#
%Web link
DESCRIPTION   : Plots (postscript)
URL           :
http://hepunx.rl.ac.uk/atlassct/cgibin/getfile.pl?file=20220330200011_RCPlot_20030121_172243.ps
#
```

6.3   TrimRange.cpp

During production, the chips used to build modules will be selected such that the offsets of all channels may be brought into line by adjustment of the TrimDAC using TrimRange 0 or TrimRange 1. In ATLAS it will be necessary to increase the range of each TrimDAC in order to accommodate the increase in the offset spread as a function of radiation dose. Hence it is necessary to determine the initial TrimDAC characteristic for each of the four TrimRange settings.

For TrimRange 0, the TrimDAC characteristic is studied using each of the possible TrimDAC values. This is done to ensure that each step may be selected and to demonstrate that the TrimDAC characteristic is linear and monotonic for all steps. For the remaining three TrimRange settings, the TrimDAC characteristic is studied using only 4 of the possible TrimDAC values. The prime motivation for this reduction in the number of component scans is to save time during testing.

Since the nominal operating threshold in ATLAS will be 1.0fC, the TrimDAC/TrimRange characterisation should be performed in response to 1.0fC injected charge.

6.3.1   Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E
		Edge Detect												OFF
		Data Compression												X1X
		Mode											Data Taking Mode	
		Select												0
		Masked Channels												None
	DACs	Ipreamp												220μA
		Ishaper												30μA
		Threshold DAC												(scanned)
		Calibration DAC											10mV (1.0fC)	
		Delay Register												(optimised)
		TrimRange												(scanned)
		TrimDAC												(scanned)
	TRIGGER	Sequence						Calibration Pulse + 131 BCO delay + L1A						
		Frequency												-
SCANS	LOOPS	1 – Trim Range										0 to 4, step size = 1		
		2 – TrimDAC					TR=0:(0 to 15) TR=1,2,3: (3, 7, 11, 15)							
		3 – THRESHOLD					Ranges and step sizes to be determined							
		4 – CAL LINE												0, 1, 2, 3
	nTriggers													200

6.3.2   Analysis

Each scan is fitted in turn to yield a matrix giving the threshold needed to obtain 50% efficiency (VT50) for 1fC input charge as a function of TrimDAC setting. For each combination of TrimRange and channel number, a straight line is fitted to the data to determine the step size and offset of the corresponding TrimDAC characteristic. Any points for which the s-curve fitting returned an error are ignored but the present version of the code does not include a noise cut at this stage.

For each TrimRange, a range of targets (2.5mV to 300mV in 2.5mV steps) is studied to determine the maximum number of channels that can be brought into line. For each channel in turn, the fitted TrimDAC characteristic is solved to determine the TrimDAC setting needed to reach the studied targets. If the calculated value is within the range of possible TrimDAC settings, the channel is considered to be trimmable for that combination of TrimRange and target.

At a second pass, the TrimRange value for each chip is chosen to maximise the number of trimmable channels. By default this is done such that all channels of the module are trimmed to the same target value, but the option exists to allow each chip to be trimmed to a different target.

For each TrimRange setting, an ASCII file is generated listing the TrimDAC values for each chip. For historical reasons this takes the form of a floating point number between 0 and 1, but this may change to a more logical format such as an integer between 0 and 15. A fifth trim file is generated listing the TrimRange and TrimDAC settings found to be best overall for the hybrid or module under test.

In each of the above five cases a corresponding mask file is generated listing those channels to be masked and the reasons why. In addition to untrimmable channels, dead, stuck and particularly noisy channels are also masked. (In this instance a particularly noisy channel is defined to be one with output noise more than 125% of the mean output noise of the parent chip.)

Defective chips and/or channels are categorised as follows:

Defect	Description	Condition(s)
TR_RANGE	A chip for which the mean step size is not as expected for the presently selected TrimRange	TR0: step < 1.5 or step > 5.0[5] TR1: step < 5.0 or step > 8.5 TR2: step < 8.5 or step > 12.0 TR3: step < 12.0 or step > 15.5
TR_STEP	A channel for which the step size differs from the mean step size of that chip	Step < (mn_step - (3* rms_step))
		Step > (mn_step + (3* rms_step))
TR_OFFSET	A channel for which the offset differs from the mean offset of that chip	Offset < (mn_offset - (3* rms_offset))
		Offset > (mn_offset + (3* rms_offset))

---

[5] These cuts are provisional, and may change with future batches of ABCD3T wafers.

Untrimmable channels are also listed as defects:

Defect	Description	Condition(s)
TR_NOTRIM	A channel that may not be trimmed	Untrimmable Channel

6.3.3 Database

The results of this test should be stored in the SCT database using five instances of the following table, with TRIM_TYPE = {0,1,2,3,-1} corresponding to TrimRange=0, TrimRange=1, TrimRange=2, TrimRange=3, and with optimised TrimRange settings. In each case the trim and mask files should be uploaded to the database for future reference.

TSTDAQINFO: host and version information

TSTDCSINFO: monitored voltages, currents and temperatures

TSTSCANINFO: number of scans and corresponding TrimDAC settings

TSTHYBTRIM: trim summary

DEFECTS:

Defect	*First Channel*	*Last Channel*
TR_RANGE	*Chip * 128*	*((Chip+1) *128)-1*
TR_STEP	*First Channel*	*Last Channel*
TR_OFFSET	*First Channel*	*Last Channel*

RAW DATA:

TRIM_DATA (mandatory)

6.3.4 Acceptance

The "PASS" field is set to "NO" if any defect of type TR_RANGE has been recorded, or if there are any untrimmable channels.

The database reporting structure should also provide the possibility to set acceptance cuts on the number of trimmable channels, the mean and rms of the distribution of vt50 values after trimming, the TrimDAC offset and the TrimDAC step size.

6.3.5 Sample Output from the Results File

Example 1: with all chips set to TrimRange 0

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533-15
TEST_DATE      : 21/01/2003
PASSED         : NO
PROBLEM        : NO
```

```
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:23:16"
#
%DCS_INFO
#
#T0      T1
29.0    29.0
#VDET    IDET
200.0    0.90
#VCC     ICC
3.50     940
#VDD     IDD
4.00     490
#TIME_POWERED
.
#
#
%SCAN_INFO
#
#POINT_TYPE
"TrimDAC (bits)"
#N_POINTS
16
#POINTS
0.00    1.00    2.00    3.00    4.00    5.00    6.00    7.00
8.00    9.00    10.00   11.00   12.00   13.00   14.00   15.00
#
%Trim
#
#TRIM    CHARGE  TYPE    ALGORITHM
         1.0     0       0
#(trim whole module)
#
#        range   target  ntrim   vt50    vt50rms tr_off  off_rms tr_step step_rms
#M0
         0       90.0    127     90.0    1.23    -19.7   2.8     3.53    0.17
#S1
         0       90.0    127     90.1    1.29    -20.5   3.4     3.41    0.17
#S2
         0       90.0    128     90.0    1.34    -17.9   2.0     4.03    0.20
#S3
         0       90.0    128     90.0    1.19    -19.8   2.3     3.51    0.16
#S4
         0       90.0    128     90.2    1.23    -19.2   2.3     3.68    0.14
#E5
         0       90.0    128     90.3    1.28    -19.4   2.2     3.51    0.18
#M8
         0       90.0    128     90.1    1.43    -17.7   1.8     3.89    0.18
#S9
         0       90.0    128     90.1    1.18    -20.4   2.3     3.48    0.15
#S10
         0       90.0    128     89.8    0.95    -19.9   2.5     3.18    0.18
#S11
         0       90.0    128     90.2    1.36    -18.2   2.3     3.57    0.17
#S12
         0       90.0    128     90.2    1.31    -19.8   2.4     3.43    0.17
#E13
         0       90.0    128     90.2    1.31    -19.4   2.2     3.64    0.18
```

```
#
%Defect
DEFECT NAME    : TR_NOTRIM
FIRST CHANNEL  : 9
LAST CHANNEL   : 9
#
%Defect
DEFECT NAME    : TR_NOTRIM
FIRST CHANNEL  : 221
LAST CHANNEL   : 221
#
#2 defects found
#
%TEST Rawdata
FILENAME       : D:\sctvar\results\20220330200011_tr0_20030121.trim
#
%Web link
DESCRIPTION    : Plots (postscript)
URL            :
http://hepunx.rl.ac.uk/atlassct/cgibin/getfile.pl?file=20220330200011_TrimRangePlot_20030121_173801.ps
#
```

Example 2: with optimised TrimRange settings

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533-15
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:23:16"
#
%DCS_INFO
#
#T0     T1
29.0    29.0
#VDET   IDET
200.0   0.90
#VCC    ICC
3.50    940
#VDD    IDD
4.00    490
#TIME_POWERED
.
#
```

```
#
%Trim
#
#TRIM    CHARGE  TYPE    ALGORITHM
         1.0     -1      0
#(trim whole module)
#
#       range   target  ntrim   vt50    vt50rms tr_off  off_rms tr_step step_rms
#M0
         2       102.5   128     102.9   3.16    -6.9    0.9     10.12   0.39
#S1
         1       102.5   128     102.5   1.91    -10.6   1.6     6.64    0.29
#S2
         0       102.5   128     102.6   1.18    -17.9   2.0     4.03    0.20
#S3
         0       102.5   128     102.5   1.06    -19.8   2.3     3.51    0.16
#S4
         0       102.5   128     102.6   1.07    -19.2   2.3     3.68    0.14
#E5
         0       102.5   128     102.5   0.97    -19.4   2.2     3.51    0.18
#M8
         0       102.5   128     102.4   1.13    -17.7   1.8     3.89    0.18
#S9
         1       102.5   128     102.5   1.89    -10.5   1.2     6.79    0.24
#S10
         1       102.5   128     102.6   1.91    -9.8    1.2     6.41    0.30
#S11
         1       102.5   128     102.8   1.93    -9.6    1.2     6.80    0.29
#S12
         0       102.5   128     102.4   0.96    -19.8   2.4     3.43    0.17
#E13
         0       102.5   128     102.6   1.03    -19.4   2.2     3.64    0.18
#
%Defect
DEFECT NAME    : TR_OFFSET
FIRST CHANNEL  : 9
LAST CHANNEL   : 9
#
#1 defects found
#
%TEST Rawdata
FILENAME       : D:\sctvar\results\20220330200011_tr-1_20030121.trim
#
%Web link
DESCRIPTION    : Plots (postscript)
URL            :
http://hepunx.rl.ac.uk/atlassct/cgibin/getfile.pl?file=20220330200011_TrimRangePlot_20030121_173801.ps
#
```

6.4 ResponseCurve.cpp

6.4.1 Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E
		Edge Detect	OFF[6]											
		Data Compression	X1X											
		Mode	Data Taking Mode											
		Select	0											
		Masked Channels	Untrimmable, Stuck, Dead and Noisy Channels											
	DACs	Ipreamp	220µA											
		Ishaper	30µA											
		Threshold DAC	(scanned)											
		Calibration DAC	(variable)											
		Delay Register	(optimised)											
		TrimRange	0											
		TrimDAC	(optimised)											
	TRIGGER	Sequence	Calibration Pulse + 131 BCO delay + L1A											
		Frequency	-											
SCANS	LOOPS	1 – Qinj	0.50fC, 0.75fC, 1.00fC, 1.25fC, 1.50fC, 2.00fC, 3.00fC, 4.00fC, 6.00fC, 8.00fC											
		2 – THRESHOLD	Ranges and step sizes to be determined											
		3 – CAL LINE	0, 1, 2, 3											
	nTriggers		1000											

6.4.2 Analysis

A complementary error function is fitted to each threshold scan to yield values of VT50 and output noise for each channel. A straight line is fitted to each set of three VT50 points to determine the gain and offset of each channel. The input noise can now be calculated by dividing the output noise measured at 2fC by the calculated gain.

During early production of barrel modules it was found that for some chips, notably during cold tests, analysis of threshold scans performed with high injected charges gave anomalous high response and high noise values. This is understood to be due to the saturation of the threshold DAC towards the upper limit of its range, and of no relevance to the operational efficiency of the ATLAS SCT since the operating threshold will be much lower, however this effect can give rise to the incorrect determination of the gain. For this reason the analysis code has been modified to exclude scans recorded for injected charges in excess of 5.0fC from the gain calculation on a chip by chip basis where the mean noise of a chip for that scan is greater than 1.5 * the mean noise of the same chip when all scans are taken into account. A database comment is written to the result file for each chip where this cut has come into effect.

---

[6] When running with EDGE DETECT ON / EDGE COMPRESSION, threshold scans with small charges do not reach 100% efficiency since the noise is of comparable value to the injected charge. By running with edge detect off, in any other compression mode, such problems are minimised.

Anomalous channels are categorised as follows:

Defect	Condition	Default value of cut
DEAD	No output	-
STUCK	Continuous output	-
LO_GAIN	Gain < (0.75 * mean_chip_gain)	-
HI_GAIN	Gain > (1.25 * mean_chip_gain)	-
LO_OFFSET	Offset < **MIN_OFFSET**	-100 (mV)
HI_OFFSET	Offset > **MAX_OFFSET**	120 (mV)
UNBONDED	Noise < **BONDED_NOISE**	800 (ENC)
PARTBONDED	Noise < **MIN_INNSE**	1100 (ENC)
NOISY	Noise > (1.15*mean_chip_noise)	-
INEFFICIENT	Maximum efficiency <100%	(not yet implemented)

No Channels are masked as a result of the ResponseCurve test.

6.4.3 Database

This test has the same inputs and outputs as ThreePointGain.cpp:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures
TSTSCANINFO: number of scan points and corresponding charge values
TSTHYBRC: response curve, gain, noise and offset information

DEFECTS:

Defect	*First Channel*	*Last Channel*
DEAD	*First Channel*	*Last Channel*
STUCK	*First Channel*	*Last Channel*
LO_GAIN	*First Channel*	*Last Channel*
HI_GAIN	*First Channel*	*Last Channel*
LO_OFFSET	*First Channel*	*Last Channel*
HI_OFFSET	*First Channel*	*Last Channel*
UNBONDED	*First Channel*	*Last Channel*
PARTBONDED	*First Channel*	*Last Channel*
NOISY	*First Channel*	*Last Channel*
INEFF	*First Channel*	*Last Channel*

RAW DATA:

CHANNEL_DATA (mandatory)

6.4.4   Acceptance

The "PASS" field is set to "NO" if one or more of the following criteria are fulfilled:

- A single chip is DEAD, STUCK or INEFFICIENT
- A single chip has gain < 0 or gain > 100
- More than 8 consecutive bad strips
- More than 15 bad strips in total

In each case the reason why the test has failed is stated in the results file in the form of a DB comment.

The database reporting structure must provide the possibility to set additional acceptance cuts on the mean and rms of VT50, gain, offset and noise, together with cuts on the maximum number of allowable channel defects falling into each of the following two categories:

A) LOST   DEAD, STUCK, UNBONDED, NOISY

B) FAULTY   LO_GAIN, HI_GAIN, LO_OFFSET, HI_OFFSET,
                   PARTBONDED, INEFFICIENT

6.4.5   Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533-43
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:47:36"
#
%DCS_INFO
#
#T0     T1
28.0    29.0
#VDET   IDET
200.0  1.04
#VCC    ICC
3.48    980
#VDD    IDD
4.00    490
#TIME_POWERED
.
#
#
%SCAN_INFO
#
#POINT_TYPE
"QCAL (fC)"
#N_POINTS
10
#POINTS
```

```
0.50    0.75    1.00    1.25    1.50    2.00    3.00    4.00
6.00    8.00    .       .       .       .       .       .
#
```

```
0.50    0.75    1.00    1.25    1.50    2.00    3.00    4.00
6.00    8.00    .       .       .       .       .       .
#
```

```
#
%ResponseCurve
#
#Loop A - Fit
#      func    p0      p1      p2
#M0
        3       1729.05         7.79    -816.33
#S1
        3       1934.48         8.75    -919.00
#S2
        3       1790.33         7.99    -848.20
#S3
        3       1787.20         7.86    -847.33
#S4
        3       2188.48         9.95    -1046.14
#E5
        3       2056.55         9.44    -979.85
#M8
        3       1898.70         8.64    -901.74
#S9
        3       2135.62         9.46    -1020.99
#S10
        3       1649.58         7.61    -775.52
#S11
        3       2008.14         9.35    -954.29
#S12
        3       2114.72         9.75    -1008.89
#E13
        3       2118.27         9.41    -1012.56
#
#Loop B - Gain, Offset, Noise at 2.00fC
#      vt50    rms     gain    rms     offset  rms     outnse  innse   rms
#M0
        158.1   3.51    54.5    1.19    48.3    3.82    13.07   1499    33
#S1
        157.4   2.43    54.6    1.16    48.1    2.45    13.44   1537    36
#S2
        158.7   1.81    55.3    1.31    46.9    1.93    13.36   1511    34
#S3
        158.7   1.69    56.0    1.18    46.2    1.67    13.57   1513    31
#S4
        156.8   1.70    54.7    1.24    47.8    1.78    13.32   1523    30
#E5
        156.5   1.69    54.0    1.13    48.3    1.57    13.03   1509    38
#M8
        156.4   1.79    54.3    1.19    47.5    1.76    12.75   1468    33
#S9
        158.4   2.27    55.8    1.11    46.8    2.25    13.26   1486    33
#S10
        156.5   2.33    53.4    1.15    49.1    2.39    12.81   1501    37
#S11
        155.8   2.66    53.2    1.22    49.6    2.25    13.02   1529    36
#S12
        155.6   1.65    53.8    1.28    48.3    1.78    13.04   1515    33
#E13
        158.2   1.68    55.6    1.02    46.7    1.48    13.53   1520    36
#
#Loop C - Comment
#M0  S1   S2   S3   S4   E5
"OK"    "OK"    "OK"    "OK"    "OK"    "OK"
#M8  S9   S10  S11  S12  E13
"OK"    "OK"    "OK"    "OK"    "OK"    "OK"
```

```
#BadChannelSummary - not for the database
#  at 2.00fC
#            lost   dodgy   dead   stuck   ineff   unbon   lo_gn   hi_gn   lo_off  hi_off  partbon hi_nse
#Chip  0:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip  1:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip  2:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip  3:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip  4:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip  5:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip  6:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip  7:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip  8:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip  9:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip 10:     0      0      0      0       0       0       0       0       0       0       0       0
#Chip 11:     0      0      0      0       0       0       0       0       0       0       0       0
#Link  0:     0      0      0      0       0       0       0       0       0       0       0       0
#Link  1:     0      0      0      0       0       0       0       0       0       0       0       0
#Link  2:     0      0      0      0       0       0       0       0       0       0       0       0
#No defects found!
#
%TEST Rawdata
FILENAME      : D:\sctvar\results\20220330200011_RC_533_43.txt
#
%Web link
DESCRIPTION   : Plots (postscript)
URL           :
http://hepunx.rl.ac.uk/atlassct/cgibin/getfile.pl?file=20220330200011_RCPlot_20030121_174736.ps
#
```

6.5   NO.cpp

For this measurement, the trigger frequency should approach the nominal ATLAS trigger rate of 100kHz[7], being throttled back as necessary at higher occupancies in order to avoid buffer overflow errors. In order to measure noise occupancies down to the level of 10^{-6} up to 10^{6} events are taken. At the other end of the scale, where occupancy approaches 1.0, only 2000 events are recorded. Between the two extremes the fractional occupancy of each channel is calculated after each partial burst and the number of events taken is varied such that, for each scanpoint, a minimum of 50 hits are seen in more than 50% of the active readout channels. In the case that the occupancy of a given channel should overflow the depth of the MuSTARD histogram memory, its fractional occupancy is frozen as that determined prior to the overflow condition.

A variant of the algorithm is under development to adjust the scanned range of each module according to the target values to which its chips have been trimmed. This will provide a faster turnaround when several modules are being tested in parallel. Under such circumstances the scanned range will appear as –75 to 75 mV corresponding to the range (target-75) to (target+75) mV. The analysis has been rewritten to detect the revised range and to accommodate the trim target values when making the plot of log occupancy vs. threshold[2] (fC^2).

---

[7] The 100kHz trigger rate and buffer overflow control have been implemented only for users of CLOAC. A fallback test has been implemented for users with only SLOG, but the trigger rate is not controlled.

6.5.1 Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E
		Edge Detect												OFF
		Data Compression												X1X
		Mode										Data Taking Mode		
		Select												0
		Masked Channels					Untrimmable, Stuck, Dead and Noisy Channels							
	DACs	Ipreamp												220µA
		Ishaper												30µA
		Threshold DAC												(scanned)
		Calibration DAC												-
		Delay Register												(optimised)
		TrimRange												0
		TrimDAC												(optimised)
	TRIGGER	Sequence												L1A
		Frequency					Up to 100kHz, depending upon occupancy							
SCANS	LOOPS	1 – THRESHOLD					0 – 150mV in 2.5mV steps (typically to cover the range –1.0fC to +2.0fC)							
	nTriggers						Up to 1000,000, depending upon occupancy							

6.5.2 Analysis

This scan yields a direct measurement of noise occupancy at 1fC. The trim information is read in from the most recent results file such that the 1fC point is accurately known: in this the module currents and its noise occupancy at the nominal operating point can be extracted from the data.

By fitting an error function to the noise occupancy curve for each chip, the noise occupancy offset is determined. The response curve is read in from the most recent results file and the information is used to fit a straight line to a plot of log occupancy vs. threshold^2 (fC^2) to yield a measurement of the noise. A plot of the noise occupancy s-curves is automatically generated.

Defective channels are categorised as follows:

Defect	Description	6.5.2.1 Condition(s)
NO_HI	A channel with high noise occupancy	Occupancy > 5×10^{-4}

6.5.3 Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information

TSTDCSINFO: monitored voltages, currents and temperatures

TSTHYBNOISE: noise occupancy at 1fC, NO offset and estimated noise (ENC)

DEFECTS:

Defect	*Channel*	*Last Channel*
NO_HI	*First Channel*	*Last Channel*

6.5.4   Acceptance

Use of the "PASS" field is not yet implemented for this test, hence it is always set to "YES".

The database reporting structure should provide the possibility to set acceptance cuts on each of the following parameters:

- The extrapolated noise occupancy offset
- The mean noise occupancy at 1fC
- RMS of the noise occupancy at 1fC
- The estimated noise at 1fC
- The number of channels with high noise occupancy
- The typical and maximum values of Icc and Idd.

6.5.5   Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533-53
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"17:54:18"
#
%DCS_INFO
#
#T0     T1
28.0    29.0
#VDET   IDET
200.0   1.06
#VCC    ICC
3.50    970
#VDD    IDD
4.00    500
#TIME_POWERED
.
#
```

```
#
%NO
#
#MAX   ICC    IDD
       980    780
#TYP   ICC    IDD
       960    510
#
#      Offset MeanOcc      RMSOcc         EstENC
#M0
       45.8   3.0e-005     8.1e-005       1506
#S1
       46.7   3.2e-005     2.4e-005       1500
#S2
       43.7   6.1e-006     4.2e-006       1422
#S3
       42.7   7.9e-006     5.2e-006       1425
#S4
       46.0   1.5e-005     7.2e-006       1462
#E5
       46.1   1.5e-005     8.0e-006       1470
#M8
       45.2   5.9e-006     3.9e-006       1419
#S9
       43.7   1.2e-005     9.5e-006       1449
#S10
       47.7   8.4e-006     7.5e-006       1405
#S11
       49.4   2.2e-005     1.5e-005       1451
#S12
       47.5   1.1e-005     5.7e-006       1427
#E13
       44.3   9.8e-006     5.8e-006       1436
#
%Defect
DEFECT NAME    : NO_HI
FIRST CHANNEL  : 9
LAST CHANNEL   : 9
#
#1 defects found
%Web link
DESCRIPTION    : Plots (postscript)
URL            :
http://hepunx.rl.ac.uk/atlassct/cgibin/getfile.pl?file=20220330200011_NoPlot_20030121_175418.ps
#
%Web link
DESCRIPTION    : Scurves (postscript)
URL            :
http://hepunx.rl.ac.uk/atlassct/cgibin/getfile.pl?file=20220330200011_NoScurve_20030121_175418.ps
#
```

6.6 Timewalk.cpp

In the ABCD3T Chip specification document, timewalk is defined as, "The maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10.0fC, with the comparator set to 1fC". This procedure sets out to make this measurement.

6.6.1   Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E
		Edge Detect												ON
		Data Compression												01X
		Mode										Data Taking Mode		
		Select												0
		Masked Channels				Untrimmable, Stuck, Dead and Noisy Channels							
	DACs	Ipreamp												220μA
		Ishaper												30μA
		Threshold DAC												(1fC)
		Calibration DAC												(variable)
		Delay Register												(scanned)
		TrimRange												0
		TrimDAC												(optimised)
	TRIGGER	Sequence				Calibration Pulse + 131 BCO delay + L1A							
		Frequency												-
SCANS	LOOPS	1 – Qinj										1.25fC, 10.0fC		
		2 – Delay										0 to 63, step size = 1		
	nTriggers													1000

6.6.2   Analysis

For each value of injected charge, a complementary error function is fitted to the falling edge of a plot of efficiency vs. the setting of the delay register, to determine the delay setting at which the efficiency reaches half of its peak value. The difference between these two values gives the timewalk in terms of steps on the delay register.

In the case of the delay scan taken with 10fC injected charge, an error function is fitted to the rising edge of the efficiency plot. Since these scans are taken in edge mode the width of the strobe delay peak will be 25nS. This provides a calibration factor for the strobe delay register, hence the timewalk can be converted to units of nS.

Anomalous timewalk values are categorised as defects as follows:

Defect	Condition	Default value of cut
TW_LO	Timewalk < **MIN_TW**	5
TW_HI	Timewalk > **MAX_TW**	16

6.6.3   Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures
TSTSCANINFO: number of scans and corresponding charge values
TSTHYBTW: timewalk (nS) and calibration factor of each chip

DEFECTS:

Defect	*First Channel*	*Last Channel*
TW_LO	*First Channel*	*Last Channel*
TW_HI	*First Channel*	*Last Channel*

6.6.4   Acceptance

The "PASS" field will be set to "NO" if any defects are found.

The database reporting structure should provide the possibility to set more stringent acceptance cuts on the calculated value of the timewalk and the strobe delay calibration factor.

6.6.5   Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200011
TEST MADE BY   : PWP
LOCATION NAME  : RAL
Run number     : 533-55
TEST_DATE      : 21/01/2003
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PPDNT3"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"18:06:08"
```

```
#
%DCS_INFO
#
#T0       T1
28.0      29.0
#VDET     IDET
200.0     1.06
#VCC      ICC
3.50      970
#VDD      IDD
4.00      510
#TIME_POWERED
.
#
#
%SCAN_INFO
#
#POINT_TYPE
"QCAL (fC)"
#N_POINTS
10
#POINTS
1.25      1.50   1.75   2.00    3.00    4.00    5.00    6.00
8.00      10.00          .       .       .       .       .       .
#
#
%Timewalk
#
#TW
#M0       S1     S2     S3      S4      E5
11.5      11.5   12.1   11.8    11.9    11.8
#
#M8       S9     S10    S11     S12     E13
12.3      11.9   12.7   12.3    12.8    12.0
#
#TCAL
#M0       S1     S2     S3      S4      E5
25.9      25.7   25.7   25.7    26.0    25.9
#
#M8       S9     S10    S11     S12     E13
26.5      26.6   25.9   26.6    26.5    27.1
#
#No defects found!
%Web link
DESCRIPTION    : Plots (postscript)
URL            :
http://hepunx.rl.ac.uk/atlassct/cgibin/getfile.pl?file=20220330200011_TimewalkPlot_20030121_180609.ps
#
```

7 *Description of Other Electrical Tests*

7.1 *HybridLTT.cpp*

7.1.1 Method

This is a "warm" test of 90 hours duration. For a barrel hybrid, the temperature is controlled such that the hybrid thermistors report 37^OC. Every five minutes the temperatures and currents are monitored and a short burst of triggers is sent to monitor the noise occupancy of the hybrid at 1fC threshold. Every two hours a confirmation test is performed and, at the end of the test, a characterisation sequence is initiated.

During the test, the monitored temperatures are checked against an upper limit. If they exceed that limit the power is switched off and the test is stopped. Upon completion of a warm test the power is switched off.

7.1.2 Analysis

The results of each confirmation sequence will be compared against earlier data to identify the occurrence of any new defects.

7.1.3 Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures at the end of test
TSTHYBLTT: minimum and maximum temperatures and currents during the test

DEFECTS: as for the individual test components

RAW DATA:

LTT_MONITOR_DATA (mandatory)

7.1.4   Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200013
TEST MADE BY   : dgc
LOCATION NAME  : Birmingham
Run number     : 1016-1
TEST_DATE      : 30/07/2002
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"EPAT2"
#VERSION
"3.34"
#DUT
"Barrel_Hybrid"
#TIME
"17:08:39"
#
%DCS_INFO
#
#T0     T1
36.0    36.0
#VDET   IDET
0.0     0.00
#VCC    ICC
3.50    970
#VDD    IDD
4.00    530
#TIME_POWERED
.
#
#
%LongTermTest
#
#Duration
90.0
#Time of first failure
-1.0
#T0 min max
36.0    38.0
#T1 min max
35.0    37.0
#Icc min max
940     1010
#Idd min max
510     540
#Idet min max
.       .
#
%TEST Rawdata
FILENAME       : D:\sctvar\results\20220330200013_ltt_1016-1.txt
```

7.2 *HybridColdTest.cpp*

7.2.1 Method

This is a "cold" test of 10 hours duration. For a barrel hybrid, the temperature is controlled such that the hybrid thermistors report 0^OC. Every five minutes the temperatures and currents are monitored and a short burst of triggers is sent to monitor the noise occupancy of the hybrid at 1fC threshold. Every two hours a confirmation test is performed and, at the end of the test, a characterisation sequence is initiated.

During the test, the monitored temperatures are checked against an upper limit. If they exceed that limit the power is switched off and the test is stopped. Upon completion of a cold test the power is left on.

7.2.2 Analysis

The results of each confirmation sequence will be compared against earlier data to identify the occurrence of any new defects.

7.2.3 Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures at the end of test
TSTHYBLTT: minimum and maximum temperatures and currents during the test

DEFECTS: as for the individual test components

RAW DATA:

LTT_MONITOR_DATA (mandatory)

7.2.4 Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220330200009
TEST MADE BY   : dgc
LOCATION NAME  : Birmingham
Run number     : 181-2
TEST_DATE      : 24/07/2002
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"EPAT6"
#VERSION
"3.34"
#DUT
"Barrel_Hybrid"
#TIME
"13:46:20"
#
%DCS_INFO
#
#T0     T1
0.0     0.0
#VDET   IDET
0.0     0.00
#VCC    ICC
3.50    1000
#VDD    IDD
4.00    500
#TIME_POWERED
.
#
#
%LongTermTest
#
#Duration
10.8
#Time of first failure
-1.0
#T0 min max
0.0     0.0
#T1 min max
0.0     1.0
#Icc min max
990     1000
#Idd min max
490     530
#Idet min max
.       .
#
%TEST Rawdata
FILENAME       : D:\sctvar\results\20220330200009_ltt_181-2.txt
```

7.3 ModuleLTT.cpp

7.3.1　　　Method

For the test duration of 24 hours, a module is maintained at the operating temperature expected in ATLAS. Every five minutes the temperatures and currents are monitored and a short burst of triggers is sent to monitor the noise occupancy of the module at 1fC threshold. Every two hours a confirmation test is performed and, at the end of the test, a characterisation sequence is initiated.

During the test, the monitored temperatures are checked against an upper limit. If they exceed that limit the power is switched off and the test is stopped. Similarly in the event of a high voltage trip, the test is stopped. The low voltage power is left on at the end of the test.

7.3.2　　　Analysis

The results of each confirmation sequence will be compared against earlier data to identify the occurrence of any new defects.

7.3.3　　　Database

The following information should be stored in the SCT database:

TSTDAQINFO:　　host and version information
TSTDCSINFO:　　monitored voltages, currents and temperatures at the end of test
TSTHYBLTT:　　minimum and maximum temperatures and currents during the test

DEFECTS:　　as for the individual test components

RAW DATA:

LTT_MONITOR_DATA (mandatory)

7.3.4   Sample Output from the Results File

```
#
%NewTest
#
SERIAL NUMBER  : 20220170100038
TEST MADE BY   : DR
LOCATION NAME  : Cambridge
Run number     : 186-1
TEST_DATE      : 05/06/2002
PASSED         : YES
PROBLEM        : NO
#
%DAQ_INFO
#
#HOST
"PCBJ"
#VERSION
"3.34"
#DUT
"Barrel_Module"
#TIME
"11:54:01"
#
%DCS_INFO
#
#T0     T1
1.0     1.0
#VDET   IDET
197.0   0.13
#VCC    ICC
3.50    970
#VDD    IDD
4.02    500
#TIME_POWERED
.
#
#
%LongTermTest
#
#Duration
25.5
#Time of first failure
-1.0
#T0 min max
0.0     1.0
#T1 min max
0.0     1.0
#Icc min max
960     980
#Idd min max
490     500
#Idet min max
0.113   0.225
#
%TEST Rawdata
FILENAME       : D:\sctvar\results\20220170100038_ltt_186-1.txt
```

8   Appendices

8.1   Appendix 1 – Definitions of Utility Tables

TSTDAQINFO: tag "%DAQ_INFO"

Column Name		Representation	Range	Comment
HOST	O	Char(30)	–	Hostname of test PC
VERSION	O	Char(10)	–	Software Version, e.g. 3.20
DUT	O	Char(20)	–	Device Under Test eg. "Barrel Hybrid" or "Barrel Module"
TEST_TIME	O	Char(10)	–	Time the test started

TSTDCSINFO: tag "%DCS_INFO"

Column Name		Representation	Range	Comment
T0	O	Float	-100 to 200	Module Temp. 0 (^{O}C)
T1	O	Float	-100 to 200	Module Temp. 1 (^{O}C)
Vdet	O	Float	0 to 500	Detector Voltage (V)
Idet	O	Float	0 to 5200	Detector Current (μA)
Vcc	O	Float	0 to 10	Analogue Voltage (V)
Icc	O	Float	0 to 10	Analogue Current (A)
Vdd	O	Float	0 to 10	Digital Voltage (V)
Idd	O	Float	0 to 10	Digital Current (A)
TIME_POWERED	O	Float	0 – inf.	(hours)[8]

TSTSCANINFO: tag "%SCAN_INFO"

Column Name		Representation	Range	Comment
POINT_TYPE	M	Char(20)	–	Scan point descriptor
N_POINTS	M	Int (8 bit)	0 to 16	Number of scans
POINT_0	O	Float	-inf to inf	Scan point setting
POINT_1	O	Float	-inf to inf	Scan point setting
POINT_2	O	Float	-inf to inf	Scan point setting
POINT_3	O	Float	-inf to inf	Scan point setting
POINT_4	O	Float	-inf to inf	Scan point setting
POINT_5	O	Float	-inf to inf	Scan point setting
POINT_6	O	Float	-inf to inf	Scan point setting
POINT_7	O	Float	-inf to inf	Scan point setting
POINT_8	O	Float	-inf to inf	Scan point setting
POINT_9	O	Float	-inf to inf	Scan point setting
POINT_10	O	Float	-inf to inf	Scan point setting
POINT_11	O	Float	-inf to inf	Scan point setting
POINT_12	O	Float	-inf to inf	Scan point setting
POINT_13	O	Float	-inf to inf	Scan point setting

---

[8] Not yet implemented

POINT_14	O	Float	-inf to inf	Scan point setting
POINT_15	O	Float	-inf to inf	Scan point setting

8.2   Appendix 2 – Definitions of Result Tables

TSTMODIV: tag "%DetModIV"[9]

Column Name		Representation	Range	Comment
TEMPERATURE	M	Float		For compatibility with existing IV table (=T0)
I_LEAK_150	M	Float	0 to 5200	Leakage Current (μA)
I_LEAK_350	M	Float	0 to 5200	Leakage Current (μA)

TSTHYBRESET: tag "%HardReset"

Column Name		Representation	Range	Comment
ICC_NOCONFIG	M	Float	0 to 2000	Analogue Current (mA)
IDD_NOCONFIG	M	Float	0 to 2000	Digital Current (mA)
ICC_NOCLOCK	M	Float	0 to 2000	Analogue Current (mA)
IDD_NOCLOCK	M	Float	0 to 2000	Digital Current (mA)

TSTHYBPIPE: tag "%PipelineTest"

Column Name		Representation	Range	Comment
M0_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S1_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S2_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S3_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S4_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
E5_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
M8_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S9_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S10_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S11_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S12_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
E13_NGOOD	M	Int (8 bit)	0 to 128	No. good channels

TSTHYBBPASS: tag "%FullBypassTest"

Column Name		Representation	Range	Comment
M0_TOKEN	M	Float	0 to 10 V	
M0_RTOKEN	M	Float	0 to 10 V	
S1_TOKEN	M	Float	0 to 10 V	
S1_RTOKEN	M	Float	0 to 10 V	
S2_TOKEN	M	Float	0 to 10 V	
S2_RTOKEN	M	Float	0 to 10 V	
S3_TOKEN	M	Float	0 to 10 V	
S3_RTOKEN	M	Float	0 to 10 V	
S4_TOKEN	M	Float	0 to 10 V	

---

[9] Prior to version 3.21, the tag "%ModIVScan" was used, however the tag "%DetModIV" is required for DB compatibility. When uploading old data, this change is affected by the java upload application "jSCTDAQ".

S4_RTOKEN	M	Float	0 to 10 V	**FORWARD ONLY**
E5_TOKEN	M	Float	0 to 10 V	**FORWARD ONLY**
E5_RTOKEN	M	Float	0 to 10 V	
M8_TOKEN	M	Float	0 to 10 V	
M8_RTOKEN	M	Float	0 to 10 V	
S9_TOKEN	M	Float	0 to 10 V	
S9_RTOKEN	M	Float	0 to 10 V	
S10_TOKEN	M	Float	0 to 10 V	
S10_RTOKEN	M	Float	0 to 10 V	
S11_TOKEN	M	Float	0 to 10 V	
S11_RTOKEN	M	Float	0 to 10 V	
S12_TOKEN	M	Float	0 to 10 V	
S12_RTOKEN	M	Float	0 to 10 V	**FORWARD ONLY**
E13_TOKEN	M	Float	0 to 10 V	**FORWARD ONLY**
E13_RTOKEN	M	Float	0 to 10 V	
M0_COMMENT	M	Char(20)		
M0_RCOMMENT	M	Char(20)		
S1_COMMENT	M	Char(20)		
S1_RCOMMENT	M	Char(20)		
S2_COMMENT	M	Char(20)		
S2_RCOMMENT	M	Char(20)		
S3_COMMENT	M	Char(20)		
S3_RCOMMENT	M	Char(20)		
S4_COMMENT	M	Char(20)		
S4_RCOMMENT	M	Char(20)		**FORWARD ONLY**
E5_COMMENT	M	Char(20)		**FORWARD ONLY**
E5_RCOMMENT	M	Char(20)		
M8_COMMENT	M	Char(20)		
M8_RCOMMENT	M	Char(20)		
S9_COMMENT	M	Char(20)		
S9_RCOMMENT	M	Char(20)		
S10_COMMENT	M	Char(20)		
S10_RCOMMENT	M	Char(20)		
S11_COMMENT	M	Char(20)		
S11_RCOMMENT	M	Char(20)		
S12_COMMENT	M	Char(20)		
S12_RCOMMENT	M	Char(20)		**FORWARD ONLY**
E13_COMMENT	M	Char(20)		**FORWARD ONLY**
E13_RCOMMENT	M	Char(20)		

TSTHYBDELAY: tag "%StrobeDelay"

Column Name		Representation		Comment
M0_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S1_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S2_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S3_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S4_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
E5_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
M8_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S9_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S10_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S11_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S12_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
E13_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
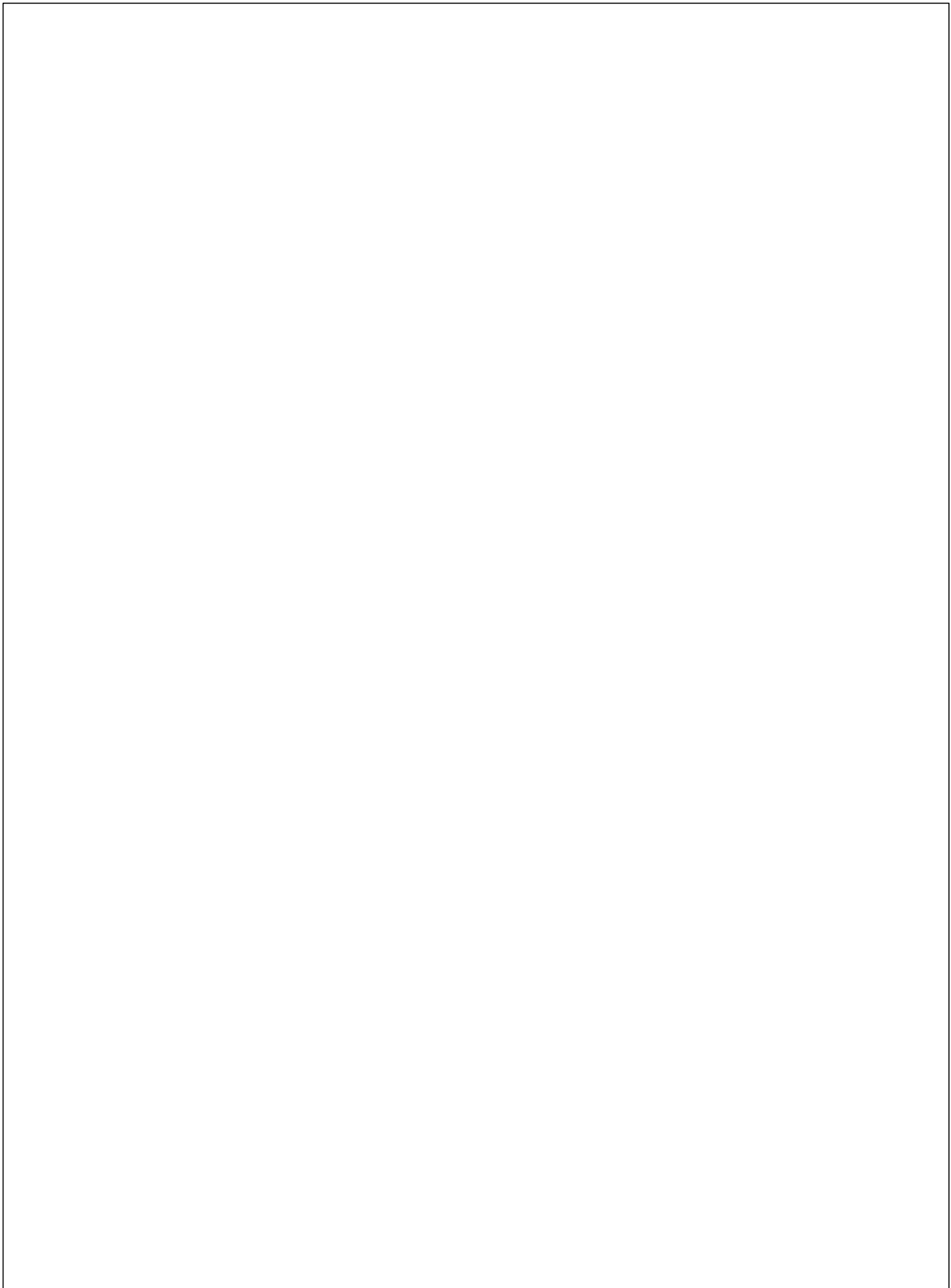
TSTHYBRC: tags "%ThreePointGain" and "%ResponseCurve"

Column Name		Representation	Range	Comment
Loop A				
A_RC_FIT	M	Float[10]	0 to 255	Fit function type
A_RC_P0	M	Float	-inf to inf	Fit parameter 0
A_RC_P1	M	Float	-inf to inf	Fit parameter 1
A_RC_P2	M	Float	-inf to inf	Fit parameter 2
Where A ={M0,S1,S2,S3,S4,E5,M8,S9,S10,S11,S12,E13}				
Loop B				
B_RC_MN_VT50	M	Float	0 to 640	Mean VT50 at 1fC (mV)
B_RC_RMS_VT50	M	Float	0 to 30	RMS VT50 at 1fC (mV)
B_RC_MN_GAIN	M	Float	0 to 100	Mean gain at 2fC(mV/fC)
B_RC_RMS_GAIN	M	Float	0 to 30	RMS gain at 2fC (mV/fC)
B_RC_MN_OFFSET	M	Float	-100 to 120	Extrapolated Offset(mV)
B_RC_RMS_OFFSET	M	Float	0 to 30	RMS Ext. Offset(mV)
B_RC_MN_NSE	M	Float	0 to 120	Mean output noise at 2fC (mV)
B_RC_MN_ENC	M	Float	0 to 5000	Mean input noise at 2fC (ENC)
B_RC_RMS_ENC	M	Float	0 to 1000	RMS input noise at 2fC (ENC)
Where B ={M0,S1,S2,S3,S4,E5,M8,S9,S10,S11,S12,E13}				
Loop C				
B_RC_COMMENT	M	Char(20)	–	Comment
Where C ={M0,S1,S2,S3,S4,E5,M8,S9,S10,S11,S12,E13}				

TSTHYBNOISE: tag "%NO"

Column Name		Representation	Range	Comment
ICC_MAX	M	Float	0 to 2000	Highest Icc (mA)
IDD_MAX	M	Float	0 to 2000	Highest Idd (mA)
ICC_TYP	M	Float	0 to 2000	Icc at 1fC (mA)
IDD_TYP	M	Float	0 to 2000	Idd at 1fC (mA)
Loop A				
A_NO_OFFSET	M	Float	-100 to 120	Noise occupancy offset (mV)
A_NO_MN_OCC	M	Float	0 to 1	Mean Noise occupancy at 1fC
A_NO_RMS_OCC	M	Float	0 to 1	RMS Noise occupancy at 1fC
A_NO_NSE	M	Float	0 to 5000	Estimated noise (ENC)
Where A ={M0,S1,S2,S3,S4,E5,M8,S9,S10,S11,S12,E13}				

---

[10] For reasons of convenience when reading the table into the database

TSTHYBTRIM: tag "%Trim"

Column Name		Representation	Range	Comment
TR_CHARGE	M	Float	-inf to inf	Trim Charge
TR_TYPE	M	Int (8 bit)	-1 to 127	Trim Type (Range)
TR_ALGORITHM	M	Int (8 bit)	0 to 255	Trim Algorithm
Loop A				
A_TR_RANGE	M	Float[11]	0 to 3	Trim Range Setting
A_TR_TARGET	M	Float	0 to 640	Trim Target
A_TR_NTRIM	M	Float[11]	0 to 128	Number of trimmable channels
A_TR_MN_VT50	M	Float	0 to 640	Mean VT50 after trimming (mV)
A_TR_RMS_VT50	M	Float	0 to 120	RMS VT50 After trimming (mV)
A_TR_MN_STEP	M	Float	0 to 20	Mean TrimDAC step (mV)
A_TR_RMS_STEP	M	Float	0 to 10	RMS TrimDAC step (mV)
A_TR_MNOFFSET	M	Float	-120 to 120	Mean TrimDAC Offset (mV)
A_TR_RMSOFFSET	M	Float	0 to 10	RMS TrimDAC offset (mV)
Where A ={M0,S1,S2,S3,S4,E5,M8,S9,S10,S11,S12,E13}				

TSTHYBTW: tag "%Timewalk"

Column Name		Representation	Range	Comment
M0_TW	M	Float	0 to 25	Timewalk (nS)
S1_TW	M	Float	0 to 25	Timewalk (nS)
S2_TW	M	Float	0 to 25	Timewalk (nS)
S3_TW	M	Float	0 to 25	Timewalk (nS)
S4_TW	M	Float	0 to 25	Timewalk (nS)
E5_TW	M	Float	0 to 25	Timewalk (nS)
M8_TW	M	Float	0 to 25	Timewalk (nS)
S9_TW	M	Float	0 to 25	Timewalk (nS)
S10_TW	M	Float	0 to 25	Timewalk (nS)
S11_TW	M	Float	0 to 25	Timewalk (nS)
S12_TW	M	Float	0 to 25	Timewalk (nS)
E13_TW	M	Float	0 to 25	Timewalk (nS)
M0_TCAL	M	Float	-1 to 63	Calibration factor
S1_TCAL	M	Float	-1 to 63	Calibration factor
S2_TCAL	M	Float	-1 to 63	Calibration factor
S3_TCAL	M	Float	-1 to 63	Calibration factor
S4_TCAL	M	Float	-1 to 63	Calibration factor
E5_TCAL	M	Float	-1 to 63	Calibration factor
M8_TCAL	M	Float	-1 to 63	Calibration factor
S9_TCAL	M	Float	-1 to 63	Calibration factor
S10_TCAL	M	Float	-1 to 63	Calibration factor
S11_TCAL	M	Float	-1 to 63	Calibration factor
S12_TCAL	M	Float	-1 to 63	Calibration factor
E13_TCAL	M	Float	-1 to 63	Calibration factor

---

[11] For reasons of convenience when reading the table into the database

TSTHYBLTT: tag "%LongTermTest"

Column Name		Representation	Range	Comment
Duration	M	*Float*	*0 to 1000*	*Duration of test (hours)*
Fail_time	M	*Float*	*-1 to 1000*	*Time of first failure*
T0_min	M	*Float*	*-100 to 200*	*Minimum hybrid temp.*
T0_max	M	*Float*	*-100 to 200*	*Maximum hybrid temp.*
T1_min	M	*Float*	*-100 to 200*	*Minimum hybrid temp.*
T1_max	M	*Float*	*-100 to 200*	*Maximum hybrid temp.*
Icc_min	M	*Float*	*0 to 2000*	*Minimum analogue current*
Icc_max	M	*Float*	*0 to 2000*	*Maximum analogue current*
Idd_min	M	*Float*	*0 to 2000*	*Minimum digital current*
Idd_max	M	*Float*	*0 to 2000*	*Maximum digital current*
Idet_min	O	*Float*	*0 to 5200*	*Minimum detector current*
Idet_max	O	*Float*	*0 to 5200*	*Maximum detector current*

8.3   Appendix 3 – List of Defect Names

Defect	Associated Test(s)	Associated Table(s)	First Channel	Last Channel
IV_LIMIT	IVCurve.cpp	TSTMODIV	0	1535
IV_TRIP			0	1535
HR_NOCLK	HardReset.cpp	TSTHYBRESET	Link * 768	((Link+1)*768)-1
HR_NOCON			Link * 768	((Link+1)*768)-1
HR_NORST			Link * 768	((Link+1)*768)-1
CLK_ADDR0	RedundancyTest.cpp	none	Chip * 128	((Chip+1)*128)-1
CLK_ADDR1			Chip * 128	((Chip+1)*128)-1
CLK_COM0			Chip * 128	((Chip+1)*128)-1
CLK_COM1			Chip * 128	((Chip+1)*128)-1
CLK_ERROR			Chip * 128	((Chip+1)*128)-1
TOKEN	FullBypassTest.cpp	TSTHYBBPASS	Chip * 128	((Chip+1)*128)-1
RTOKEN			Chip * 128	((Chip+1)*128)-1
DEAD	PipelineTest.cpp	TSTHYBPIPE	Channel	Channel
STUCK			Channel	Channel
DEADCELL			Channel	Channel
STUCKCELL			Channel	Channel
SD_LO	StrobeDelay.cpp	TSTHYBDELAY	Chip * 128	((Chip+1)*128)-1
SD_HI			Chip * 128	((Chip+1)*128)-1
DEAD	ThreePointGain.cpp ResponseCurve.cpp	TSTHYBRC	First Channel	Last Channel
STUCK			First Channel	Last Channel
LO_GAIN			First Channel	Last Channel
HI_GAIN			First Channel	Last Channel
LO_OFFSET			First Channel	Last Channel
HI_OFFSET			First Channel	Last Channel
UNBONDED			First Channel	Last Channel
PARTBONDED			First Channel	Last Channel
NOISY			First Channel	Last Channel
INEFF			First Channel	Last Channel
TR_RANGE	TrimRange.cpp	TSTHYBTRIM	Chip * 128	((Chip+1)*128)-1
TR_STEP			First Channel	Last Channel
TR_OFFSET			First Channel	Last Channel
TR_NOTRIM			First Channel	Last Channel
NO_HI	NO.cpp	TSTHYBNOISE	First Channel	Last Channel
TW_LO	Timewalk.cpp	TSTHYBTW	First Channel	Last Channel
TW_HI			First Channel	Last Channel

8.4 Appendix 4 – Database table implementation status

Table	Table approved for addition to DB	Table added to the DB	File format approved for Java Application	Java Application Implemented
TSTDAQINFO	**YES**	**YES**	**YES**	**YES**
TSTDCSINFO	**YES**	**YES**	**YES**	**YES**
TSTSCANINFO	**YES**	**YES**	**YES**	**YES**
TSTMODIV	*Already exists as **TSTDETIV***			
TSTHYBRESET	**YES**	**YES**	**YES**	**YES**
TSTHYBCLOCK	**YES**	**YES**	**YES**	**YES**
TSTHYBBPASS	**YES**	**YES**	**YES**	**YES**
TSTHYBPIPE	**YES**	**YES**	**YES**	**YES**
TSTHYBDELAY	**YES**	**YES**	**YES**	**YES**
TSTHYBRC	**YES**	**YES**	**YES**	**YES**
TSTHYBTRIM	**YES**	**YES**	**YES**	**YES**
TSTHYBNOISE	**YES**	**YES**	**YES**	**YES**
TSTHYBTW	**YES**	**YES**	**YES**	**YES**
TSTHYBLTT	**NOT YET**	**-**	**-**	**-**

8.5 Appendix 5 – Changes to the upload file format between versions 3.20 and 3.21

Between SCTDAQ/document versions 3.20 and 3.21, implementation of the DB tables and java upload applications has started. A few minor inconsistencies have been found which have required changes to be made to the format of the results file. These are outlined below. For users wishing to upload data created with SCTDAQ version 3.20, corrections are applied by the java upload application "jSCTDAQ".

IVCurve.cpp

The results of this test are stored in the table TSTDETIV, which already exists in association with the tag "%DetModIV". Hence to eliminate the need to change the java upload application, the tag has been changed to match that which had already been defined.

SCAN_INFO utility table

This table contains 16 fields in which scan point settings may be recorded. For DB upload, all unused fields in the results file must be filled with a dot. They had previously been left blank.

HybridLTT.cpp, HybridColdTest.cpp and Module LTT.cpp

In version 3.20 of the interpreted class TLTT, which underpins these tests, the "%TEST Rawdata" tag was not generated correctly. This has now been fixed.

9 References

[1] ATLAS SCT Barrel Module FDR, ATLAS-SCT-BM-FDR-7

[2] The Quality Assurance of the ATLAS SCT End-Cap Detector Modules, ATL-IS-QA-0004

[3] The Atlas SCT Production Database, ATL-INDET-2002-015

[4] W. Dabrowski et al., "The ABCD Binary Readout Chip for Silicon Strip Detectors in the ATLAS Silicon Tracker", CERN/LHCC/98-36, p175

[5] RD29 Status Report: "DMILL, A Mixed Analog-Digital Radiation Hard Technology for High Energy Physics Electronics", CERN/LHCC/97-15

[6] http://sct-testdaq.home.cern.ch/sct-testdaq/sctdaq/sctdaq.html

[7] http://root.cern.ch/

[8] http://www.hep.phy.cam.ac.uk/~silicon/jSCTDAQ.html

[9] http://www.hep.man.ac.uk/groups/atlas/SCTdatabase/TableDef.html

[10] http://www-ucjf.troja.mff.cuni.cz/~sct/tests/beta/

[11] http://atlas.web.cern.ch/Atlas/GROUPS/INNER_DETECTOR/SCT/testbeam/

[12] http://atlas-sct-irradiation.web.cern.ch/atlas-sct-irradiation/default.htm