EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN/SPSC 87 – 14
SPSC/P93 Add. 4

PROPOSAL FOR THE INSTALLATION OF A SECOND SILICON ARRAY IN THE UA2 DETECTOR

The UA2 Collaboration

Bern - Cambridge - CERN - Heidelberg - Milan -
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ABSTRACT

We propose to equip the inner region of the UA2 detector with an additional array of silicon counters in order to enhance its pattern recognition capabilities. Experience with a similar array in the UA2 environment gives us confidence in the reliability and quality of the expected performance. The necessary miniaturization is made possible by the expected availability of ASIC electronics developed at CERN in the EF Division. Time table and financial considerations are presented in some detail and lead us to propose the installation of the array in UA2 between the 1987 and 1988 data taking periods.

1. INTRODUCTION

The UA2 detector is presently being modified [1] in order to reach improved performance matching that of the upgraded $\bar{p}p$ Collider [2]. Construction and installation are proceeding according to schedule and we shall be able to take data as soon as the Collider resumes operation in 1987. In particular a completely new central detector is presently being assembled (Figure 1). It serves two main functions, electron identification and tracking. The former is achieved using mostly a preshower detector, a transition radiation detector and an array of silicon counters [3] providing significant rejection against converted photons. The latter also uses the silicon array but it rests mainly on two tracking detectors located in the innermost and outermost regions respectively : the jet vertex detector (JVD) and the scintillating fibre detector (SFD). Several space points are provided by each of these two detectors along a track. In the JVD case combined measurements of drift time and charge division are available on each wire and are complemented by cathode strip localisation on the outer detector shell. In the SFD case the fibres are arranged in six layers of small angle stereoscopic triplets. Both detectors taken together will have powerful pattern recognition capabilities and will provide the track localisation accuracy and the resolving power between neighbour tracks which are necessary to reach high performance in electron identification. However, the detailed elaboration of their data involves processing complex algorithms and is a time consuming operation, in particular in the case of high multiplicity events (resulting either from multivertex collisions or from the production of several hadron jets). It also implies using extensive calibration data, most of which are only available after off-line processing of a fraction of the events. In contrast, the information provided by the silicon array can be immediately presented as a space pattern (it can even be used on-line) but the achieved accuracy is not as good as in the SFD + JVD case. Experience with a restricted coverage silicon array, installed in UA2 during the 1985 data taking period, has shown the high detection efficiency and the low background and noise levels to be such that the detector can be reliably used to guide and ease pattern recognition. The vertex location along the beam being a priori unknown, the reconstruction of the track pattern based on silicon counters only can be made possible with a second array of similar solid-angle granularity and located at adequate radial distance from the first array. Its presence would enable an instantaneous and accurate localisation of the event vertex (or vertices).

From our former experience with problems of pattern recognition in the UA2 environment, we are convinced that the addition of a second silicon array (hereafter refered to as the "inner array") would provide UA2 with a very powerful tool, well matched to both our on-line and off-line needs, and would significantly enhance our efficiency at analysing data. The savings which would result in terms of effort and of computer time largely outscale the relatively low construction cost. We shall develop these arguments in Section 3 after having given a brief description of our experience with a restricted coverage silicon array (a fraction of the already approved "outer array") in Section 2. The proposed design is presented in Section 4 and Section 5 deals with matters of time table and of finance.

2. EXPERIENCE WITH THE PRESENT SILICON HODOSCOPE

During the 1985 data taking period the UA2 detector was equipped with an array of silicon counters (a fraction of the approved outer array) of limited coverage ($\simeq 45°$ in azimuth ϕ and $\sim 60°$ in polar angle θ) at a distance of $\simeq$ 15 cm from the beam line. Details of its construction and performance have been presented elsewhere [3,4]. In addition a large number of silicon counters have been exposed to electron, pion and muon beams of various energies in 1986. In the present Section we summarize briefly our understanding of this detector, illustrating our presentation with some of the most representative features.

The detector geometry is shown in Figure 2 and a photograph of a silicon counter, with its seven 8.7×40 mm^2 independent pads, is shown in Figure 3a. The whole array includes 432 such counters (3024 pads), of which only 25 were installed in UA2 during the 1985 data taking period. Each counter

is mounted on a fiberglass printed circuit board (see Figure 3b) equipped with 7-channel hybrid preamplifiers [5]. The amplified signals are shaped and analysed in three 16-channel ADC using an external multiplexed readout scheme.

Pulse height distributions obtained with traversing particles are shown in Figures 4a and 4b. The distribution in Figure 4a is for tracks reconstructed in the UA2 central detector as hitting the silicon counter pad in which the pulse height is measured. Requiring that neighbour pads contain no significant pulse height, rejects tracks near the pad boundary (for those, however, the summed pulse height of adjacent hit pads has a distribution very similar to that of Figure 4a). The rare occurence ($\simeq$ 4%) of zero pulse heights is consistent with the probability that the reconstucted track is in fact a "ghost" resulting from pattern recognition ambiguities. Their distribution is well separated from that measured for real tracks. Figure 4b is for 220 GeV μ^- from a SPS test beam. Drift chambers located along the beam are used to locate the incident particle and to require that it hits the pad under study. This is done with limited accuracy and explains the presence of a small fraction of events (2.8%) having zero pulse height. From both distributions we infer a detection efficiency in excess of 99% : we have in fact no evidence for any inefficiency and the rare occurence of zero pulse-height events (well separated from the real signal) is explained by other sources. The data in Figure 4 provide evidence that the silicon array can be reliably and efficiently used to reject spurious tracks in a complex track pattern. Figures 5 and 6 provide the complementary evidence that the noise and background levels in the UA2 environment are low. They show patterns of hit pads for a $W \rightarrow e\nu$ event and for a typical large transverse momentum jet pointing to the silicon array. We estimate the probability to measure a spurious pulse height in a given pad (resulting from noise or from background) not to exceed 2.10^{-4}, corresponding to ~ 4% of the average occupancy in minimum bias events (and therefore less when compared to large transverse energy triggers). This is in fact an upper limit since no correction has been made for track reconstruction inefficiency.

We conclude this Section with data related to the ionization measurement. Although less important for the present proposal they provide additional evidence for the quality of the detector performance. Figure 7 shows the pulse-height distribution measured at the SPS in a 150 GeV electron beam contaminated by electron pairs produced in an upstream radiator. The curve superimposed on the data is obtained from the response to a single electron predicted by theory (see Figure 4) and used to generate the response to an electron pair (each member of which is assumed to act independently). The relative contribution of the pair distribution is adjusted to best fit the data and an excellent agreement is achieved in the valley between the two peaks. The tail at larger pulse heights can be ascribed to higher multiplicity contamination. Figure 8 illustrates the independence of the measured pulse height on particle velocity. This results from energetic δ-rays (partly responsible for the relativistic rise of the energy loss, see the smooth curve) escaping the thin silicon counter, an effect which depresses the Landau tail and narrows the one-particle peak, thereby improving the separation between one and two particles [6].

3. THE INNER SILICON ARRAY : MOTIVATION AND JUSTIFICATIONS

From the pattern of hit pads in the outer array we obtain an instantaneous "photograph" of the pattern of track intersects. The inner array, providing this information at another radius, would then make it possible to draw tracks between hit pads. This information, obtained immediately, would be of invaluable help in speeding up pattern recognition. Before developing this argument it is useful to remember the main specific features of the tracking problem in UA2 :

– the absence of magnetic field results in straight tracks, vertices have an approximately gaussian distribution along the beam ($\sigma \simeq 11$ cm) and multivertex events (i.e. accompanied by another $\bar{p}p$ collision in the same bunch crossing) are expected to occur in at least $^1/_3$ of the cases at design luminosity,

– the compactness of the UA2 central calorimeter leaves little room for tracking (a radius of 45 cm), of which 16 cm is occupied by the polypropylene radiators of the TRD. The SFD, the JVD and the outer array occupy radial spaces of 6, 10 and 3 cm respectively. A radial space of approximately 0.6 cm was recently made available by adopting a smaller diameter vacuum chamber [7]. We propose to install the inner array in this space, between the JVD and the new chamber,
– the required accuracy is mostly dictated by the need for an unambiguous match of the track segments measured in the various detectors : JVD, silicon array, TRD, SFD, preshower detectors and calorimeters. This contrasts with other experiments equipped with a magnetic field, for which the dominant factor is momentum measurement accuracy. Here, instead, the essential feature is the ability to identify electrons, a task requiring an unambiguous identification of the electron track and a good resolving power against neighbour tracks. It must be performed in the high multiplicity environment characteristic of large transverse energy events.

For the inner array to serve its purpose, its solid angle granularity must approximately match that of the outer array. We propose a segmentation in 3072 pads (192 counters of 16 pads each), each pad measuring 2 mm along the beam and covering a 30° azimuth interval in the orthogonal direction (Figure 9). These dimensions are dictated by the average radius, $\simeq$ 3 cm, of the second silicon array. In particular the azimuthal coverage of each counter is twice that achieved in the outer array for feasibility reasons. Such a geometry implies, for tracks joining hit pads in each of the two arrays, a measurement accuracy of $\simeq$ 1 mm for their intersect along the beam line, a direct consequence of the small pad width of the inner array and of its proximity to the beam line. A detailed description of the proposed design is given in the next Section. Here, we first discuss the expected performance.

A simple algorithm has been written to test the effectiveness of the double layer silicon system for pattern recognition. A histogram is plotted of the intersection points with the beam axis of each pair of hits in the inner and outer layers, lying in each 30° ϕ sector defined by the inner modules (it must be remembered that the position of the collision point in the plane normal to the beams is known a priori to better than 1 mm). Since the tracks radiate in straight lines from the vertex point, it is seen as a clear peak on a small combinatorial background. The vertex resolution found for single minimum bias events is $\leq$ 1 mm. This improves for higher multiplicity events obtained from large transverse energy triggers (Figure 10).

The method can easily be used for multiple vertex events, by removing the hits contributing to the most prominent peak and performing a new search with the remainder. A two vertex separation of $\sim$ 1 cm is achieved. Figure 11 shows the result of a Monte Carlo simulation of

$$\begin{aligned} \bar{p}p &\rightarrow WX \\ W &\rightarrow t\bar{b} \\ t &\rightarrow b e \nu \end{aligned}$$

with an independent minimum bias event superimposed. Two different representative events are displayed. After the first pass the position of the main vertex is clearly seen, while the second vertex does not stand out until a second pass is performed.

The algorithm is intrinsically fast, taking 0.03 IBM 168 secs per pass with no optimisation. This compares with an estimated 15 IBM 168 secs for a full event reconstruction. Since the method provides narrow roads in which to search for tracks, a substantial improvement in the overall processing time would be achieved. In addition the method could be used online to monitor the vertex distribution and double event rate.

4. PROPOSED DESIGN

The 192 silicon counters are attached to a carbon fibre cylinder fitting tightly around the vacuum chamber as shown in Figure 9. They are assembled in 12 rows of 16 counters each, each having an azimuthal width of 16.4 mm. The whole set up fits in the cylindrical space between 5.6 and 6.7 cm diameters and has a length of 55 cm along the beam. The counters of one row overlap with those of the next row in order to achieve nearly full coverage. Each counter is equipped with its associated electronics as described below. It is 300 μm thick and is operated under full depletion at a reverse bias voltage between 50 and 90 V. On average, the total detector thickness, including supports and electronics, does not exceed 0.02 radiation lengths (note that pulse height measurement is available from each pad, thereby providing additional rejection against converted photons). Once the detector is assembled on the carbon fibre support cylinder its installation in UA2 requires a shut-down period of about two months, in order to remove the vacuum chamber and the JVD, and reinsert them after having added the inner array. This operation implies no significant disturbance to the rest of the UA2 detector.

Ceramic printed circuits are used to connect each counter to its associated electronics, a 16-channel CMOS chip "AMPLEX" [8] including preamplifiers, shaping amplifiers, track-and-hold and multiplexing. Daisy-chained bus lines running on the ceramic plates of a same row are used for readout purpose and for supplying necessary DC voltages. Several connection schemes are presently under study with the aim to find the best compromise between conflicting requirements such as ease of repairs and rigidity of the assembly. The total power dissipation, estimated between 3 and 10 W, is taken care of by a nitrogen gas flow cooling the detector along its whole length.

The Application Specific Integrated Circuit (ASIC) chip, developed by P. Jarron, contains 16 FET preamplifiers followed by track-and-hold and multiplex stages (Figure 12 and Table 1). It uses a 3 μm n-well CMOS processing, available to CERN via a collaboration with IMEC in Leuven (Belgium). A 4-channel prototype, presently in production, will be available for tests by the end of April. We shall use the same multiplex readout scheme with FERA-ADC's [9] as presently used for the outer array and for ECPT's. One FERA-ADC channel digitizes the signals of 8 AMPLEX chips, i.e. the multiplex level is 128, and 24 ADC-channels (2 ADC modules) are required. The multiplexer outputs of the 16 AMPLEX chips of each row of counters are connected via two common analog signal lines to low power output amplifiers. The multiplexer switches are controlled by a shift-register logic on the AMPLEX chip, allowing for cascading of the 8 chips connected to a common analog signal line. Data reduction after digitization is done within the existing UA2 data acquisition framework and requires no additional hardware.

We have performed measurements of possible radiation damage to both the counters themselves and the CMOS chips. These include 00334 irradiations with radioactive sources, exposures to a 300 GeV pion beam and studies perform the UA2 environment. No significant deterioration is expected over the expected duration of the UA2 experiment [4].

5. TIME TABLE AND COST

The production of the 16-channel chip would take place in January 1988 after having tested the prototype circuits produced in Autumn 1987. However, no major surprise is expected once the 4-channel prototype, to be available before end April 1987, has been thoroughly tested.

We therefore expect that by early June 1987 our confidence in the time table will be on solid ground. By that time our studies of the various possible connection schemes will be completed, we shall start receiving counter prototypes and the main tests of the ASIC electronics will have been performed. Very little money ($\simeq$ 30 kSF) will have been committed by then. We shall then review the main deadlines before deciding on major series order (silicon counters, ASIC chips, and associated equipment).

The array would be assembled in the laboratory between February 1st 1988 and May 31st 1988, leaving the months of June and July for installation in LSS4. We should then be ready to take data starting August 1st 1988, as soon as the Collider resumes operation. A summary of the main milestones is presented in Table 2.

Table 3 gives a summary of the expected cost. We have asked possible manufacturers for offers in relation with the silicon counters proper and shall receive answers in March. No major surprise is to be expected on any of the quoted items. We are presently enquiring about means of sharing the detector costs among the various collaborating Institutes in UA2. From preliminary contacts we believe that about 50% of the total cost could be contributed by the Institutes outside CERN. We repeat that the savings in computer time which this detector will allow largely outweigh its relatively low production cost.

We should like to ask the SPS Committee to give us an immediate answer on their general reaction to the present proposal in order for us to

i. order silicon counter prototypes,

ii. take official steps with our funding authorities.

Final approval by the Research Board would have to take place early June 1987 if we want to keep the time table and place the main orders in time.

REFERENCES

1. The UA2 experiment at ACOL, the UA2 Collaboration, presented by C.N. Booth at the 6th Int. Conf. on $\bar{p}p$ Physics, Aachen, June 30 - July 4, 1986;
   Proposal to improve the performance of the UA2 detector, CERN/SPSC 84-30 SPSC/P93 Add. 2, May 15th 1984;
   Proposal to improve the performance of the UA2 central detector, CERN/SPSC 84-95 SPSC/P93 Add.3 Dec. 1st 1984;
   UA2 Collaboration, presented by B. Merkel, Proc. 5th topical workshop on $\bar{p}p$ coll. phys. St Vincent, 25 Feb. - 1 March 1985, p.635.

2. Design study of an antiproton collector (ACOL), ed. E.J.N. Wilson, CERN 83-10, Oct. 1983; E. Jones et al., IEEE Trans. Nucl. Sc., Vol NS-30 nr 4, Aug. 1983.

3. K. Borer et al., Nucl. Inst. Meth. A253 (1987) 548.

4. UA2 $\bar{p}p$ note 523 and references therein, 19 November 1986.

5. LABEN type 5315 preamplifier, LABEN, Milano, Italy.

6. H. Esbensen et al., Phys. Rev. B18 (1978) 1039. See also E. Heijne, CERN Yellow Report 83-6, p. 25.

7. Memorandum to P. Pistilli from P. Darriulat and O. Gildemeister dated 22 December, 1986.

8. P. Jarron, "CMOS charge preamplifier", contribution to Int. Conf. on Fast Analog Integrated Circuits for Particle Physics, Univ. of Pennsylvania, 2 - 4 March 1987.

9. LeCroy FERA modules of the 4300 series.

TABLE 1

TARGET SPECIFICATIONS OF 16-CHANNEL AMPLEX CHIP

Number of inputs :		16 at the pitch of 300μm
Chip size	:	5mm*5mm
Signal peaking time:		600nS ,shaping with continuous filtering
Detector dark current:		50nA with inputs DC coupled
Output type	:	analog multiplexed
Charge gain	:	40mV/M.I.P. (90keV in 300μm of silicon)
Dynamic range	:	±1.2V (30 M.I.P.)
Noise performance	:	E.N.C. = 250 r.m.s. electrons at C_{in}=0pF noise slope = 8 e/pF for .5μS shaping time
Power dissipation	:	0.2mW to 6mW/channel adjustable typique 2.5mW/channel ,40mW/chip
Sample and hold	:	voltage drop.rate 10mV/s maximum clocking 400kHz

TABLE 2

Time table

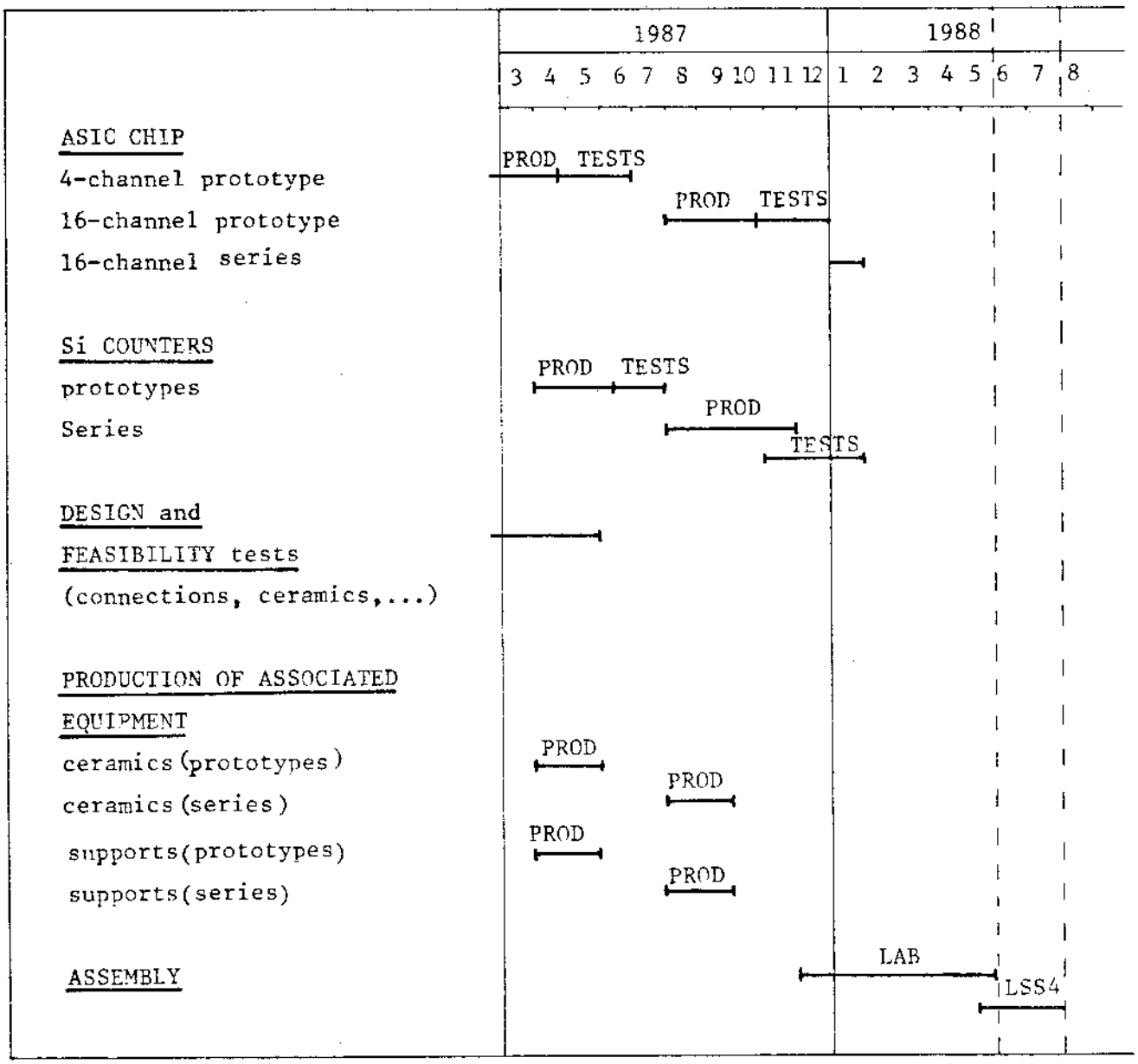


TABLE 3

Material Costs

Item	Cost (kSF)	
Silicon counters	100	166
AMPLEX chips	60	
Ceramics (equipped)	6	
Carbon fibre cylinders	10	34
Flanges	5	
Support profiles	5	
Kapton boards	4	
Conductive rubber	4	
Ceramic spacers	2	
Readout lines	2	
Connectors	2	
Readout electronics	30	45
LV supplies	7	
HV supplies	6	
Cables	2	
Cooling	10	60
Test bench / test electronics	25	
Contingency	25	
Total		305

FIGURE CAPTIONS

1. Schematic assembly of the central UA2 detector cut in a plane containing the beam line (around which the detector has rotational symmetry). The detector is left-right symmetric with respect to the median plane indicated as a dash-dot line.

2. Outer silicon array assembly. The schematic arrangement of the counter rows is shown in the upper part of the figure (cross-section normal to the beam). The lower part of the figure shows a cut across one of the counters.

3. a. Photograph of a counter of the outer array. The seven pads, the guard ring and the connecting pins are visible.

   b. Photograph of two assemblies of 9 counters of the outer array. The upper one is seen from the preamplifier side, the lower one from the silicon side.

4. a. Pulse height distribution measured in the UA2 environment for tracks crossing a counter pad.

   b. Pulse height distribution measured in a 220 GeV μ^- beam. The line across the data is a fit using a Landau distribution convoluted with the resolution obtained from the pedestal shape.

5. Hit pattern measured in the restricted coverage silicon array for a $W \rightarrow e\nu$ event with its decay electron pointing to the array. The full dots are the intersects with the array of tracks reconstructed in the vertex detector of UA2.

6. Hit pattern measured in the restricted coverage silicon array for a typical jet event. The intersect of the jet axis, measured from the central calorimeter energy pattern, is indicated.

7. Pulse height distribution measured in an electron beam containing higher multiplicity contaminations. The curve is a fit to a mixture of single electron and electron pairs using the same theoretical input as in Figure 4b (see text).

8. Dependence on particle velocity of the pulse height measured in counters of the outer array (full dots). The curve shows what the particle energy loss would be in a thick counter (no escaping δ-rays).

9. Schematic assembly of the inner array (cut in a plane orthogonal to the beam). The detector has rotational symmetry around the beam line and only half of it is shown. A top view of a silicon counter, indicating the arrangement of the 16 pads and of the VLSI AMPLEX chip, is shown in the insert.

10. Distribution of the distance (measured along the beam) between actual and reconstructed vertices. The inner and outer arrays alone are used for track reconstruction. The events are typical Monte Carlo events satisfying a large transverse energy trigger.

11. Finding double vertices in Monte Carlo events obtained as a superposition of a Monte Carlo generated $W \rightarrow t\bar{b}$ event with a minimum-bias interaction. Two examples are shown (event A and event B). The vertex of the $W \rightarrow t\bar{b}$ event is found in the first pass (upper figures), the vertex of the minimum-bias interaction is found in the second pass (lower figures).

12. a. Enlarged photograph (x 100) of part of an AMPLEX chip.

    b. Block diagram of the AMPLEX chip.

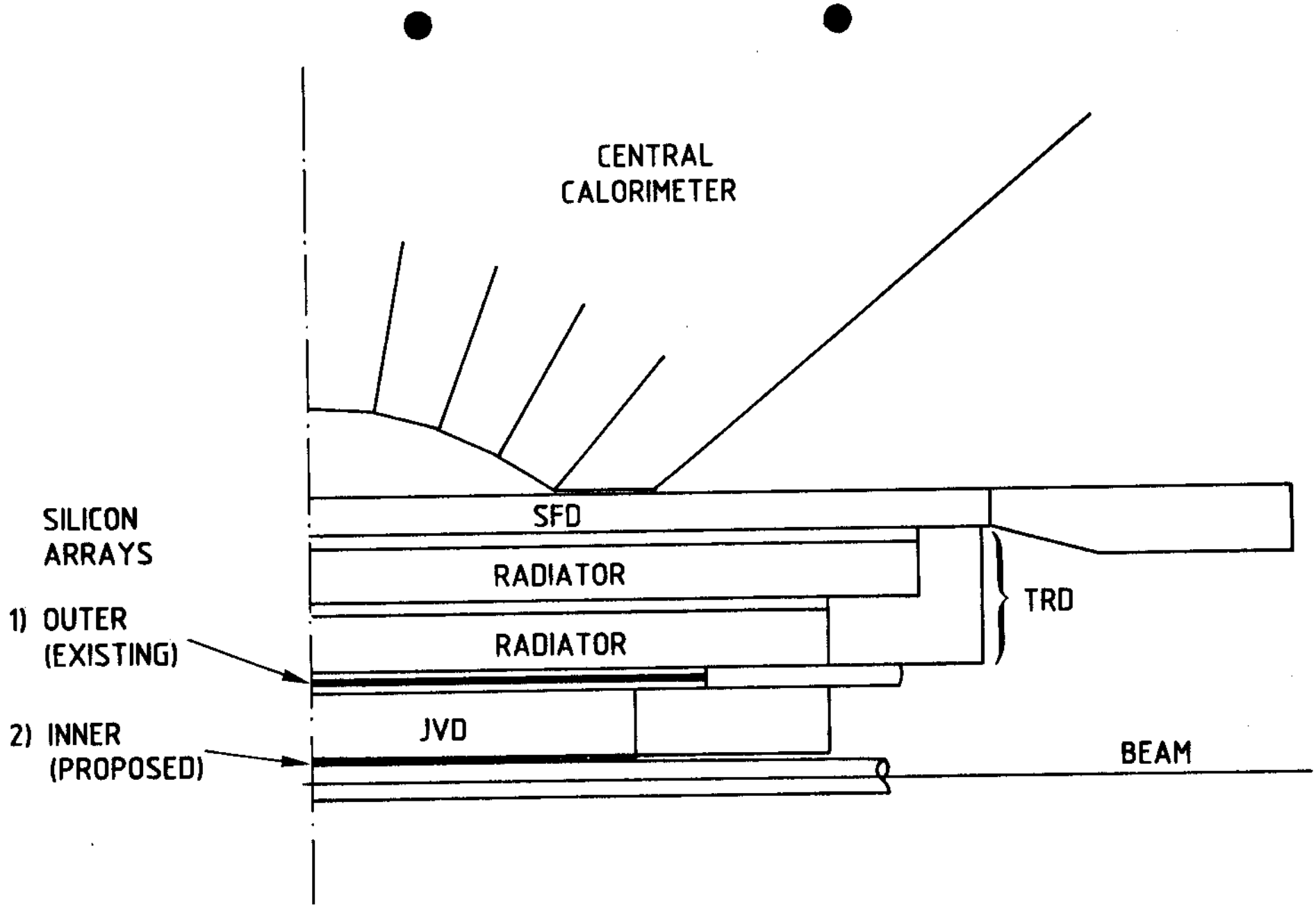
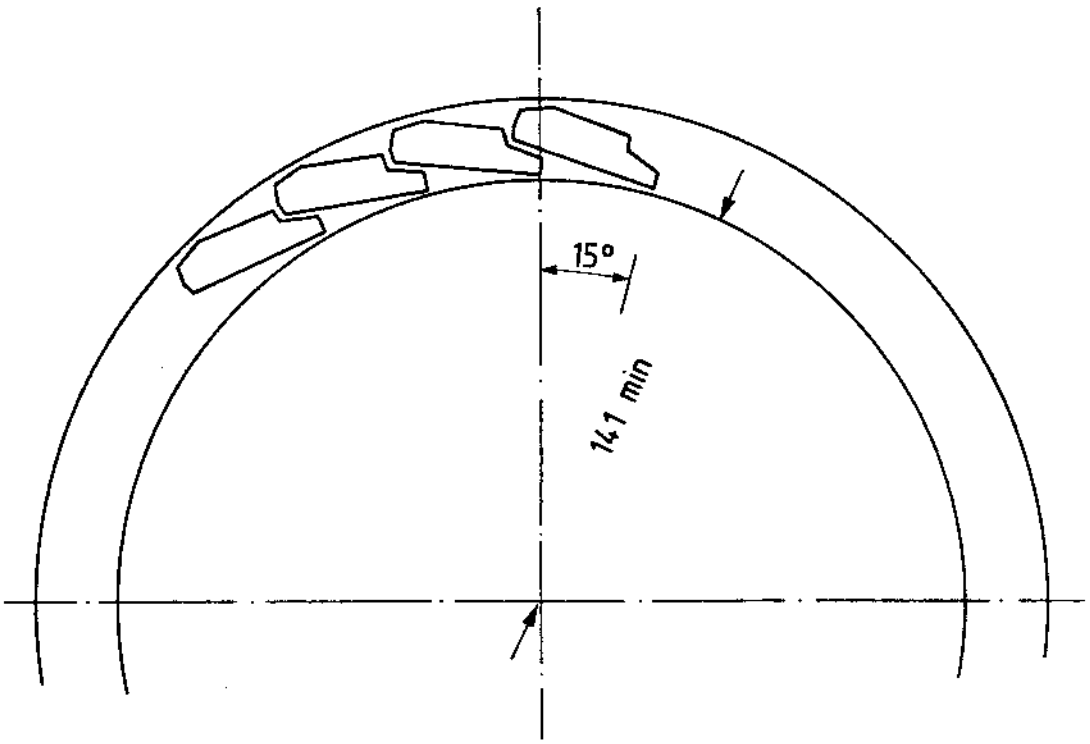

CENTRAL
CALORIMETER
SILICON
ARRAYS
SFD
RADIATOR
TRD
1) OUTER
(EXISTING)
RADIATOR
JVD
2) INNER
(PROPOSED)
BEAM

Figure 1


15°
141 min

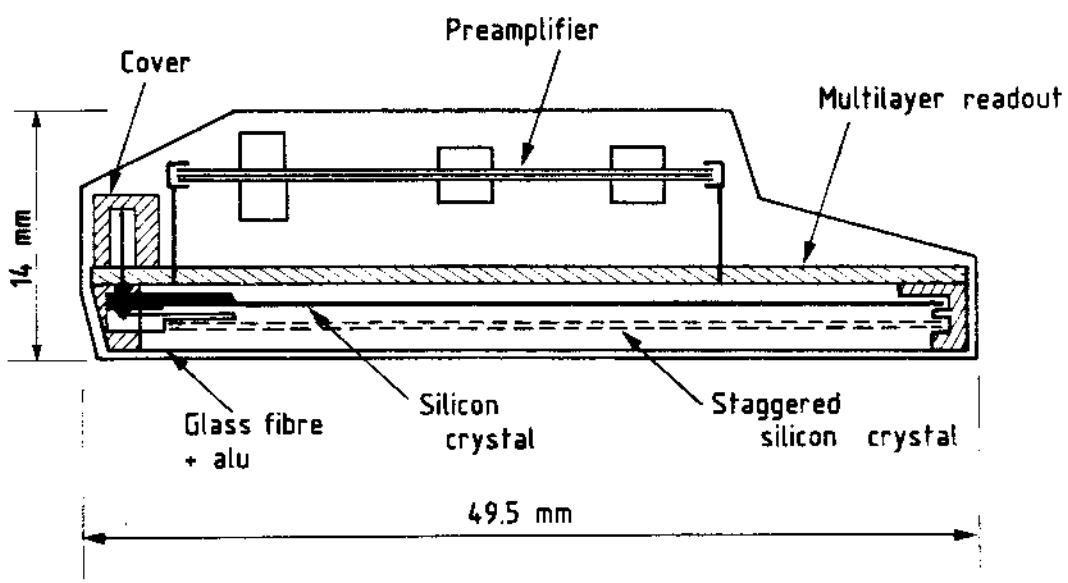

Preamplifier
Cover
Multilayer readout
14 mm
Glass fibre
+ alu
Silicon
crystal
Staggered
silicon crystal
49.5 mm

Figure 2

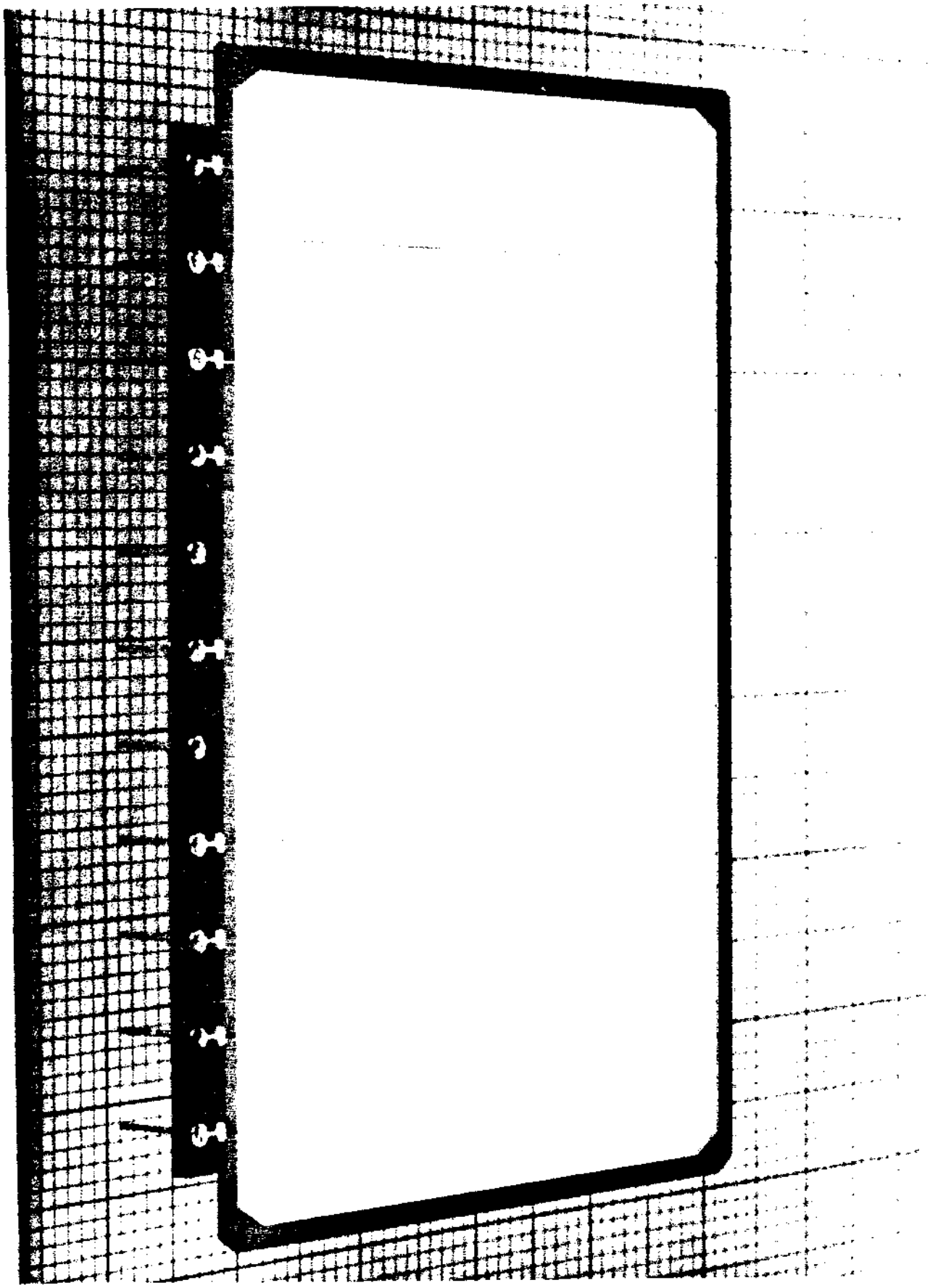


Figure 3a

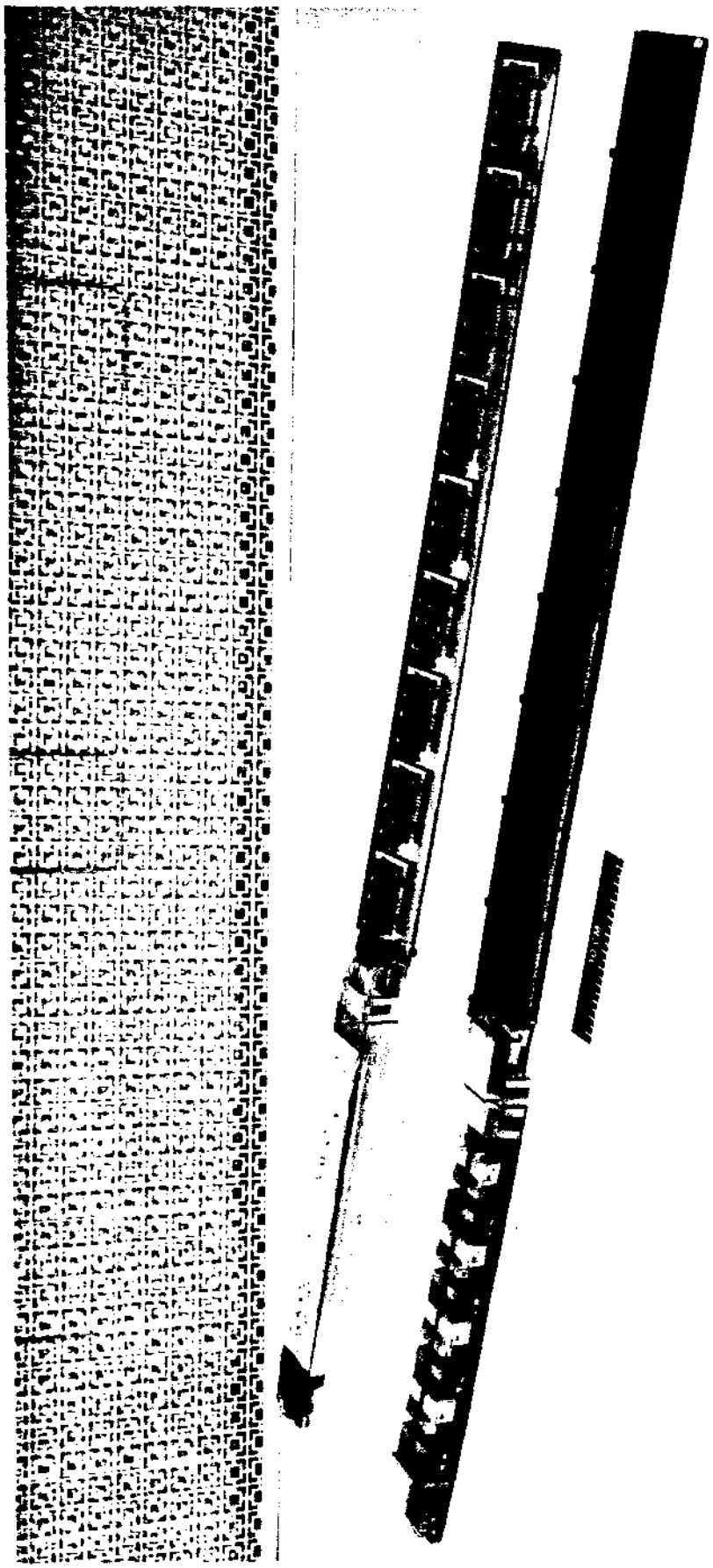


Figure 3b

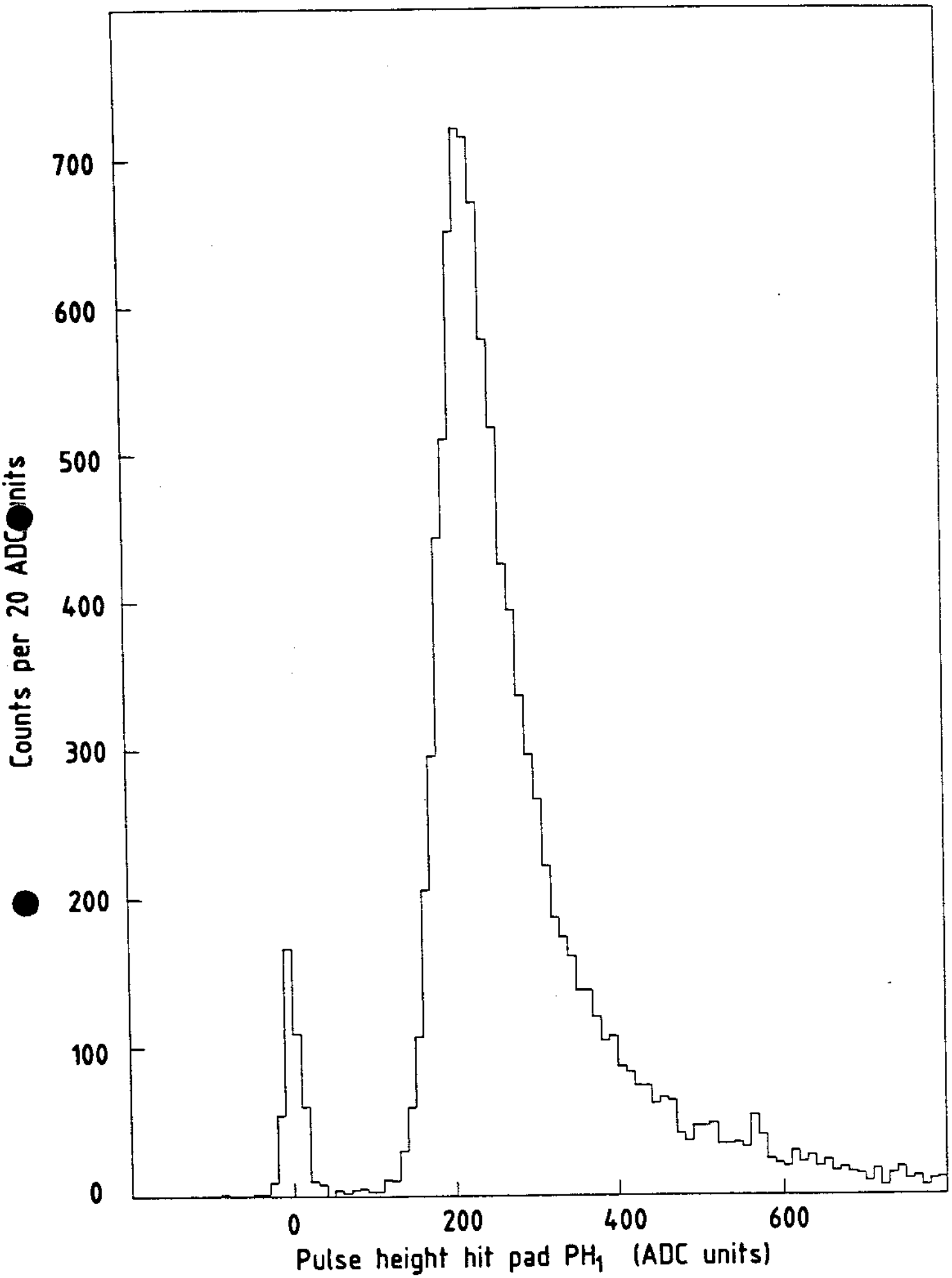

700
600
500
400
300
200
100
0
Counts per 20 ADC units
0
200
400
600
Pulse height hit pad PH1 (ADC units)

Figure 4a

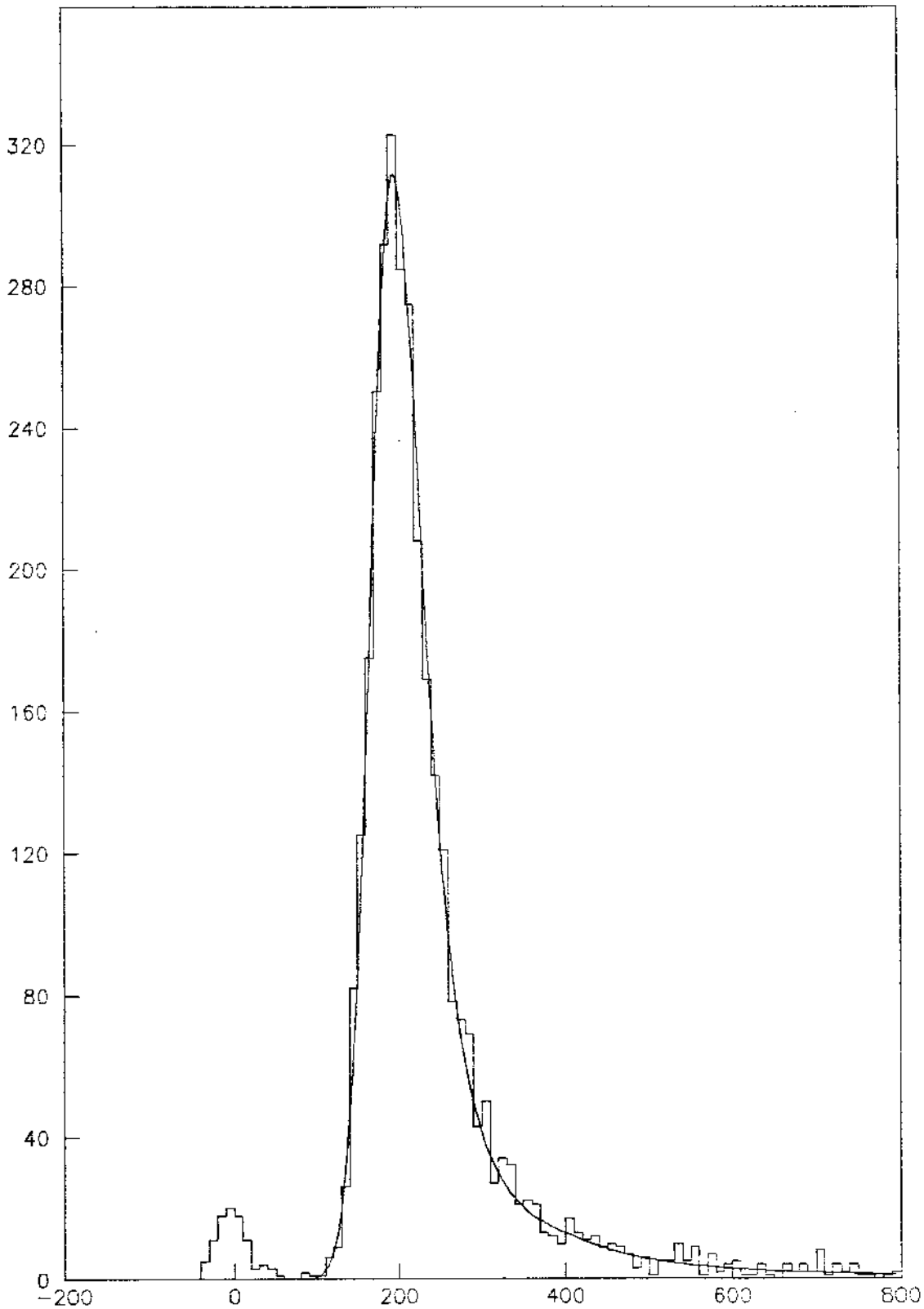

320
280
240
200
160
120
80
40
0
-200
0
200
400
600
800
PULSE HEIGHT (ADC UNITS)

Figure 4b

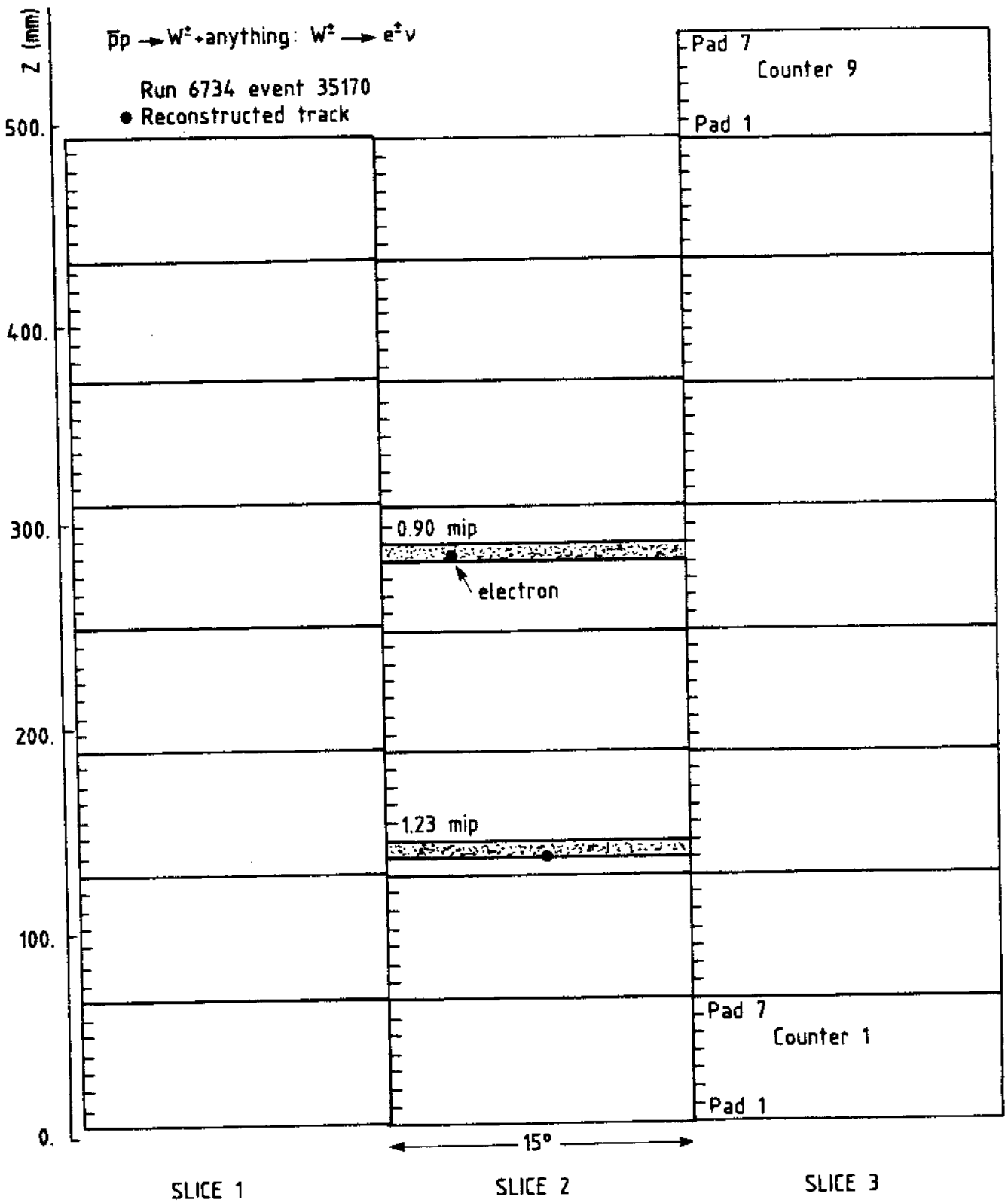

Z (mm)
$\bar{p}p \rightarrow W^{\pm}$+anything: $W^{\pm} \rightarrow e^{\pm}\nu$
Run 6734 event 35170
● Reconstructed track
Pad 7
Counter 9
Pad 1
500.
400.
300.
200.
100.
0.
0.90 mip
electron
1.23 mip
Pad 7
Counter 1
Pad 1
15°
SLICE 1
SLICE 2
SLICE 3

Figure 5

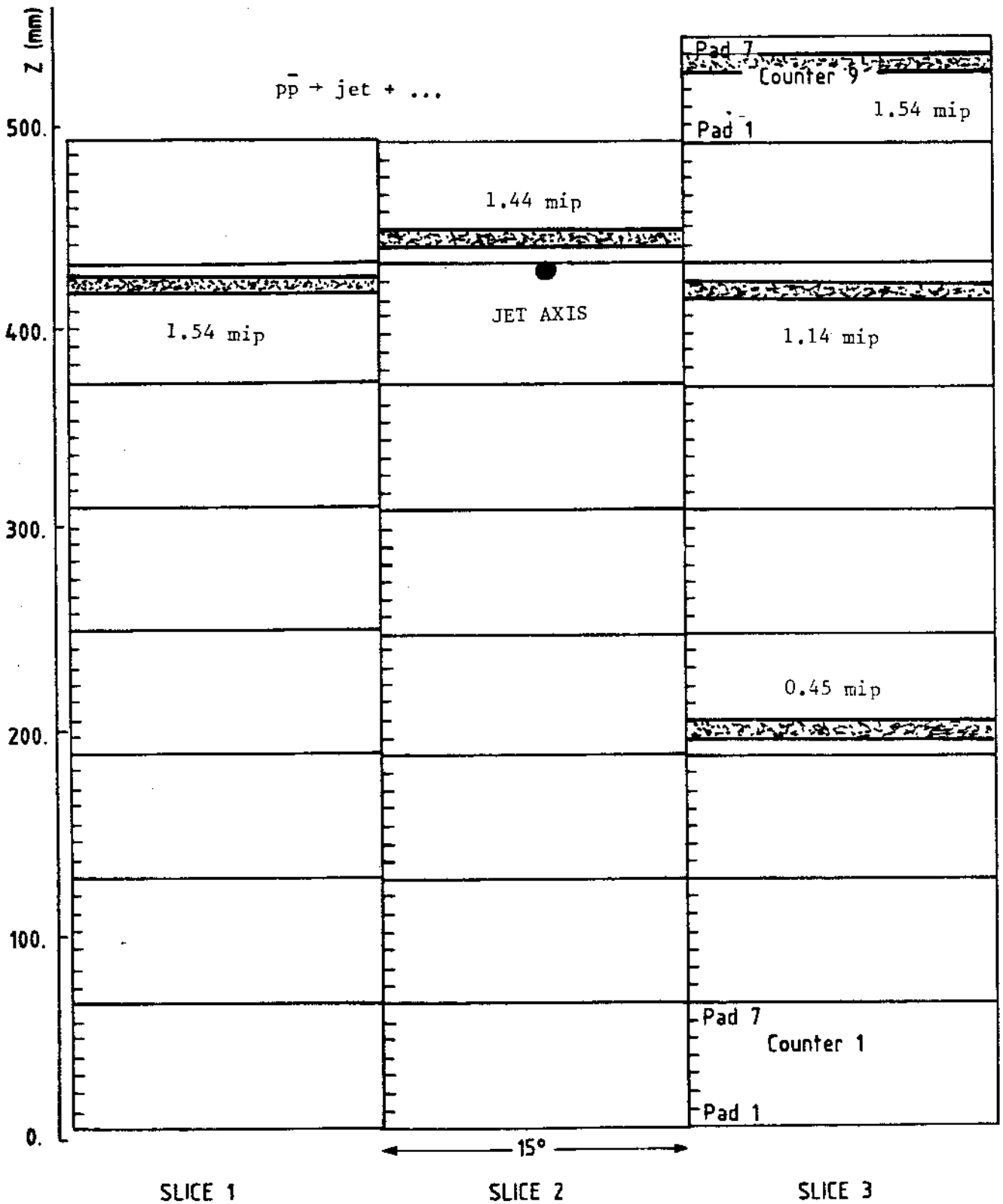

Z (mm)
500.
400.
300.
200.
100.
0.
$p\bar{p}$ → jet + ...
Pad 7
Counter 9
1.54 mip
Pad 1
1.44 mip
JET AXIS
1.54 mip
1.14 mip
0.45 mip
Pad 7
Counter 1
Pad 1
15°
SLICE 1
SLICE 2
SLICE 3

Figure 6

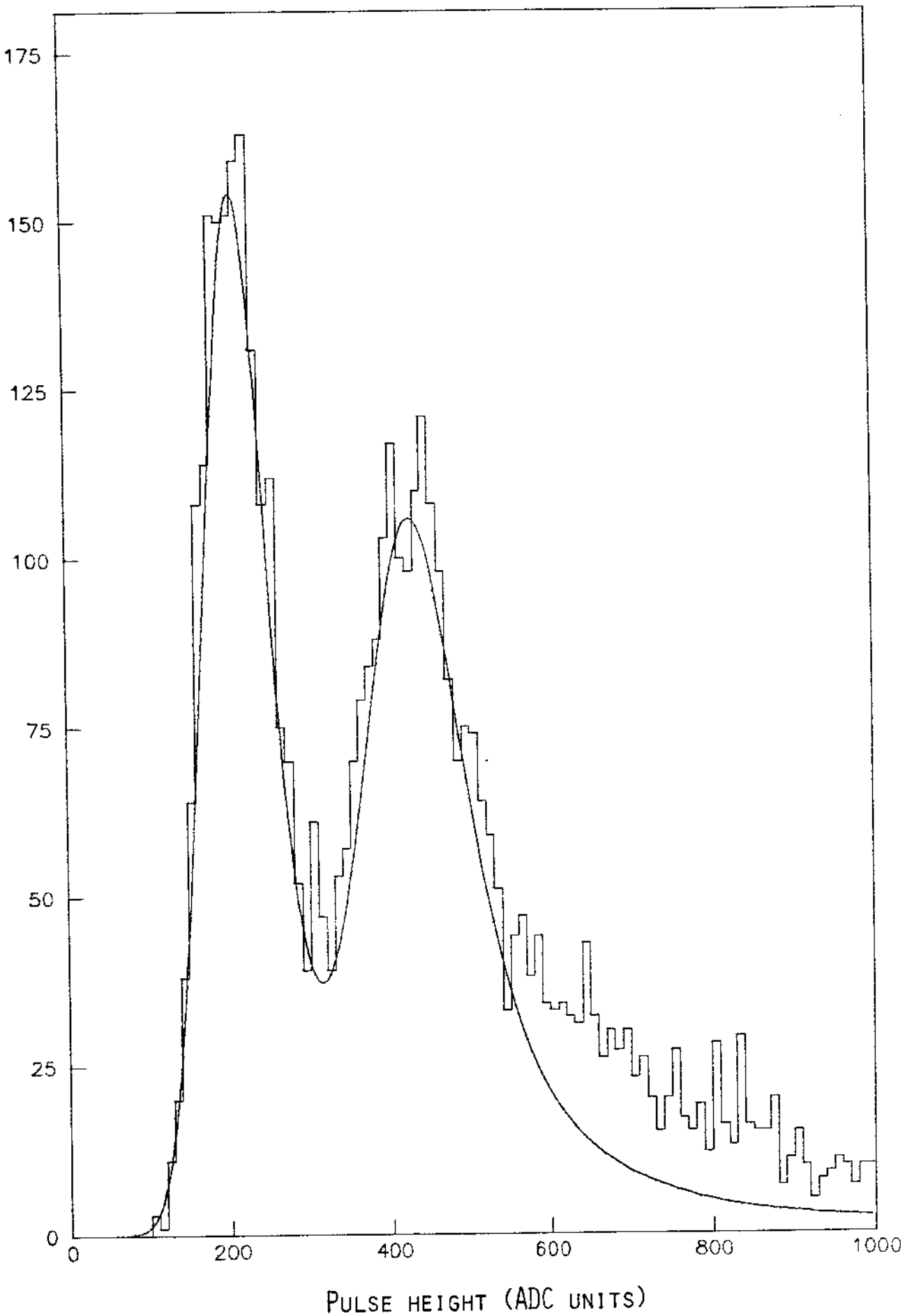

175
150
125
100
75
50
25
0
0
200
400
600
800
1000
PULSE HEIGHT (ADC UNITS)

Figure 7

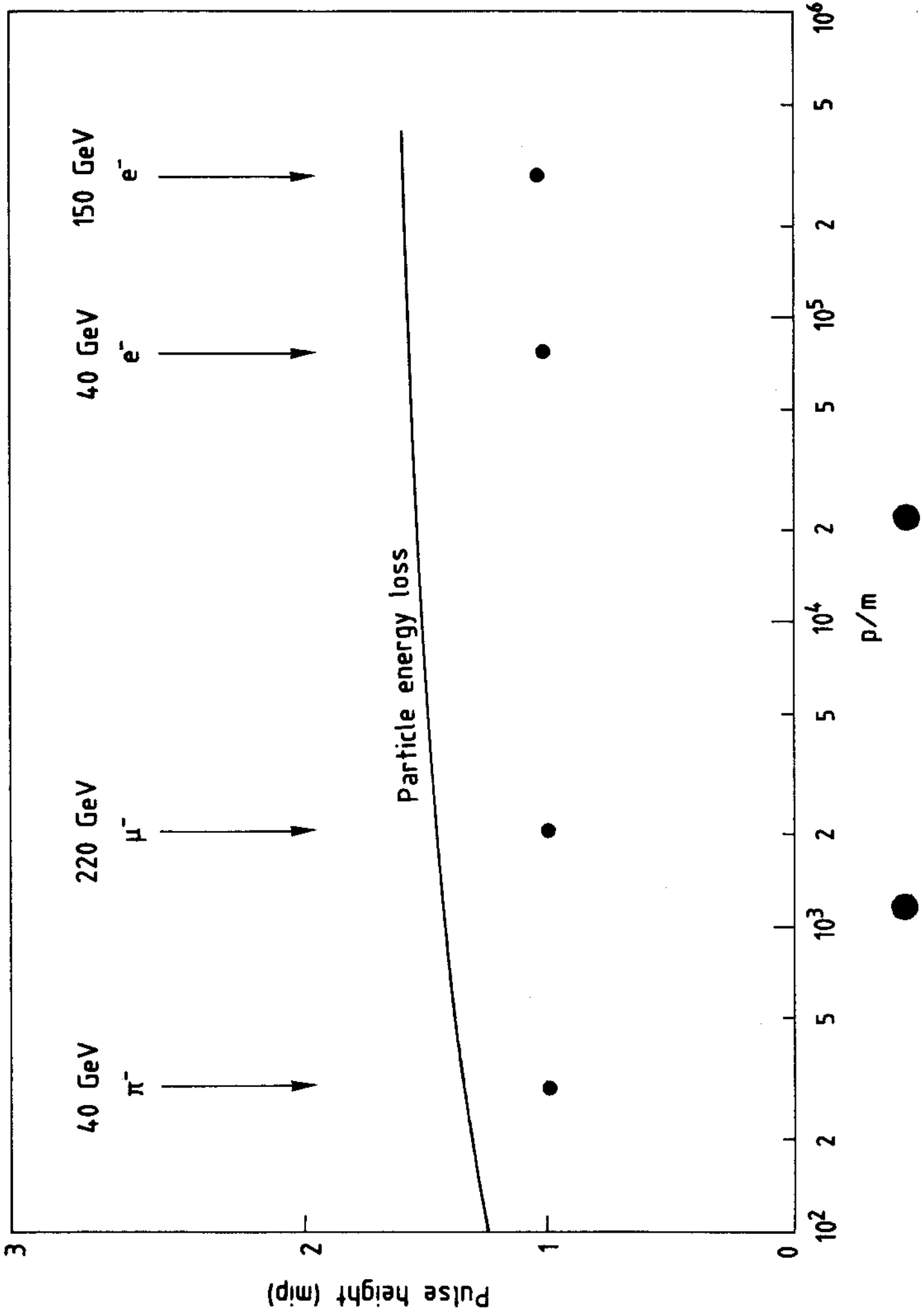

Pulse height (mip)
3
2
1
0
10^2
2
5
10^3
2
5
10^4
2
5
10^5
2
5
10^6
p/m
Particle energy loss
40 GeV
π^-
220 GeV
μ^-
40 GeV
e^-
150 GeV
e^-

Figure 8

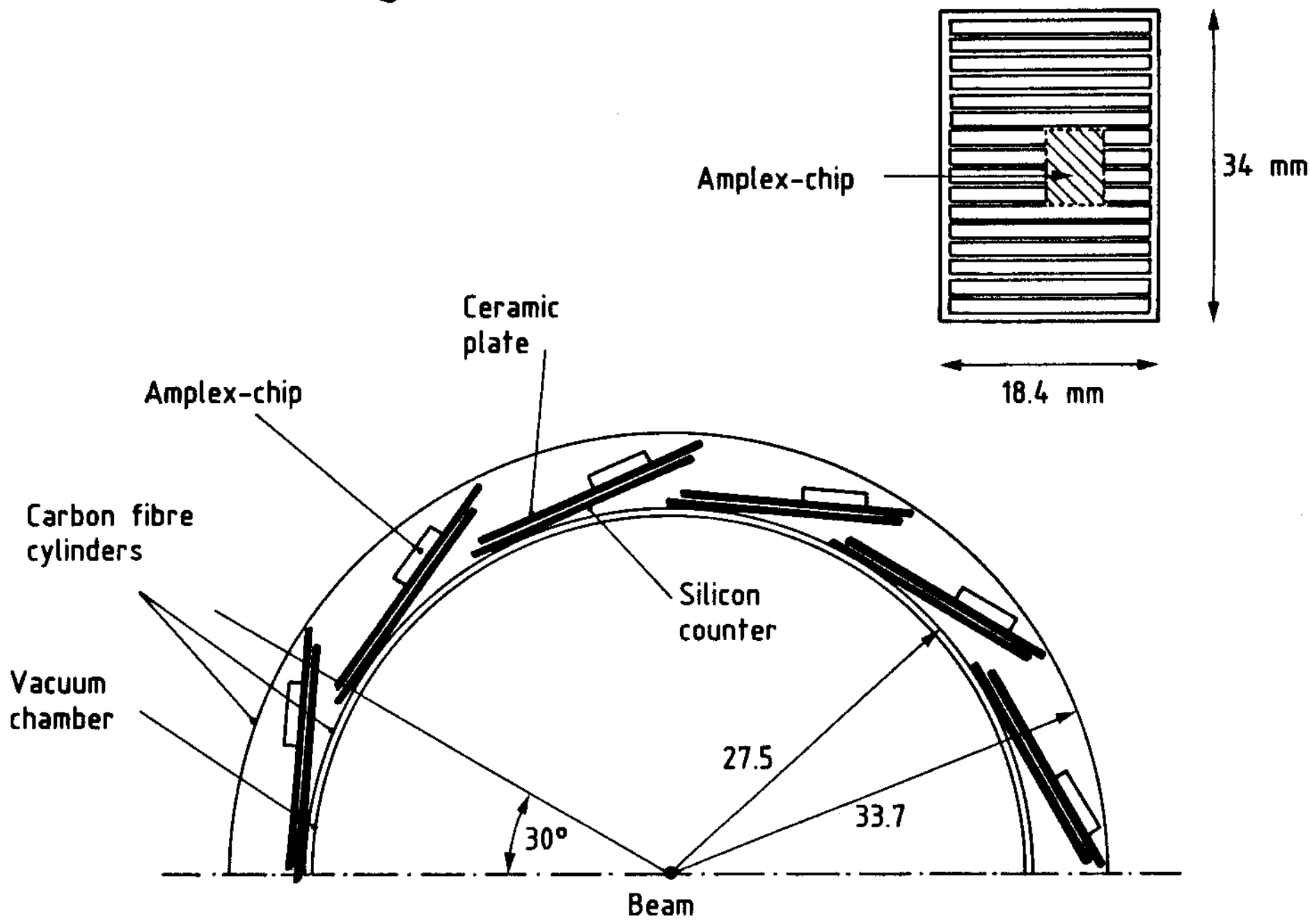

Amplex-chip
34 mm
18.4 mm
Ceramic plate
Amplex-chip
Carbon fibre cylinders
Silicon counter
Vacuum chamber
27.5
33.7
30°
Beam

Figure 9

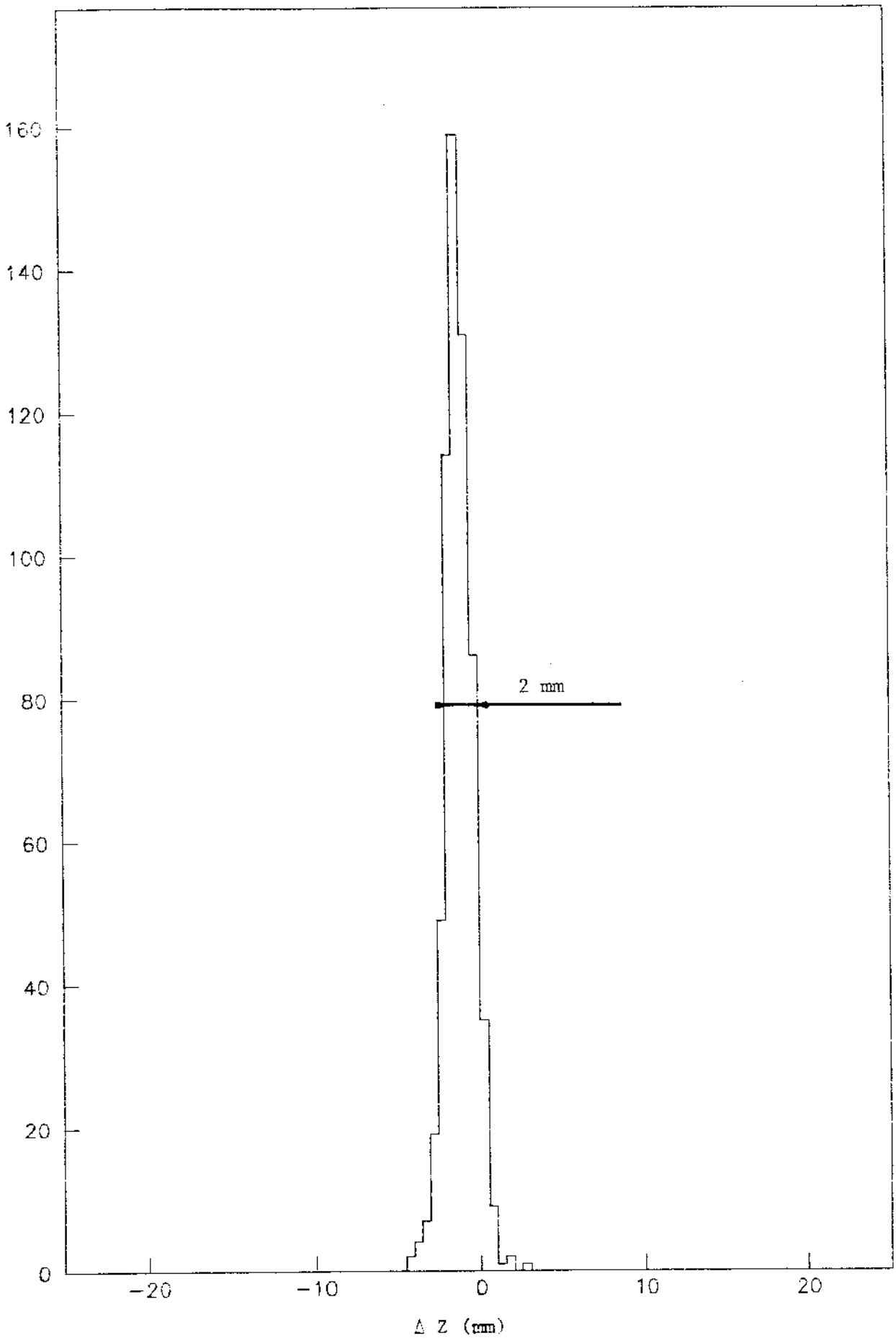


Figure 10

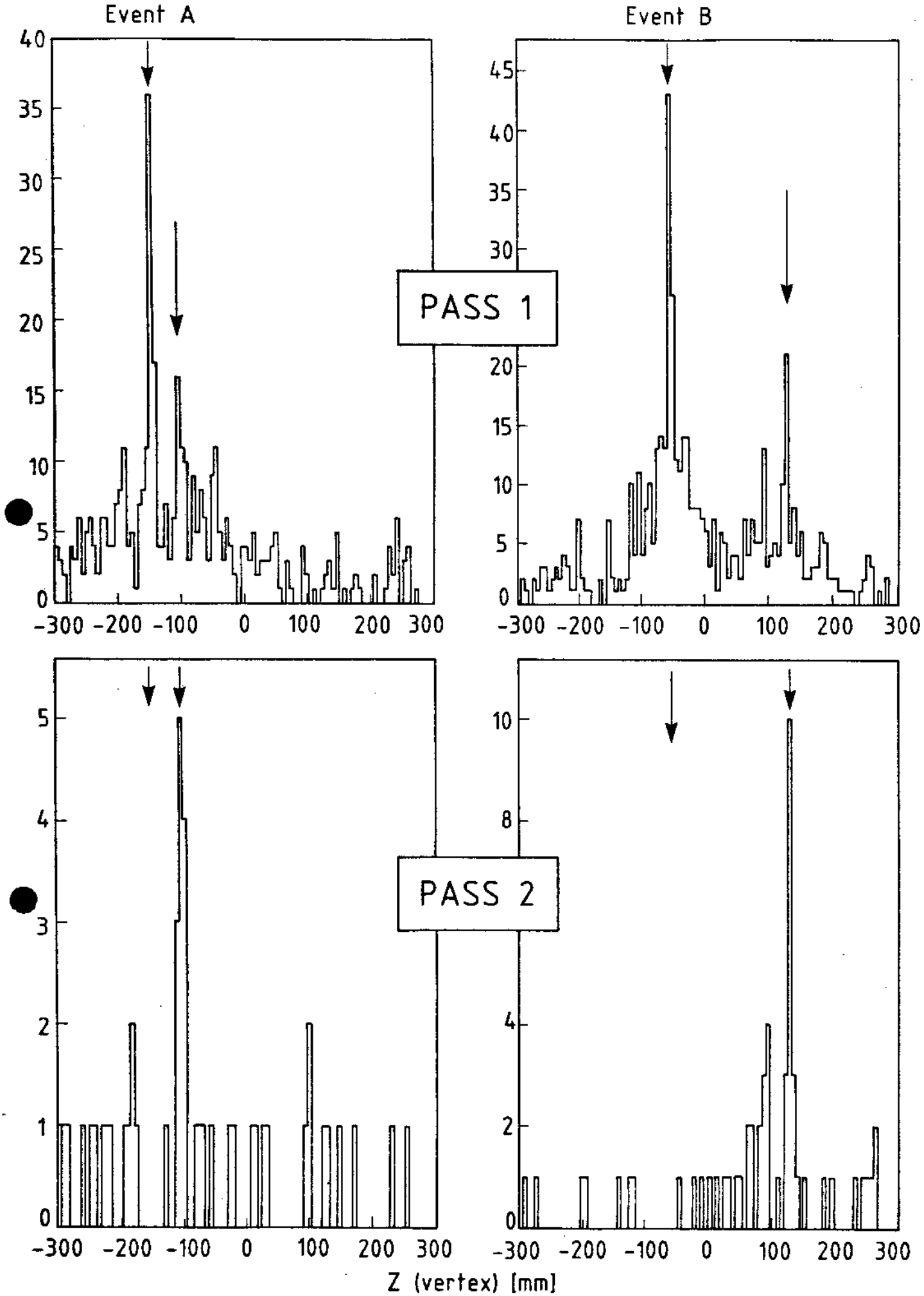


Figure 11

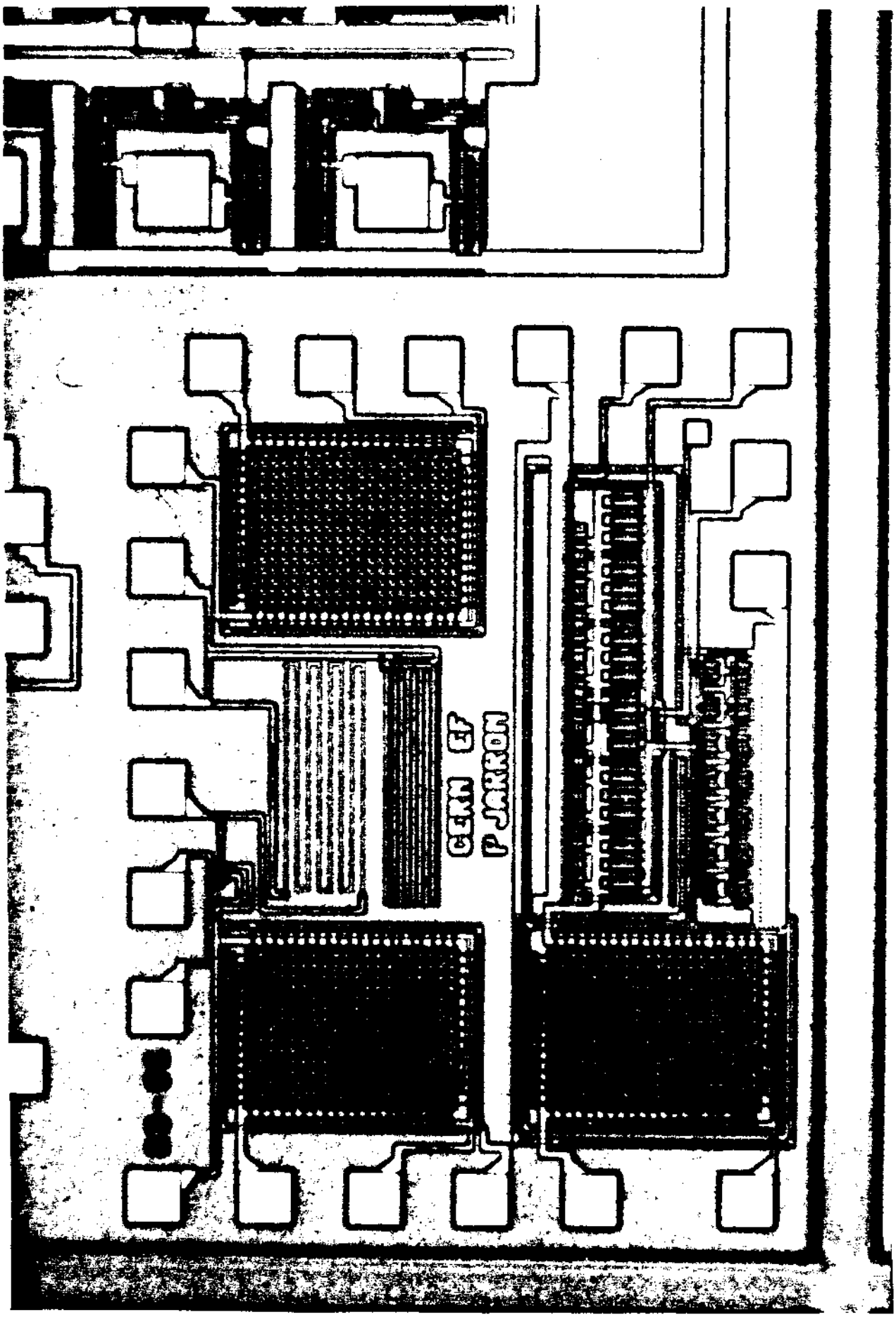


Figure 12a

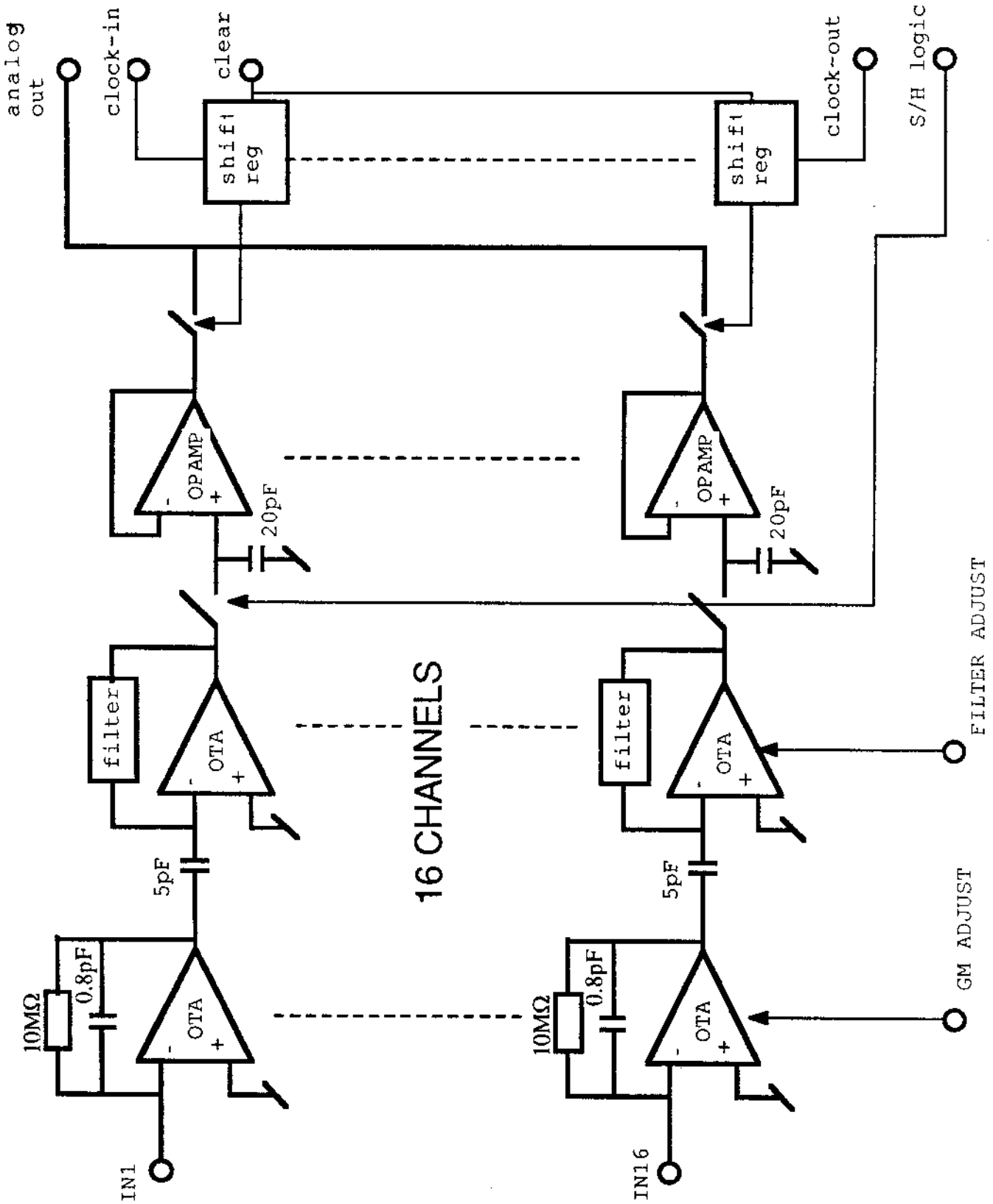

analog out
clock-in
clear
shift reg
clock-out
S/H logic
OPAMP
20pF
filter
OTA
5pF
10MΩ
0.8pF
16 CHANNELS
FILTER ADJUST
GM ADJUST
IN1
IN16

Figure 12b