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Data-acquisition system for a target multifragmentation experiment with large solidangle detectors

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Abstract

We have developed a CAMAC data-acquisition system that is capable of handling not only high-rate interrupting, but also over one hundred inputs within a single CAMAC crate in order to perform exclusive measurements of target multifragmentation induced by 8 and 12-GeV primary proton beams on heavy nuclei. The system is running under PC-Linux and a CAMAC auxiliary crate controller. Since we have selected the UNIDAQ data-acquisition system for our DAQ software, which is only using standard UNIX technology, we are expecting easy migration to another platform in a future system upgrade.

1 Introduction

An exclusive measurement of target multifragmentation in high-energy light-particle and nucleus collisions has been performed using a Bragg-Curve Counter (BCC) system covered with almost 20% of the entire solid angle [1] at the 12-GeV Proton Synchrotron of the High Energy Accelerator Research Organization (the KEK-PS). The current BCC system is an upgrade version of that [2] used for previous small-scale experiments [3], which consisted of 5 channels of BCCs. The new system has been increased to 37 channels of BCCs, which has required the development of a new data-acquisition

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system, because we expect more than ~ 10-times as large event rate and data size. The maximum trigger rate is estimated to be 5 kHz randomly, and the size of the data could reach 46 bytes per event. Therefore, the data-acquisition system should have both a data-acquisition speed of 230 kbyte/s and a fast response for very high-rate triggers. Until recently, the DAQ system using the CES 2180 CAMAC ACC (J11) has satisfied such kinds of demands. The termination of the production of the J11 module, however, forced us to develop a new CAMAC data-acquisition system.

Challenging aspects of the new data-acquisition system are as follows:

- Over a 200 kbyte/s data-acquisition speed for a single CAMAC crate controller and a 1 Mbyte/s block-transfer speed to the host computer for multi-crate experiments and for minimizing the dead time at synchrotron experiments where data can be transferred for a spill-off interval.
- No significant dead time for continuous beam experiments.
- Use standard technique enabling the porting of various platforms.
- Supporting distributed data-acquisition system with a computer network.
- Low-cost system for the required hardware and software.

As a result, we have decided to use a Kinetics Model 3927 Auxiliary Crate Controller (ACC) and Personal Computer (PC) system running under the Linux OS. For data-acquisition software we have ported the UNIDAQ system [4, 5, 6] which was originally developed for the Solenoidal Detector Collaboration (SDC) test data-acquisition system at the Superconducting Super cccollider (the SSC). The UNIDAQ system has already been ported to many platforms [7, 8, 9] and drivers have been developed for various interface cards [10]. The performances of the CAMAC data-acquisition system under Linux have been measured [11] and its fast speed performance on a standard PC system has been reported. The performances of the ACC system have also been measured [10], showing that it is suitable for target multifragmentation experiments.

In this paper, we report on an application of both the ACC and PC-Linux system with the UNIDAQ to the data-acquisition system. We will discuss the performance of the system in our experiment. The hardware implementation is presented in Section 2, where we also introduce a new clock-based time-to-digital converter (TDC) module especially developed for our experiment. In Section 3, we describe the software design, development environment, and the data and command flow. The performance achieved with this system is presented in Section 4, followed by a summary and a acknowledgement in Section 5.

2 Hardware implementation

In the experiment we are using 37 BCCs operated with P-10 gas of about ~200 Torr and an electric field of approximately ~30 V/cm[2]. Since the maximum drift length of each BCC is ~30 cm, the drift time of electrons in the field would be up to ~5 μs.

2.1 Front-end electronics

A block diagram of the front-end electronics is shown in Fig.1. The anode signal of each BCC is amplified in a charge-sensitive preamplifier and split into two main amplifiers with different shaping time constants. A signal shaped with 0.1μs reproduces the Bragg-Curve, *i.e.* the energy deposition of a particle through its trajectory in the BCC (See Fig.2). The peak of the signal gives atomic-number (Z) information about the incident particle. To adjust the timing of the peak position, the Bragg-Curve signal is delayed before being fed into the peak-sensitive ADC. Energy information about an incoming particle is obtained from the pulse height of a signal shaped with 6μs. The shaping time of 6μs almost corresponds to the maximum drift time of the electrons, *i.e.* the maximum width of the Bragg-Curve in this experiment[2]. This signal is directly fed into the peak-sensitive ADC.

The Bragg-Curve signal is also fed into a pulse-width analyzer with a 20mV threshold (Low Vth) and a discriminator with a 100mV threshold (High Vth). The pulse width analyzer generates a pair of timing pulses at the leading and trailing edges of the Bragg-Curve signal (See Fig.2). The time difference between these pulses gives range information about the particle. The pulse generated from the High Vth discriminator is used as a trigger signal and for the input to a coincidence register in order to recognize any coincidence event. The high threshold discriminator is used to select $Z \geq 3$ particles in order to reduce the trigger rate by rejection of the main trigger component from alpha particles and protons.

An "OR" of all trigger signals is used for the main trigger by selecting of the fastest trigger using a flip-flop and a AND logic. Once the main trigger is generated, it is inhibited until all data are collected by the computer. After the end of the cycle of data collection, the flip-flop is cleared by a reset signal. Gate signals for the coincidence register and ADC are formed from the main trigger signals. A gate generator after the OR gate is placed to eliminate successive pulse generation before trigger inhibition.

2.2 Read-out system

Two CAMAC crates are used for the experiment (See Fig. 3). All of the ADCs

and TDCs are placed in the main crate where an ACC reads out data from them. The ACC has 1 Mbytes of main memory used for data buffer and program area. An interrupt register is used for interrupting to the ACC when a main event trigger, a calibration pulser-event trigger, or a beam spill-end timing trigger is detected. The calibration pulser-event trigger is formed by additional front-end electronics to that explained in the previous section. A beam spill-end timing trigger is provided from the accelerator. A coincidence register is used for selecting triggered BCC channels within a 20μs coincidence gate window. Three modules of 12-bit successive approximation-type ADCs (SA-ADC) with 16-channel inputs and eight modules of the 12-bit Wilkinson-type ADCs (W-ADC) with 4-channel inputs are used for converting the energy and Z analog signals to digital ones, respectively. We need high linearity for the Z signals to separate the nuclear spices. The SA-ADC converts the signal within 5μs for one channel; hence, it takes 80μs plus overhead time for all channels to be converted. On the other hand, the W-ADC needs 20μs for converting one signal at the maximum pulse height; hence, it takes almost the same conversion time both for the SA-ADC and the W-ADC.

We used the main trigger signal for the start signal of the TDCs, and used the leading or trailing signal created by the pulse width analyzer as the stop signal (See Fig.2). Since we need to measure the time up to 7μs for the trailing signal, we were forced to develop a custom-made clock-based TDC. The detail concerning the TDC will be explained in the following section. An output register generates a reset signal to the coincidence register, the TDC, and the flip-flop when the ACC has finished one acquisition cycle. A crate controller (Kinetics Model 3922) in the main crate communicates with the data-acquisition system on the PC via a K-Bus cable and a PCI interface card (Kinetics Model 2915). The crate controller is also connected to the second crate controller. In the second crate many scalers are inserted to acquire beam information, event information, and trigger information. These scalers are read out directly by a PC during a spill-off interval.

Several personal computers are used for the experiment. One is dedicated to data collection (Collector PC), and the other is used for on-line monitoring and storing the data (Monitor PC). Each PC is connected to Ethernet. Collected data on the Collector PC are transferred to the Monitor PC via the network. The Monitor PCs have an 8mm tape drive or CDR drives for mass storage.

2.3 Clock-Based TDC

The 100 MHz CAMAC clock-based TDC module with 16-channel fast NIM level

inputs has been developed using 5 programmable logic devices[12]. Four devices are configured as 4 channels of counter chips, and the other one is configured as a controller chip of the counters, input signals and CAMAC interface. The maximum speed of the TDC is estimated to be 113 MHz based on a simulation using the development tool provided by ALTERA (MAX+plusII) [13].

The TDC has a 100 MHz internal clock generated by a crystal oscillator that allows the interval time of start and stop signals to be measured to 10ns precision; it also has a NIM external clock input for feeding the variable clock. The source of the clock can be changed by a toggle switch on the front panel. All of the functions of this TDC follow the standard CAMAC convention.

The root-mean-square (RMS) values of the measured time resolution were 0.31 Least Significant Bit (LSB) or 0.48 LSB at a 40 MHz external clock or a 100 MHz internal clock, respectively. The RMS values were slightly larger than expected quantization error ($1/\sqrt{12}$ LSB), because of time jitter (~3ns) due to electric noise inside and/or outside the TDC in our measurement system. However, the measurement has proved that the TDC works within $\pm 1/2$ LSB resolution with both a 40 MHz external clock and a 100 MHz internal clock. Finally, more than 10 CAMAC modules of this clock-based TDC were manufactured by us and successfully used for the experiments. Fortunately, no serious problem was found in those modules until now.

3 Software

A block diagram of the data-acquisition system using the UNIDAQ and the ACC is shown in Fig. 4. The UNIDAQ consists of Collector, NOVA, Recorder, NetNOVA, and Scaler processes running on the Collector PC, while an Analyzer process of the UNIDAQ is running on the Monitor PC. The Kinetics Model 3917 ACC is a standalone computer controlled by a Motorola 68EC030 40MHz processor with a 1 Mbyte dual-port memory. The memory of ACC can be accessed from both the CAMAC crate controller and the ACC processor. The control program for the ACC is down-loaded to the ACC memory from the Collector PC.

3.1 Data and control flow

The ACC starts to poll data from the ADC and TDC modules when the interrupt register generates a LAM signal. Collected data are stored in ACC buffers and sent to shared memory on the Collector PC (See Fig.4), which is managed by the NOVA process. The NOVA process passes a pointer to the Recorder and NetNOVA processes

as a message with Inter Process Communication (IPC), so that they can transfer the data to each destination. The Recorder process saves collected data to a hard disk, while the NetNOVA process transfers a part of the data to the Monitor PC via the Ethernet. We are monitoring the real-time data with PAW (Physics Analysis Workstation), developed at CERN on another computer, in order not to load the Collector PC and to have the capability to flexibly change the monitor program. The Scaler process displays the information concerning signal counts for each channel from the scaler modules.

The Collector process communicates with the ACC control program using the ACC Communication Area of the dual-port memory (See Fig.5). Data semaphore is used for access control of the ACC buffers. The ACC control program can retrieve the buffer when data semaphore is available, and returns the semaphore when the buffer is full or the spill-off trigger is received. On the other hand, the Collector process needs a semaphore during data-transferring, and returns it at completion of the transfer. The ACC program returns a DAQ status, *i.e.* SPILL OFF, DATA FULL or TIME OUT, and an ACC status, *i.e.* ACC RESUME, ACC PAUSE, ACC END, ACC WAIT, while the Collector process is polling them. On the contrary, the Collector process issues a command to the communication area, while the ACC program is always polling it at the end of each data-acquisition cycle.

3.2 Structure of the ACC control and collector programs

We mapped the ACC memory as a communication area, a buffer area, a program area and a stack area, as shown in Fig.5. The executable binary code is transferred to the program area by a down-load program called in the initialization routine (begin) of the Collector process.

After down-loading, the start command of data acquisition (resume) is dispatched to the ACC, where start of the ACC application is issued and communication between UNIDAQ and ACC is established. Once the start command is accepted, the ACC program gets a buffer and waits for the LAM of the interrupt register at the beginning of the DAQ routine.

The DAQ routine is a list of CAMAC single actions. Since the DAQ routine is written in C language, it is possible to describe it in various ways. We found that not using "for" and "while", but writing a plane iterated function call makes the ACC speed much faster. This is because the ACC is using normal dynamic memory as the dual-port memory, then frequent memory-access by the program itself makes the speed desperately slow. Frequently used variables should also be declared as being registered

variables.

In the case of the ACC buffer being full, the spill-off interrupt, or the timeout of waiting for the LAM signal from the TDCs and ADCs, the ACC program interrupts the Collector process by generating a LAM request. After the Collector checks the ACC status, the DAQ status, and the DATA semaphore, it reads corresponding data into the shared memory of the Collector PC with a block-transfer function.

If no semaphore is available, the ACC waits for its return. In the case of excessive data handling by the ACC, more than by the Collector, the ACC program always waits for the semaphores. We must then tune the trigger rate to reduce the dead time.

When we want to pause the data acquisition and to restart again, we issue a "pause" command, which keeps all of the acquired data, scaler information, event log, and run number. They are continuously updated upon restarting. When we stop data acquisition, we issue a "stop" command that stores the all of the acquired data and the information as data and log files on the hard disk.

3.3 Software development environment

All of the ACC programs can be developed using GNU gcc cross compiler and the ld linker as the 68030 target. A C-source code is compiled to relocatable the object code with this cross compiler, and it is linked with a CAMAC library (ACC CAMLIB) [14]. The ACC CAMLIB has been developed for the ACC to be compatible with the CAMLIB developed at KEK [15]. The start addresses of executable code and data segment can be changed with options of ld. On the other hand, the UNIDAQ collector program has been developed with the CAMLIB and a ACC-UNIDAQ LIB using the gcc compiler as a Linux target. The ACC-UNIDAQ LIB [14] is a function library, which has also been developed in this project, designed for a communication program between the ACC control program and the Collector process.

4 Performance

The data-acquisition performances with the ACC and/or the PC-Linux system has already been reported elsewhere [10, 11]. We only report on the performance of its application for a multifragmentation experiment.

A timing chart of the data acquisition cycle is shown in Fig.6. The main trigger is delayed for 45μs because of waiting for the completion of A-D conversion. The ACC is interrupted by the main trigger and woken up within 25μs. After that, the ACC reads the coincidence register first, and then starts to read the TDCs and the ADCs

corresponding to the hit information from the coincidence register. The total time of data acquisition is 195μs when the multiplicity of the event is one. If the multiplicity is greater than one, processing each additional multiplicity requires an extra 50 μs.

The transfer speed from the ACC memory to the PC-Linux shared memory is 1 Mbyte/s when using the 2915 PCI interface card. The dead time is less than 1 μs during a transfer and it takes about 40 μs to switch the ACC buffer.

Since the maximum acceptable trigger rate is expected to be around 5 kHz with a repeated trigger, as shown in Fig.6, the actual rate in the experiment should, of course, be lower. The accepted trigger efficiency under the typical condition, *i.e.* a multiplicity of one to two, was about 65% at a 3 kHz trigger rate. The accepted trigger efficiency is interpreted as being the probability of no other trigger within 195μs. We estimate that the efficiency is about 55% with this interpretation assuming a Poisson distribution. Since the experiment was performed with pulsed beams, the efficiency should be better than our estimation.

The A-D conversion is the most critical timing constraint for our DAQ system because we took redundant time for the A-D conversion so as to maintain the reliability of data in the experiment. If we use much faster ADC modules, we can expect to reduce the DAQ cycle to 150μs.

5 Summary and Acknowledgement

The present system is one approach to construct a low-cost and fast data-acquisition system within the framework of the traditional CAMAC measurement environment. Developed software keeps the compatibility of the UNIDAQ system and the CAMLIB library under the development environment with GNU free software. Furthermore, since the UNIDAQ has already been ported to various platforms, the current system should be easy to migrate to another platform.

In an experiment, data were recorded at a typical rate of 3 kHz, *i.e.* 78 kbyte/s data acquisition speed on the average. 65% of the triggers were accepted in typical runs.

We would like to thank Professor H. Fujii and Mr. Y. Yasu for their valuable suggestions and discussions. This work was partly supported by KEK R&D project in 1996. This work was also performed as part of a Grant under the Monbusho International Scientific Research program (No.09041113).

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Figure caption

Figure 1: Block diagram of the front-end electronics for the BCC system; 37 channels of Analog Signals are inputted to each preamplifier.

Figure 2: Schematic illustration of a Bragg-Curve signal. High Vth is a threshold at the generating trigger signal; Low Vth is a threshold at generating pulses for measuring the range.

Figure 3: Schematic of the data-acquisition system. Two CAMAC crates are used for the experiment. Personal computers are running under Linux and connected to the Ethernet.

Figure 4: Block diagram of the data-acquisition system. The arrows indicate the data and control flow of the system.

Figure 5: Flowchart of the application program for a multifragmentation experiment.

Figure 6: Performance of the ACC and UNIDAQ system in an exclusive multifragmentation measurement.

Fig. 1

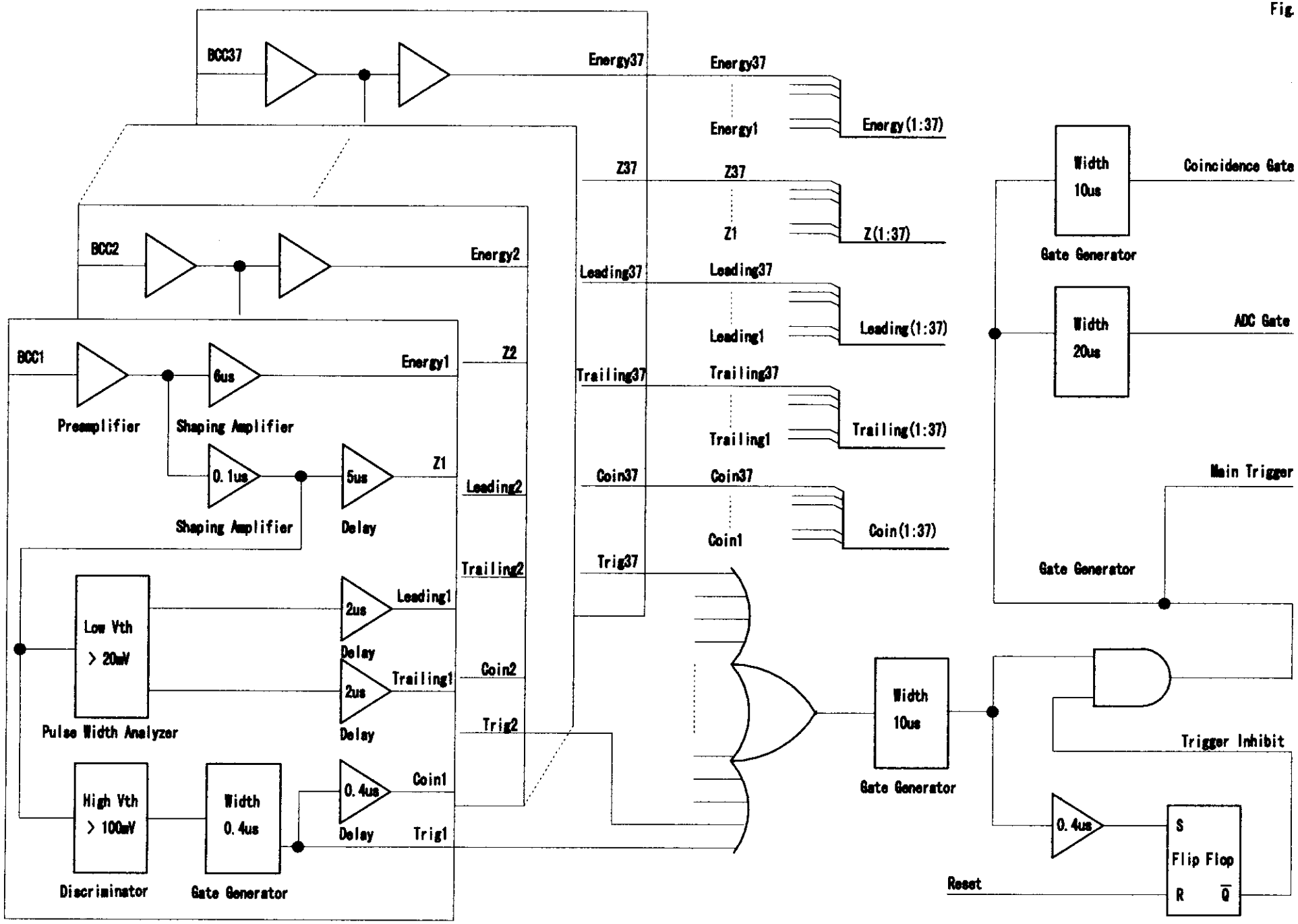

BCC37
Energy37
Energy37
Energy1
Energy(1:37)
Z37
Z37
Z1
Z(1:37)
BCC2
Energy2
Leading37
Leading37
Leading1
Leading(1:37)
BCC1
Energy1
Z2
6us
Preamplifier
Shaping Amplifier
Trailing37
Trailing37
Trailing1
Trailing(1:37)
0.1us
5us
Z1
Leading2
Coin37
Coin37
Coin1
Coin(1:37)
Shaping Amplifier
Delay
Trailing2
Trig37
Low Vth
> 20mV
2us
Leading1
Delay
2us
Trailing1
Coin2
Pulse Width Analyzer
Delay
Trig2
High Vth
> 100mV
Width
0.4us
0.4us
Coin1
Delay
Trig1
Discriminator
Gate Generator
Width
10us
Gate Generator
Width
10us
Coincidence Gate
Gate Generator
Width
20us
ADC Gate
Main Trigger
Gate Generator
Trigger Inhibit
0.4us
S
Flip Flop
R
Q
Reset

Fig. 2

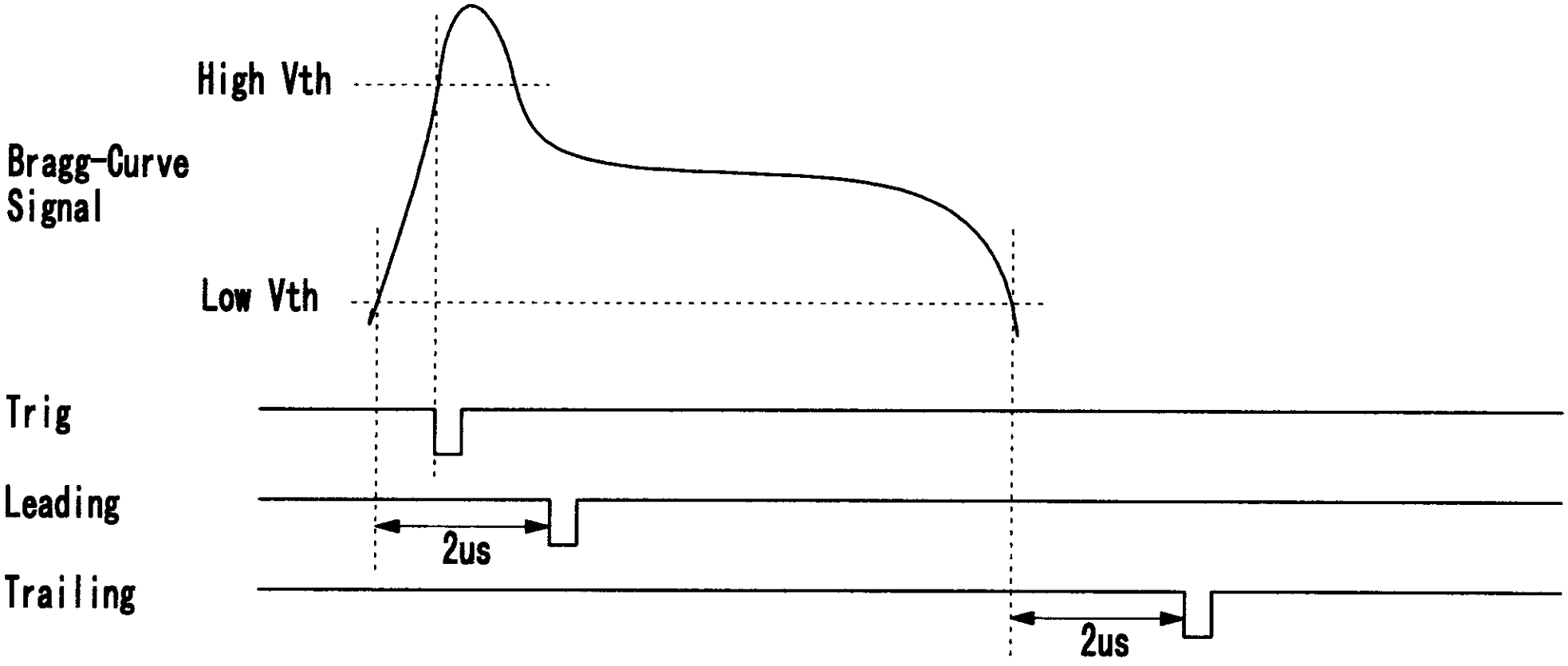

High Vth
Bragg-Curve Signal
Low Vth
Trig
Leading
2us
Trailing
2us

Fig. 3

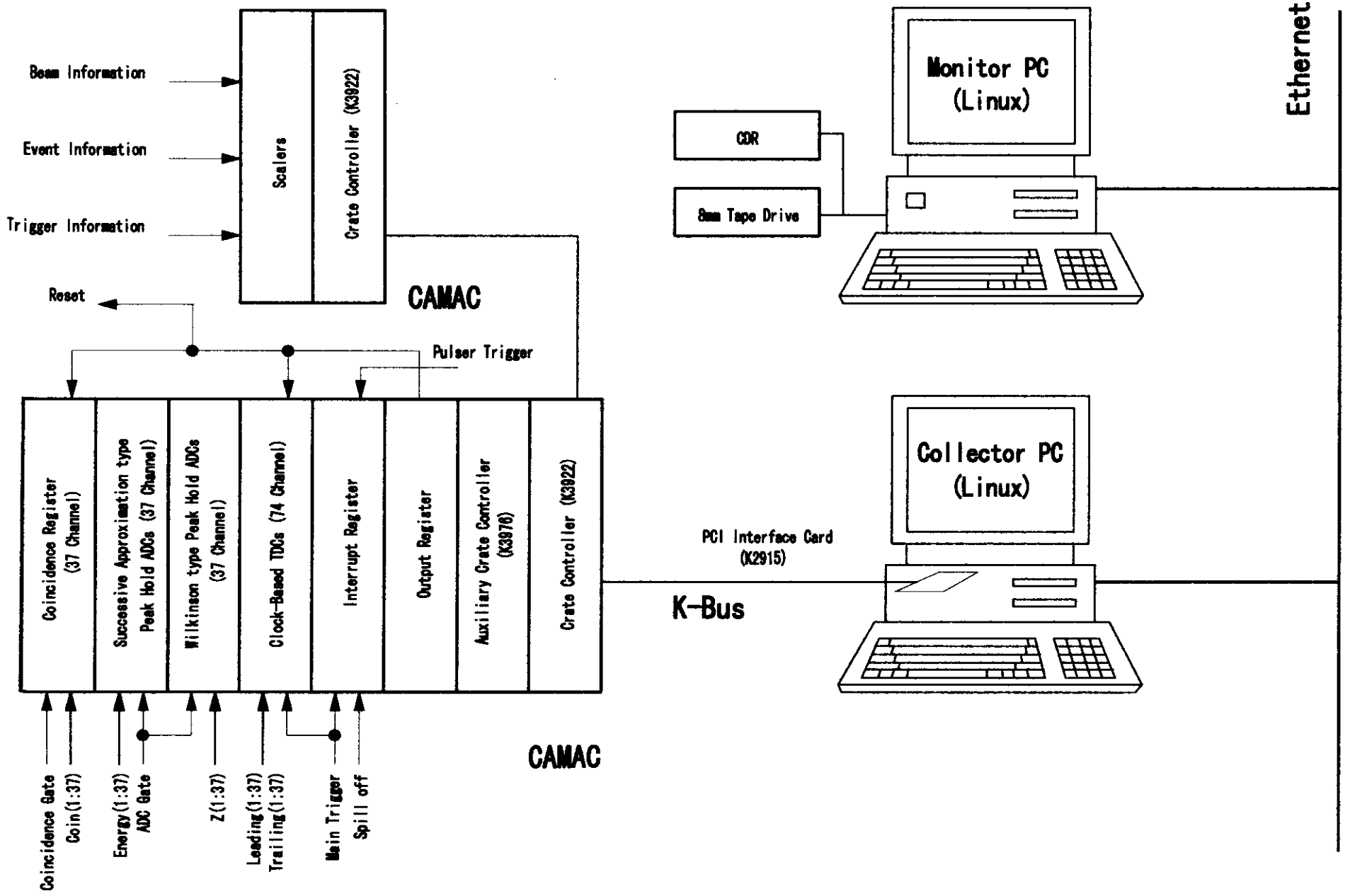

Beam Information
Event Information
Trigger Information
Scalers
Crate Controller (K3922)
CAMAC
Reset
Pulser Trigger
Coincidence Register (37 Channel)
Successive Approximation type Peak Hold ADCs (37 Channel)
Wilkinson type Peak Hold ADCs (37 Channel)
Clock-Based TDCs (74 Channel)
Interrupt Register
Output Register
Auxiliary Crate Controller (K3976)
Crate Controller (K3922)
CAMAC
Coincidence Gate
Coin(1:37)
Energy(1:37)
ADC Gate
Z(1:37)
Leading(1:37)
Trailing(1:37)
Main Trigger
Spill off
CDR
8mm Tape Drive
Monitor PC (Linux)
Ethernet
PCI Interface Card (K2915)
K-Bus
Collector PC (Linux)

Fig. 4

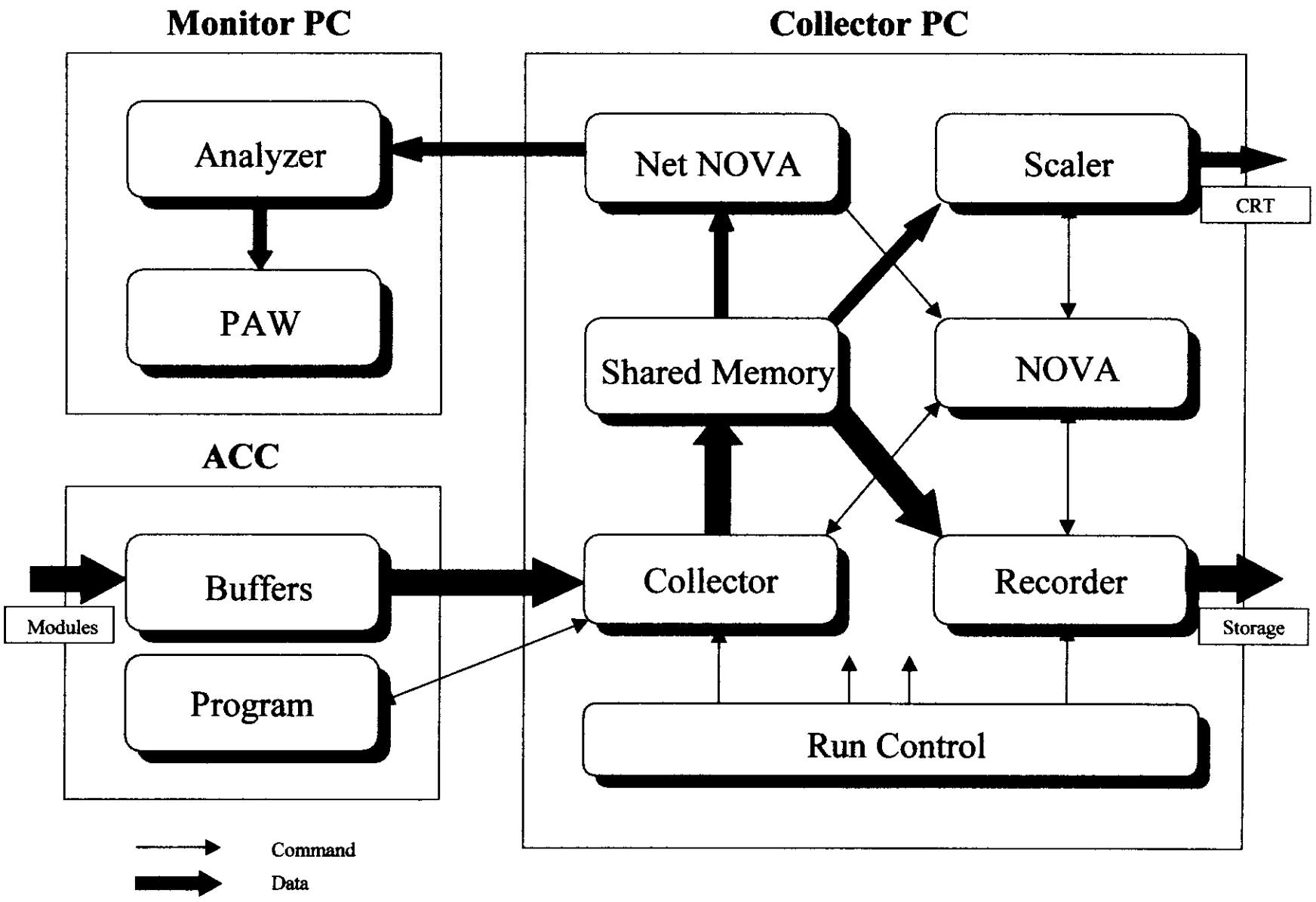

Monitor PC
Collector PC
Analyzer
PAW
Net NOVA
Scaler
CRT
Shared Memory
NOVA
ACC
Buffers
Modules
Collector
Recorder
Storage
Program
Run Control
Command
Data

Fig. 5

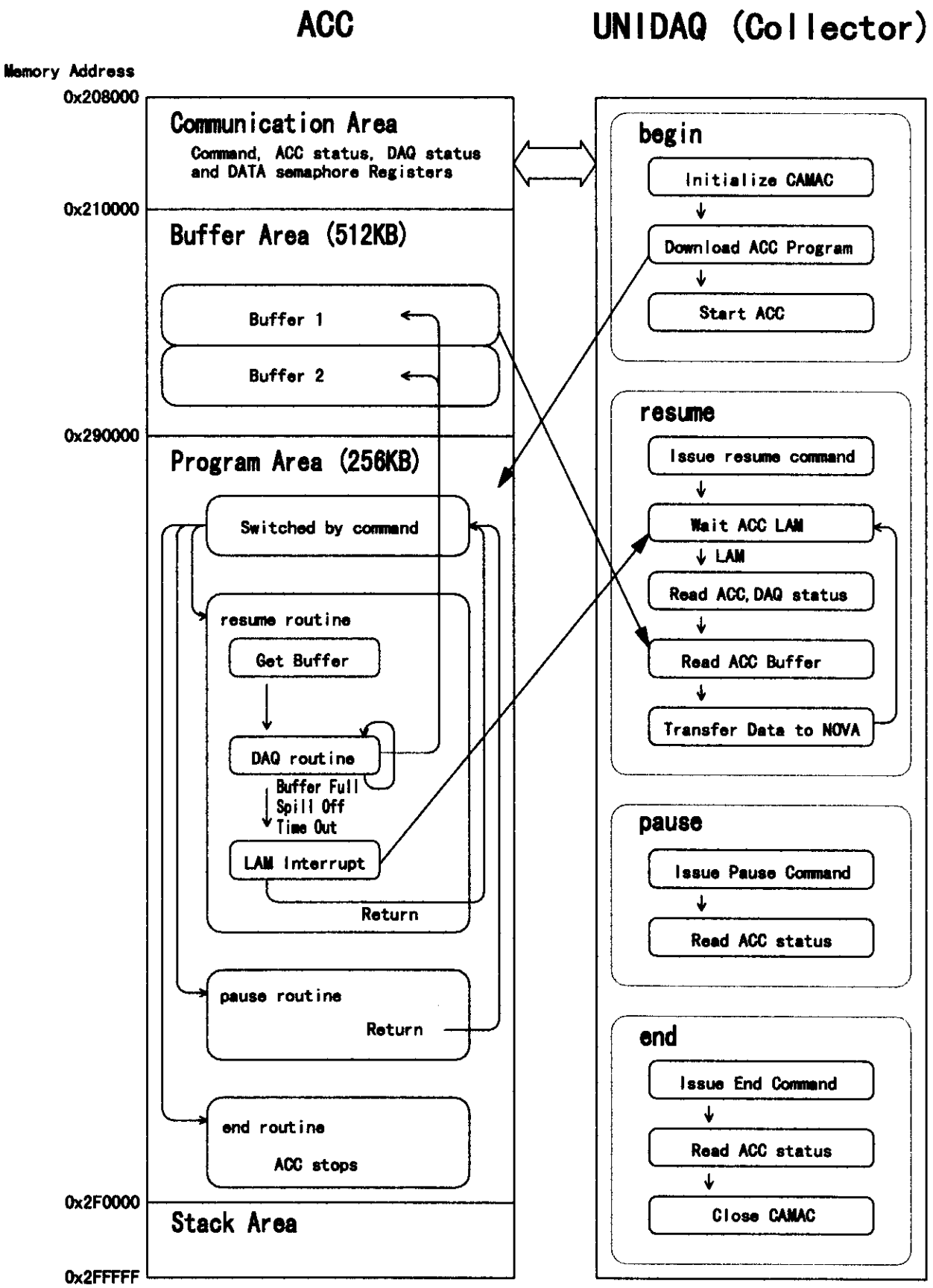
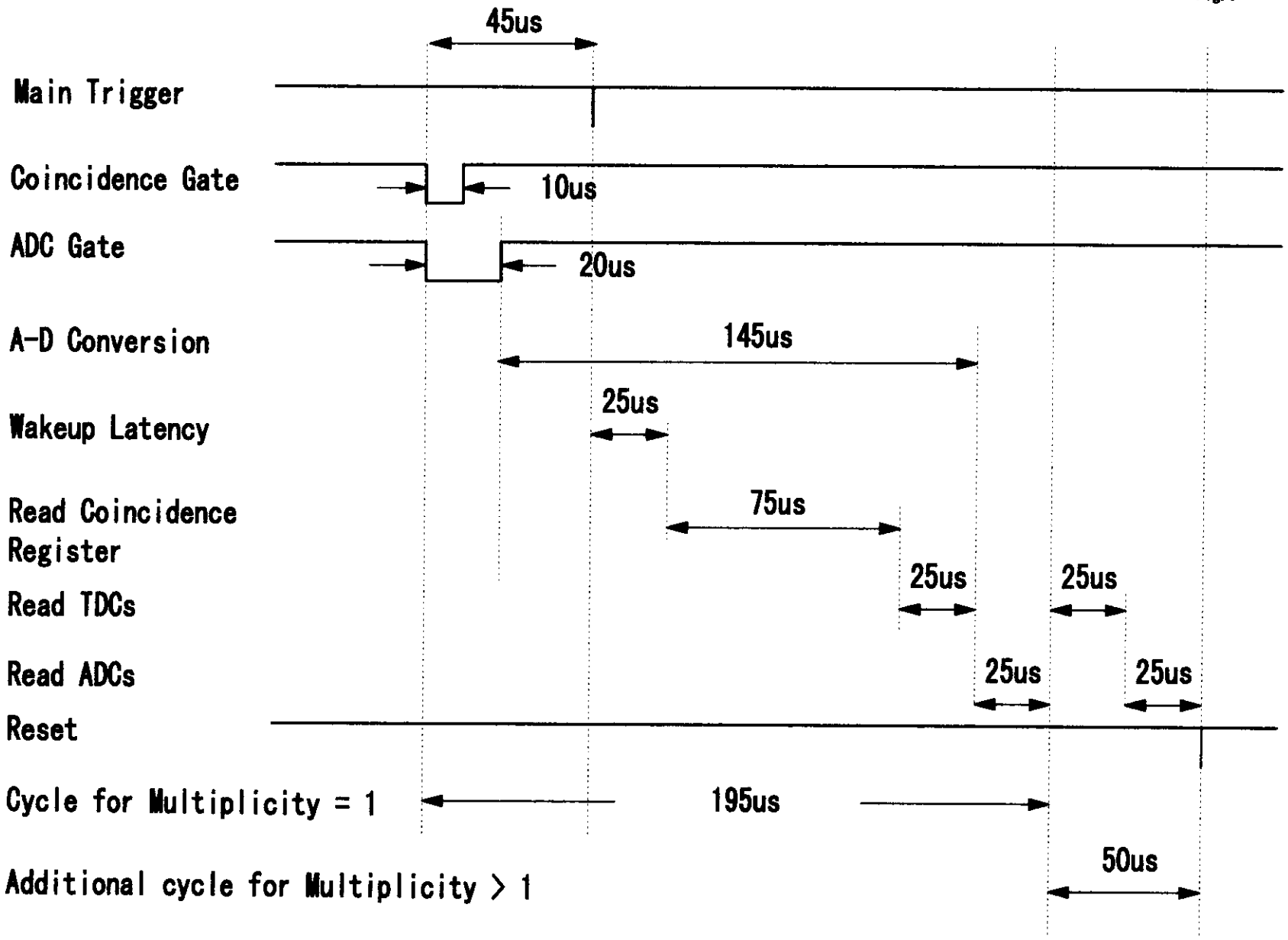

ACC
UNIDAQ (Collector)
Memory Address
0x208000
Communication Area
Command, ACC status, DAQ status and DATA semaphore Registers
0x210000
Buffer Area (512KB)
Buffer 1
Buffer 2
0x290000
Program Area (256KB)
Switched by command
resume routine
Get Buffer
DAQ routine
Buffer Full
Spill Off
Time Out
LAM Interrupt
Return
pause routine
Return
end routine
ACC stops
0x2F0000
Stack Area
0x2FFFFF
begin
Initialize CAMAC
Download ACC Program
Start ACC
resume
Issue resume command
Wait ACC LAM
LAM
Read ACC, DAQ status
Read ACC Buffer
Transfer Data to NOVA
pause
Issue Pause Command
Read ACC status
end
Issue End Command
Read ACC status
Close CAMAC

Fig. 6


45us
Main Trigger
Coincidence Gate
10us
ADC Gate
20us
A-D Conversion
145us
25us
Wakeup Latency
Read Coincidence Register
75us
25us
25us
Read TDCs
Read ADCs
25us
25us
Reset
Cycle for Multiplicity = 1
195us
50us
Additional cycle for Multiplicity > 1