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DEVICE FOR READING OUT INFORMATION FROM THE FERRITE MATRICES OF WIRE SPARK CHAMBERS

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INTRODUCTION

Wire spark chambers in which the information is recorded on ferrite cores are widely used in physics experiments. The number of wires in spark chamber systems is continually increasing and now often reaches several tens of thousands. At the same time, more and more is being required of the devices which read out the information from the ferrite matrices and transfer it to the computer, as all the information must be read in a period not exceeding the chambers' dead time (i.e. several milliseconds) and the devices must remain relatively simple. A series of systems has been developed for reading out information from ferrite matrices (1-5) but they are continually being improved.

This paper describes a device developed at the JINR Laboratory for Nuclear Problems. It can read information from spark chamber systems including up to 32,000 wires. The device codes the information and transmits it to a buffer store consisting of one of the AI-4096 analyzers in the Laboratory's data storage and processing centre (6). The centre has a two-way link with a Minsk-22 computer.

Various circuit solutions described in reports (2-5) were used for the development of the device. It is made from standard BESM-4 computer modules. There are 270 modules altogether. The development work is now in its final stages, and a similar functional diagram is being used but with integrated circuits based on diode-transistor logic.

Functional diagram

A functional diagram of the device is shown in fig.1. The number of ferrite cores in the matrices may total up to 32 768. Each matrix will contain 256 or 512 cores depending on the size of the chamber to which it is connected (0.25 or 0.5 metre). Ferrite matrices are placed at both of the chamber's electrodes.

The information is read by a total current from successive groups of 32 cores. A group is selected by a two-co-ordinate system of registers II and III, which are five-bit counters. Register II and its de-coder are used to select one of the 32 current shapers, whilst register III and its de-coder are used to select one of the 32 current gates through which the current from the shaper will pass. Pulses generated when the cores are set pass through the amplifiers and switch to state "1" corresponding flip-flops in register 1, which has 32 bits.

The read-out device is put into operation by a trigger pulse which coincides with the transmission of the high voltage to the spark chambers. In order to eliminate the effect of interference caused when sparks are produced in the chambers, the trigger pulse is transmitted by a one-shot OS-1. The latter sends a ~ 30 /usec pulse to all the flip-flops in the device. The pulse is transmitted directly to registers II, III and to flip-flops $T_{beg.\ coll.}$ and $T_{end.\ coll.}$, and via circuit OR-6 to register I and control flip-flop $T_{cont.}$. All the device's flip-flops are kept in state "0" by the one-shot's pulse.

A pulse corresponding to the decay time of the one-shot's pulse is transmitted via circuit OR-1 and delay lines DL-1 and DL-2 to the 32 bit gating circuit which controls the triggering of the current shapers. As registers II and III are initially in state "0", the first group of ferrite cores will be strobed. If any cores in this group are in state "1", then pulses will be generated in their signal windings. These pulses will then be amplified and will switch the corresponding flip-flops in register 1 to state "1".

The pulse from delay line DL-2 is also transmitted to the OR-3 circuit and then through delay line DL-3, and it switches the flip-flop $T_{cont.}$ to state "1". A strobe voltage is then generated at its output. If there is information in register 1, i.e. if any flip-flops are in state "1", then circuit AND-2 will be opened and AND-1 closed by an appropriate voltage from the output of circuit

OR-4. Then the strobe voltage will pass through circuit AND-2 to the register's strobe line. The register is designed for the direct selection of information i.e. the first of the flip-flops in state "1" is immediately strobed. The number assigned to the flip-flop in binary code will appear at the output of the register 1 coder.

During operation it is possible that several adjacent flip-flops in register I will be switched to state "1". In order to cut down the time required to transfer information to the store and to reduce the number of memory modules used, the number of only the first such flip-flop is transmitted and the total number of flip-flops is indicated. The latter operation is carried out by the coder which indicates the adjacencies. This coder may be dis-connected if so required. The operation of register I and the adjacency coder will be described in greater detail below.

When a voltage occurs at any output of the register 1 coder, a voltage also occurs at the output of circuit OR-5. This voltage is a call for the store which is fed with information from coder 1, registers II and III, the adjacency coder and flip-flop $T_{beg.coll.}$.

After the information has been recorded in the store, a pulse signal is transmitted. The latter switches flip-flop $T_{beg.coll.}$ to state "1" (if the information recorded was not the first concerning the event, then the position of the flip-flop in state "1" is confirmed), and is also transmitted to the input of circuit OR-2. The pulse from the OR-2 output re-sets flip-flop $T_{con.}$ to zero. The strobe voltage is thus removed and the flip-flop in register 1 from which information was fed to the store is re-set to "0". If a group of adjacent flip-flops is in state "1", then the whole group is re-set to "0" with a delay of approximately 0,1 /usec per flip-flop.

After the flip-flop from which information was fed to the store has been re-set to "0", the voltage is removed from the output of the OR-5 circuit, and a pulse coinciding with the instant

when the voltage was removed is passed to gating circuit 1. After passing through it and then through circuit OR-3 and delay line DL-3, the pulse again switches flip-flop $T_{cont.}$ to state "1". Gating circuit 1 will be open if there are no more than two adjacencies in register 1. Otherwise the pulse will pass to the OR-3 circuit from the adjacency coder after all adjacencies (except the last two) have been re-set to the zero state. In this way, flip-flop $T_{cont.}$ is switched to state "1" only after the whole group of adjacencies has been switched to zero. (This is important, for instance, for the test mode when all 32 bits may be switched to state "1").

After flip-flop $T_{cont.}$ has been switched to state "1", the above cycle will be repeated if there is still information in register 1. If there is no more information there, circuit AND-2 will be closed and AND-1 opened. In this case, the strobe voltage will pass through circuit AND-1 after a pulse corresponding to its leading edge switches register II to the next state and also passes to circuit AND-1. The pulse passes from that circuit through delay line DL-1, and circuit OR-2 and re-sets flip-flop $T_{cont.}$ to the zero state. Furthermore, by using the pulse occurring at the output of circuit OR-1 via the above circuit, the next group of ferrite cores will be strobed. If they contain information, it will be transferred to the store; if not, the next set of cores will be strobed . When register II is over-flowing, the pulse will be switched to register III and the ferrite core groups will continue to be strobed. By using the switches in registers II and III, the total number of ferrite core groups strobed may be anything up to 1024 inclusive (i.e. 32768 cores).

After the number of the last group strobed has been recorded in registers II and III, a voltage will occur at the output of circuit AND-3, which will in turn produce a voltage at the AND-4 output after the last item of information has been fed to the store. This voltage releases the spark chamber trigger system which has been locked since the arrival of the trigger pulse.

Flip-flop $T_{end.\ coll.}$ is switched to state "1" by the leading edge of the voltage occurring at the AND-4 output. The voltage

passes from this flip-flop through the OR-6 circuit and will keep register 1 and flip-flop $T_{cont.}$ in state "0". The device is now ready to take further information from the chambers.

Current shapers, current gates and signal amplifiers

The circuits of the current shaper CS and current gate CG are shown in fig. 2a. Negative pulses of 6V and 0.5 /usec are fed to the input of the current shaper. The current gate is open if a negative voltage is fed to its input. The read current pulse which passes through the ferrite cores has a height of about 1.5A and a length of the order of 1 /usec.

The connection of the current shapers and gates to the matrix is shown in fig. 3. Ferrite cores of the 0.7 VT type with an outside diameter of 3mm. are used in the matrix.

The wires connected to the chamber in the high voltage electrode matrix are covered with Teflon tubing and all the cores are coated with epoxy resin.

In order to reduce noise during read-out the matrices are screened, and the signal windings are connected to the amplifiers by screened conductors. The noise level at the amplifier input is about 0,2V and the useful signal 0.8-1.0V. The amplifier circuit is shown in fig. 2b. The pulses at its output have a height of 6V and a length of 0.5 /usec.

Register 1 and coders

Fig. 4 shows a functional diagram of several of the bits in register 1 which records information coming from the ferrite matrices' signal windings and transfers it to the store. The register has 32 bits altogether. Each bit consists of a flip-flop T plus AND and OR logic circuits. The figures denote the number of the bit

and the letters the number of the circuit in the bit. The first bit has a simpler structure than the rest.

Information is recorded in the register by pulses via the input loops. There are voltage connections between the register's bits and also between the register and both coders - the register 1 coder and the adjacency coder.

Before information is transferred to the store, a strobe voltage is passed through the strobe busbar. If information was recorded on flip-flop T-1 (i.e. it is in state "1"), circuit AND-a1 will be open and AND-b1 closed via the inputs connected with the flip-flop. In this case the strobe voltage will pass through the AND-a1 output to the corresponding input in the register 1 coder.

After the information has been recorded in the store, the strobe voltage is removed and flip-flop T-1 re-set to state "0" by the voltage drop thus produced at the AND-a1 circuit output.

The next strobe voltage will pass through circuit AND-b1 because a "permit" voltage will be passing through the other input from flip-flop T-1. The strobe voltage will go as far as a bit with a flip-flop in state "1". As described above, the appropriate voltage will pass from the output of this bit to the register 1 coder input. The register's bits will continue to be strobed until all the information has been transferred.

If there are two adjacent flip-flops in state "1", for instance the 1st and 2nd, circuit AND-c2 will be gated through the input to flip-flop T-2 and the voltage from the AND-a1 circuit will then pass through it. This voltage will be fed to the corresponding input in the adjacency coder.

If the register's first three flip-flops are in state "1", the voltage will also be passed to the AND-c3 output, as that circuit receives the "permit" voltages both from flip-flop T-3 and from circuit AND-c2 via circuit OR-a3.

If only the 2nd and 3rd flip-flops are in state "1", the voltage will appear only at the output of the AND-c3 circuit to which the second "permit" voltage will be fed not from AND-c2 but from AND-a2.

Generally speaking, if there are several adjacencies, then, when the strobe voltage is fed through them, the voltage will pass from the least significant bit to the corresponding input in the register 1 coder. The voltage from the other bits will pass to the inputs of the adjacency coder.

When the information has been recorded in the store, the entire group of adjacencies will be re-set to "0" by the voltage drops that occur when the strobe voltage is taken away.

The circuit of the adjacency coder is shown in fig. 5. Its design is dictated by the fact that there are only two bits set aside for it in the store and that, therefore, its information can have only 4 discrete values. The information from the corresponding 2-32 bit outputs in register 1 is divided into three groups and is fed to circuits OR-1 to OR-3. The distribution of bits per circuit is shown in the diagram.

The voltages from the OR-1 to OR-3 outputs are fed to circuits OR-4 and AND-1 to AND-4. If there are only two adjacent flip-flops in state "1", the voltage from OR-4 passes via AND-5 to the output of OR-6 which is one of the coder's outputs. If there are three adjacent flip-flops in state "1", a voltage occurs at the output of OR-5 which is the second coder output. In this case there will be no voltage at the OR-6 output as circuit AND-5 will be closed by the voltage from OR-5.

If there are 4 or more adjacencies , a voltage will occur both at the OR-5 output and at the OR-6 output after passing through AND-4.

The voltage from the OR-5 output of the adjacency coder is also used to control the operation of the read-out device after it

has passed through gating circuits 1 and OR-3 as shown in fig. 1.

The register 1 coder is a diode matrix which produces the bit number in binary code at its output.

Time characteristics of the device

The time required to transfer information from the ferrite matrices to the store is composed of the time t required to strobe a group of cores, the time t_2 spent on strobing register 1 and the time t_3 taken to read the information into the store.

As can be seen from the functional diagram of the device (fig.1), all the ferrite core groups are strobed, whether or not they hold information, whereas only those bits containing information are strobed in register 1. Consequently, the total time for extracting information T will be:

$$T = Nt_1 + K\ (t_2 + t_3),$$

where N is the total number of ferrite core groups in the system and K is the number of set ferrite cores, where adjacencies in one set are counted as one.

If the system incorporates spark chambers of 25 x 25 cm^2, the maximum number of co-ordinate planes in the chambers may be $M_{max} = 128$, and the maximum number of ferrite core groups (32 cores per group) $N_{max} = 1024$. The K value is determined as a function of the number of sparks recorded by each co-ordinate plane. When only one spark is recorded, $K = M_{max} = 128$.

The time t_{1} required to strobe a ferrite core group is defined as the period between the instant when flip-flop $T_{cont.}$ is switched to state "1", when strobing begins, and the instant when the flip-flop next returns to state "1" (fig.1). This time is estimated at 3 μsec (using microsecond delay lines DL-1, DL-2 and DL-3).

The time t_2 required to strobe register 1 is composed of two

parts. The first part begins with the serial switching of flip-flop $T_{cont.}$ to state "1" and ends with the transmission of a call voltage to the store, i.e. it is defined by the time required for the leading edge of the strobe voltage to pass through the strobe circuit to the appropriate bit. The second part begins when the pulse arrives from the store showing that the information has been acquired and ends when flip-flop $T_{cont.}$ is next switched to state "1". This part is defined by the time required for the strobe voltage decay to pass through the strobe circuit (or through the circuit connected to the adjacency coder), increased by 1 /usec, i.e. by the time the signal takes to pass through delay line DL-3 which is designed to prevent an increase in the operating frequency (1MHz) of flip-flop $T_{cont.}$.

The time taken by the leading edge of the strobe voltage to pass through the strobe circuit and right through the register is approximately $t_{le} = 3$ /usec (i.e. about 0.1 /usec per bit. The time taken by the voltage decay to pass through the circuit is $t_d = 1.6$ /usec, (0.05 /usec per bit). The time taken by the voltage decay to pass through the whole circuit connected to the adjacency coder is considerably greater - approximately $t_{co} = 6.5$ /usec (i.e. 0.2 /usec per stage). However, this value may be ignored as the number of adjacencies rarely exceeds 2-3. Considering that there is an equal likelihood of information in any bit of the register, the following value should be used for calculations,

$$t_2 = \frac{t_{le} + t_d}{2} + 1 = 3.3 \text{ /usec}$$

The total time for recording information in the store with the "record" program is $t_{3max} = 28$ /usec (6). However, the pulse may be transmitted from the store not when recording has finished but on receipt of the codes, i.e. after $t_{3rec.} = 12$ /usec, and the read-out device can begin to search for new information 16 /usec earlier, the time it would take to strobe 5 core groups (if they do not contain information). When one spark is recorded in the co-ordinate plane, $t_3 = 12$ /usec. In this case, the total time required to extract

information from 128 planes will be:

$$T = N_{t1} + K\ (t_2 + t_3) = 5 \text{ msec.}$$

Arrangement of information in the store

The AI-4096 store, into which information is fed from the read-out device, contains 409618 bit numbers. One number is used to record information concerning the number of the ferrite core set by the spark current. The 15 least significant bits of the number are used to record the core number in binary code - the coders in registers 1, II and III (viz fig. 1) are each assigned 5 bits. The register 1 bits are given the code n-1 where n is the position of the bit in the register.

The 16th and 17th bits are assigned to the adjacency coder. A one in the 16th bit signifies that there are two adjacencies in register 1, a one in the 17th bit signifies three adjacencies and if there are ones in both bits, then there are 4 or more adjacencies. In all threse cases, the number of the least significant flip-flop is recorded in bits 1-5 of the number. The 18th bit is used to separate events; a one in this bit indicates the beginning of an event.

There are ferrite matrices both at the low-voltage and at the high-voltage chamber wires. The information read-out order has been arranged so that information is read out from the cores of each matrix (chamber wire) in turn and so that the total number of conductors between the read-out system and the chamber is kept to a strict minimum. Therefore, each matrix is provided with one current gate (connected to register III) and 8 or 16 current shapers (connected to register II) depending on whether the matrix has 256 or 512 cores. The same shapers and different gates are used for both matrices of a chamber. With this system the information in the two matrices will be read out not in quick succession but with a slight delay. Therefore, if the matrices each contain 256 cores, then the information will be read out firstly from the matrix of the ground

wire in the first chamber (using shapers 1-8 and gate 1), secondly from the matrices of the ground wires in the next three chambers (shapers 9-32 and the same gate) and lastly from the matrix of the high-voltage wire in the first chamber (shapers 1-8 and gate 2). If the matrices contain 512 cores each, then the information will be read out firstly from the matrix of the ground wire in the first chamber, secondly from the matrix of the ground wire in the next chamber and lastly from the second matrix in the first chamber.

The number of store words used for recording each event varies and depends on the number of set ferrite cores.

Testing the device

There are various methods of testing the operation of the device (the components required for testing are not shown in the functional diagram (fig. 1)). The device may be operated in the test mode by pushing a button or by switching on the generator simulating the trigger pulse.

When testing without the ferrite matrices, the pulse from the output of delay line DL-2 is also transmitted to the register 1 input. It may be gated to any of the register's flip-flops by means of switches.

When testing with the ferrite matrices, a suitably shaped pulse from the one-shot OS-1 is transmitted to the test windings of all the matrices or a part thereof, thus setting the ferrite cores in the same direction as the spark current.

The device may be operated either in a single-shot or in a continuous mode for both types of test. In the case of the single-shot test, the device stops operating after all the ferrite core groups have been strobed. The button must be pressed in order to repeat the test. For continuous testing, the one-shot OS-1 is repeatedly triggered by the leading edge of the voltage occurring at the AND-4 circuit output after the last core group has been

strobed and the information transferred to the store.

The device may also be tested without the store. In this case the leading edge of the voltage occurring at the OR-5 circuit output triggers an extra one-shot and a pulse corresponding to the decay time of the one-shot's pulse is used instead of the pulse from the store.

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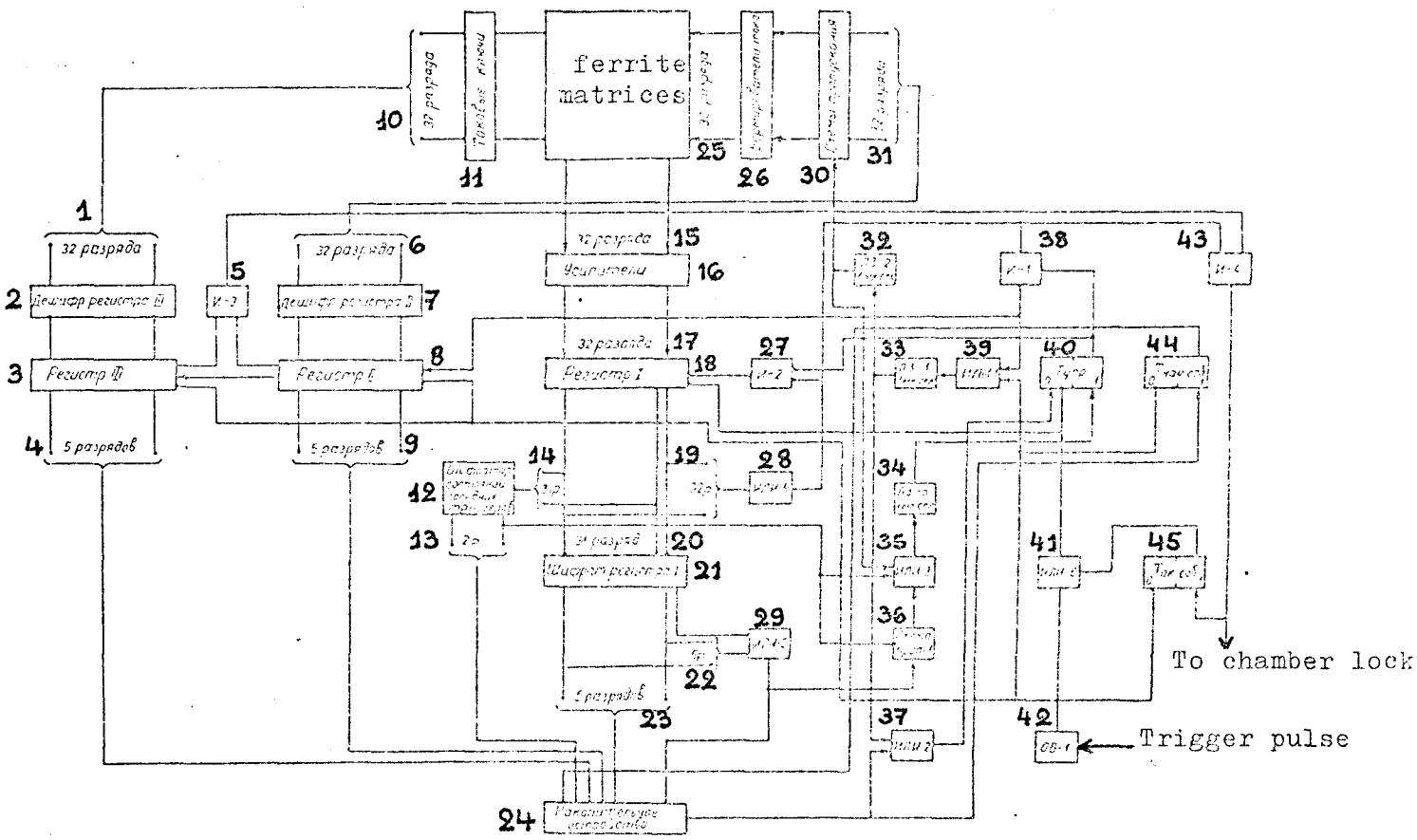

Fig. 1 Functional diagram of information read-out device.

1. 32 bits
2. Register III decoder
3. Register III
4. 5 bits
5. AND-3
6. 32 bits
7. Register II decoder
8. Register II
9. 5 bits
10. 32 bits
11. Current gates
12. Adjacency coder
13. 2 bits
14. 31 bits
15. 32 bits
16. Amplifiers
17. 32 bits
18. Register I
19. 32 bits
20. 31 bits
21. Register I coder
22. 5 bits
23. 5 bits
24. Store
25. 32 bits
26. Current shapers
27. AND-2
28. OR-4
29. OR-5
30. Gating circuits
31. 32 bits
32. DL-2 1 μsec
33. DL-1 1 μsec
34. DL-3 1 μsec
35. OR-3
36. Gating circuit 1
37. OR-2
38. AND-1
39. OR-1
40. T cont.
41. OR-6
42. OS-1
43. AND-4
44. T beg. coll.
45. T end coll.

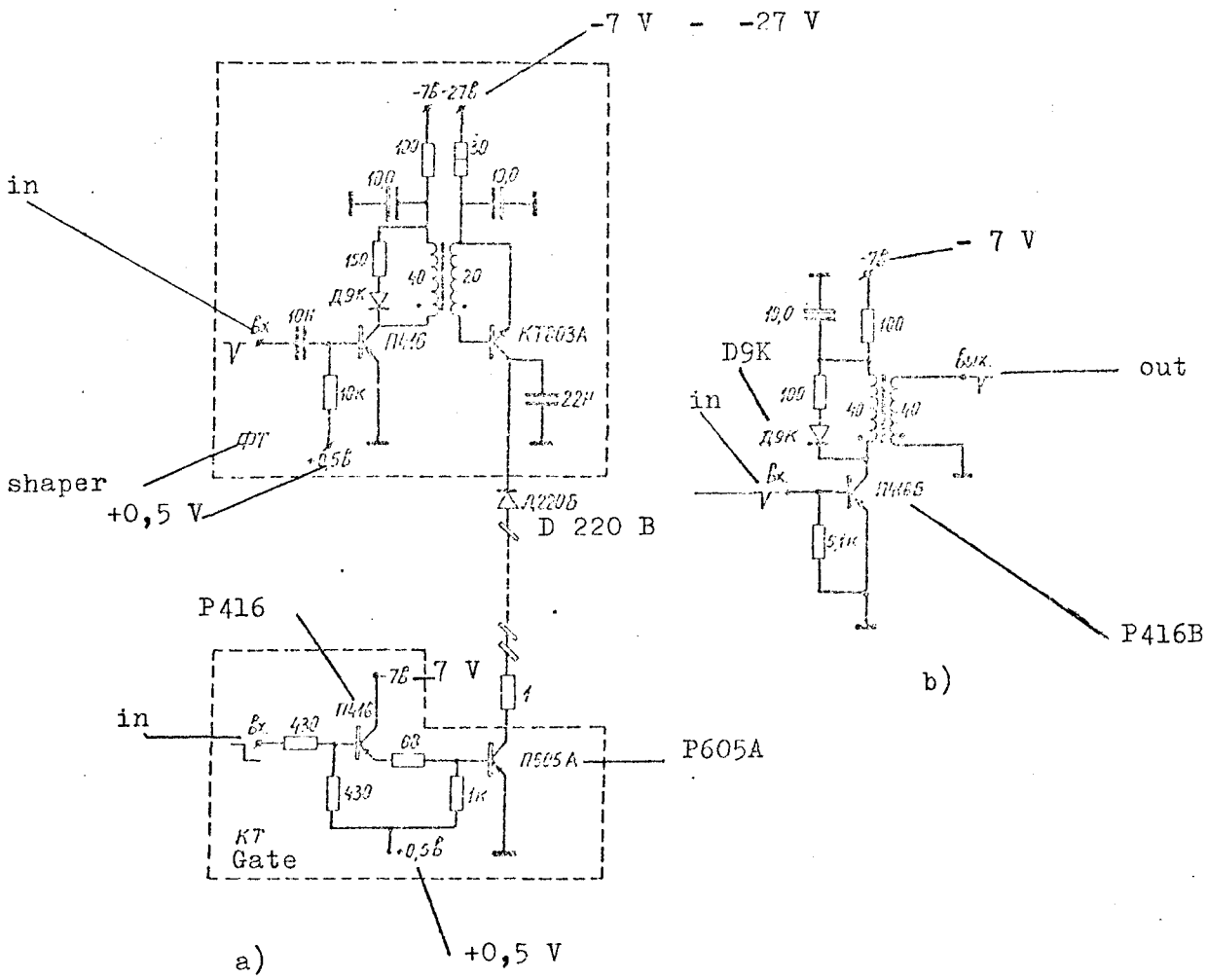

Fig. 2 a) current shaper and gate circuit;
b) signal amplifier circuit.

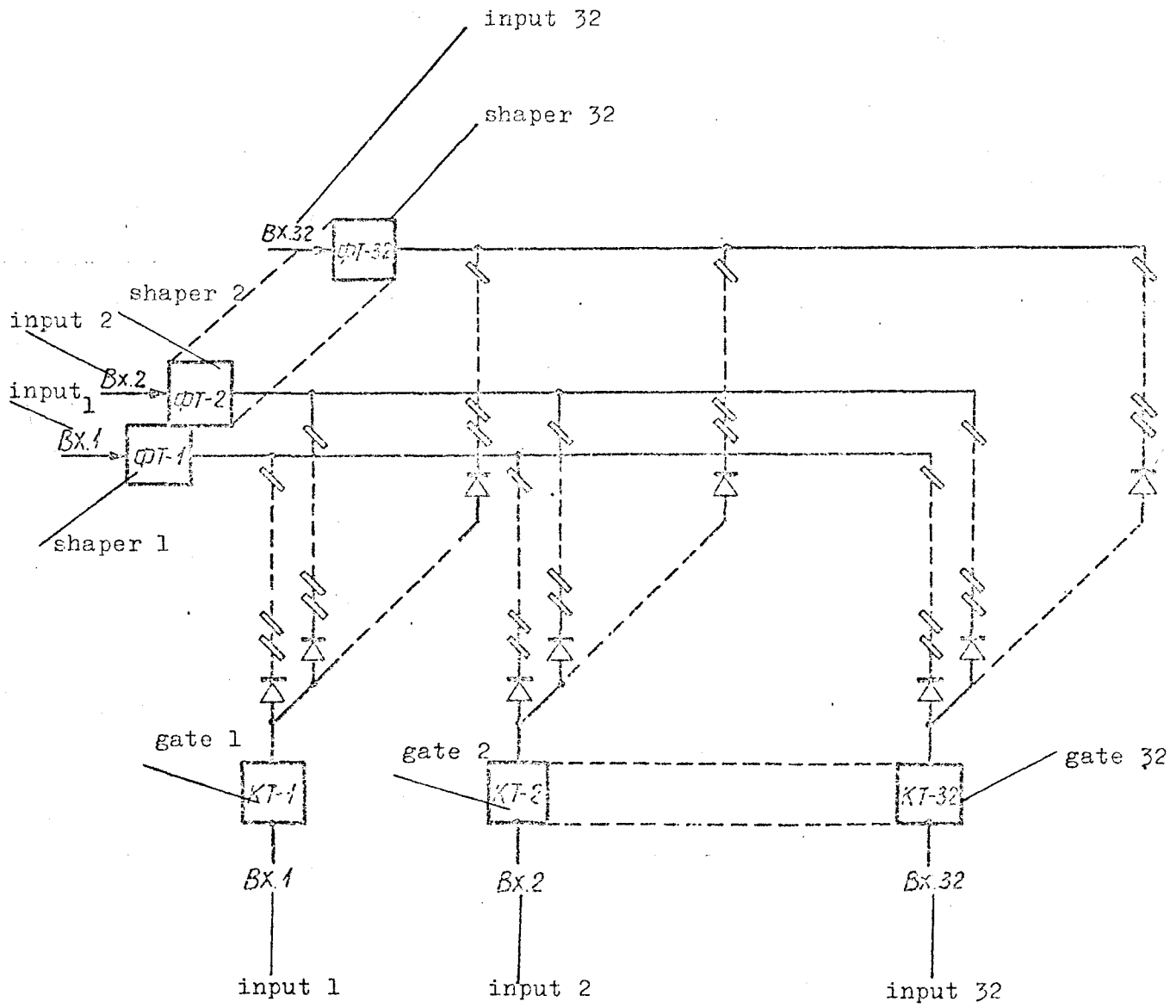

Fig. 3 Diagram of connections between current shapers, gates and matrices.

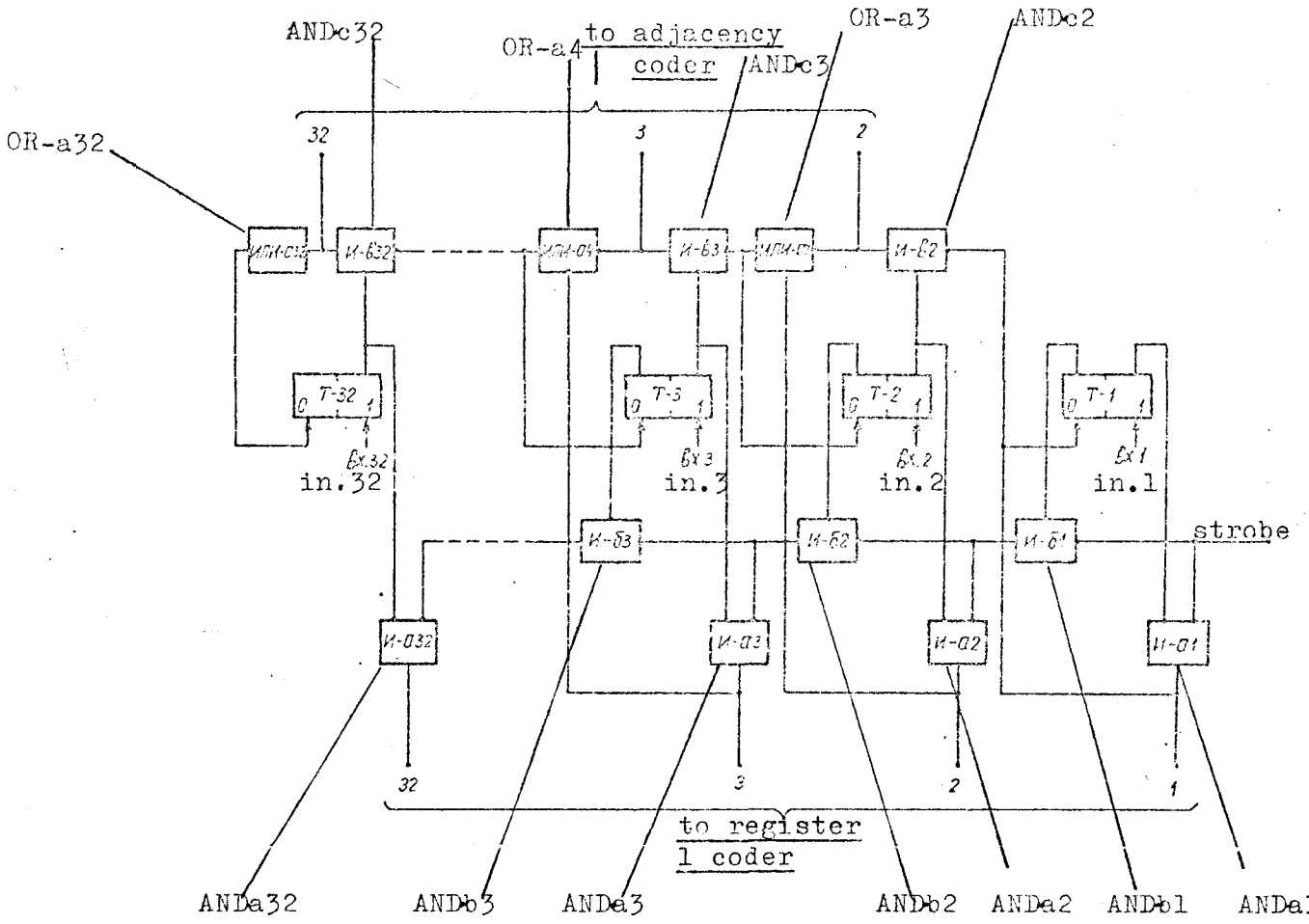

Fig. 4 Functional diagram of register 1.

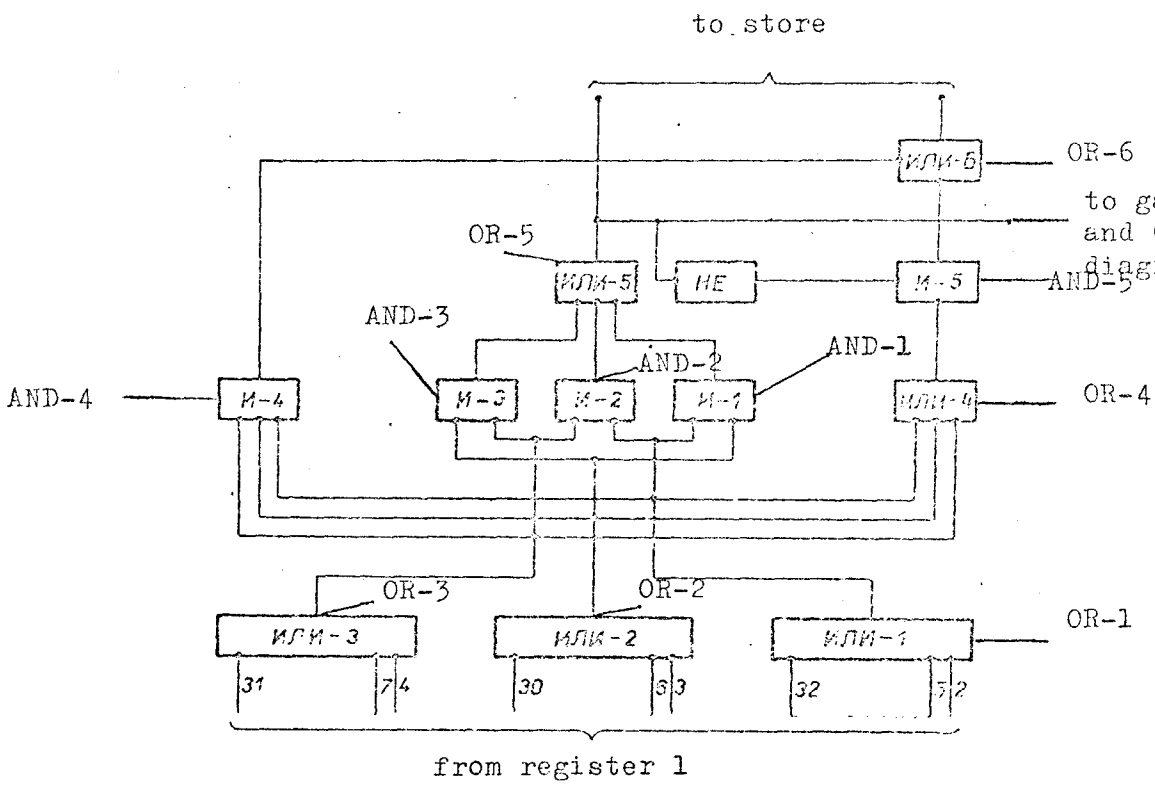

Fig. 5 Adjacency coder circuit.