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Abstract

A front-end readout system with a custom backplane and custom circuit modules has been developed for the RICH subsystem of the PHENIX experiment. The design specifications and test results of the backplane and the modules are presented in this paper. In the module design, flexibility for modification is maximized through the use of Complex Programmable Logic Devices. In the backplane design, a source-synchronous bus architecture is adopted for the data and control bus.

The transfer speed of the backplane has reached 640 Mbyte/s with a 128-bit data bus. Total transaction time is estimated to be less than 30μs per event when this system is used in the experiment. This result indicates that the performance satisfies the data-rate requirement of the PHENIX experiment.

I. Introduction

The Ring Imaging Cherenkov (RICH) detector subsystem of the PHENIX experiment at the RHIC accelerator of Brookhaven National Laboratory is the primary device for electron identification. It uses 5120 photomultiplier tubes (PMT) to measure Cherenkov photons [1]. Both charge and timing information from each PMT is recorded. A dynamic range of up to 10 photoelectrons is required for charge information, and a minimum amplitude of 10% of one photoelectron must be seen, giving a requirement of 10-bit amplitude digitization. Timing resolution of less than 200 ps is required to reduce background hits caused by electrons originating elsewhere than from the interaction vertex. The peak interaction rate is about 14 kHz in Au+Au collisions and will reach about 10 MHz in p+p collisions in a future luminosity upgrade. A system using Level-1 (LVL-1) trigger and analog memory unit (AMU) has been designed to achieve deadtimeless data acquisition under these conditions. The RICH readout system is a newly designed system customized for the RICH subsystem to maximize readout speed and implementation density.

The front-end readout system handles local LVL-1 trigger generation, data collection and buffering, formatting, and sending data to the data collection modules (DCM). In order to achieve an event rate of 25 kHz as mandated by PHENIX overall specifications, it is required that the front-end readout system completes the data transfer within 40μs.

II. Overview of the RICH Readout System

The RICH readout system consists of eight crates with 15 modules per crate. Each 9U VME-compatible crate has one Controller Module, 10 AMU/ADC Modules, 2 LVL-1 Trigger Modules, and 2 Readout Modules (see Figure 1). The Controller Module is connected to a Master Timing Module (MTM) via a G-Link fiber [2], which broadcasts the timing information and control signals. The Readout Module is connected to the data collection module (DCM) via 2 G-Link fibers (4 G-Link fibers in the future), and the LVL-1 Trigger Module is connected to the Global LVL-1 module via 2 G-Link fibers.

The RICH LVL-1 trigger is one of the six local LVL-1 triggers, which is generated every bunch-crossing cycle. In the case of RICH detector, the LVL-1 trigger signal is formed as a serial data packet of 80-bit length digitized from the current-mode summation of 20 photomultiplier-tube signals in order to find a ring image of the Cherenkov radiation.

Sixty-four channels of photomultiplier-tube signals are separately digitized in a single AMU/ADC Module, where analog memories hold an integrated charge signal and a time-to-amplitude converted (TAC) signal recorded at each bunch-crossing. Once a global LVL-1 signal is received, stored voltages coincident with the trigger are converted to digital data and are buffered in the Readout Modules. The resulting data are formed into a serial data packet and sent to the DCM.

The Controller Module performs all of the functions associated with front-end electronics control, command interpretation/execution, and communication. In normal operation mode, control and timing signals are received from the MTM. In non-operation mode, the slow control and download, *i.e.* initialization, reconfiguration of programmable devices, parameter setting, *etc.*, are performed via the ARCNET serial link.

A symmetric bus architecture is adopted as the system buses. They are named Common Bus for control signals and Separate Bus for data transfer. The buses extend on both sides of the central Controller Module, and are operated in so-called 'source-synchronous timing mode' instead of 'common-clock timing mode' used for usual synchronous system [3]. On the

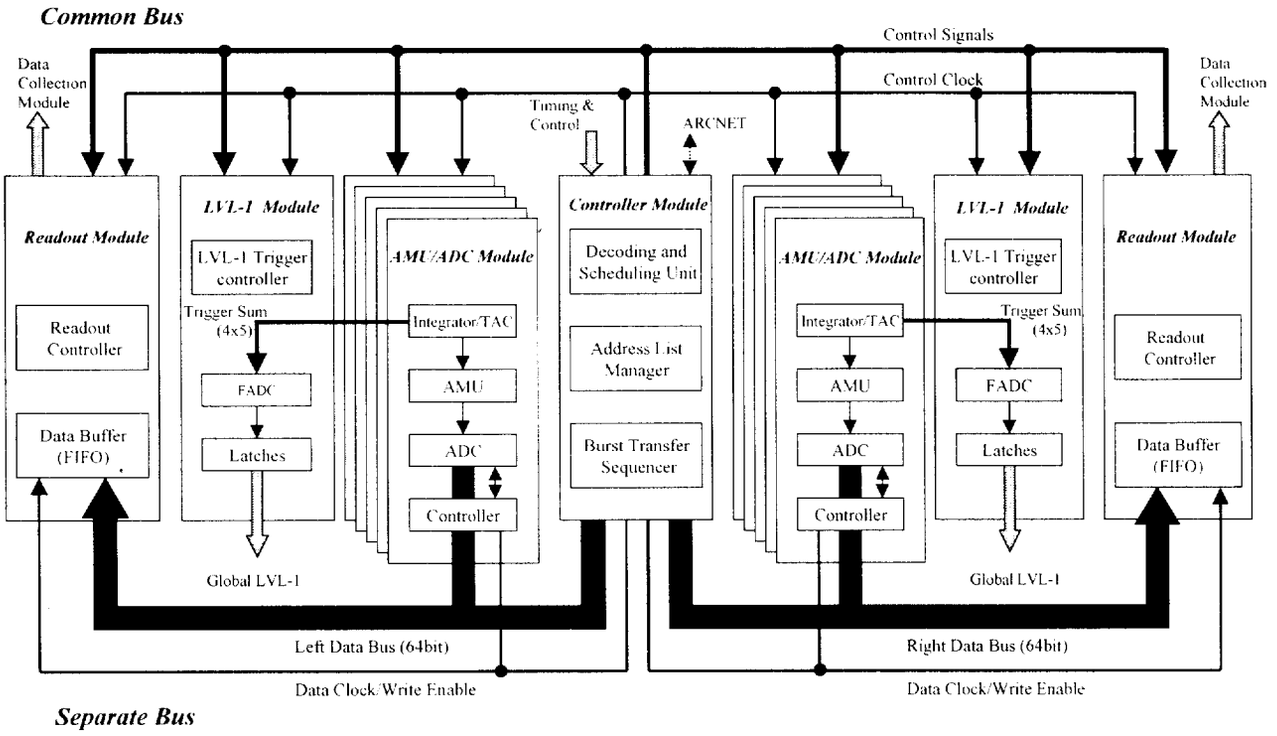

Figure 1: Block diagram of RICH Readout System for a single crate.

other hand, precisely synchronized timing signals such as the AMU-write or TAC-stop signals are independently provided to the modules from the Controller Module front panel using twisted-pair cables with the same total delay time, as adjusted by cable length. These timing signals are generated from the beam-crossing clock of the MTM in the Clock Distributor daughter Board (CDB) on the Controller Module with less than 200 ps time jitter. The control clocks of the Common Bus, namely the beam-crossing clock (BC) and the 4x beam-crossing clock (4BC), are also generated from this board and are distributed to the backplane via the Controller Module. The data clocks of the Separate Bus are generated from the control clocks on each AMU/ADC Module or on the Controller Module, as needed, only while the module is performing a burst transfer transaction.

The global timing diagram of the RICH readout system is shown in Figure 2. The PMT signal appears after the bunch-crossing, *i.* ., the rising edge of BC, then the TAC start signal (TAC-start) is generated from a Constant Fraction Discriminator and is fed into the TAC. At the rising edge of the TAC-stop, the TAC is stopped. The trigger-sum current is sent out synchronized with the trigger-sum clock, which in turn is generated from the beam-crossing clock, with the capability of phase adjustment in 1/8 BC steps. Within 5 BCs, the LVL-1 Trigger Module digitizes the trigger-sum current and sends the data packet to the Global LVL-1 Module. The LVL-1 accept signal is generated from the MTM after 40 BCs delay to allow for the LVL-1 trigger decision time. The output voltages of the TAC and the charge integrator are memorized in the AMU cells at every rising edge of the BC. If a LVL-1 accept signal is received, the voltages of the AMU cell coinciding with the previous and post clock of the event are digitized. In contrast, the TAC output one beam clock after the event is utilized as the TAC signal because the output voltage of the TAC needs to settle. Once the digitization is completed, event data are collected from each module into the Readout Modules and sent to the DCM along with header and trailer information.

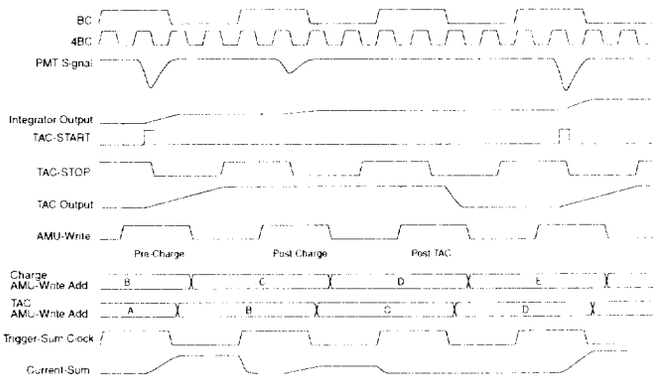

Figure 2: Timing diagram of RICH readout system. Cross symbols indicate signals used for digitization. TAC write address is output one BC after charge address.

III. Front-End Modules and Circuits

A. AMU/ADC Modul

Figure 3 shows a picture of the AMU/ADC Module. Two kinds of ASIC chips are used on it: One is the AMU/ADC chip comprising 32 channels of 64-cell analog memories and

Wilkinson 12-bit Analog-to-Digital Converters (ADC), which is fabricated in the 1.2μm N-well HP CMOS process. The other is the Integrator/TAC chip, which is fabricated in the 1.2μm N-well Orbit CMOS process. The Integrator/TAC chip consists of eight channels of Charge Integrating Amplifier (CIA) and Variable Gain Amplifier (VGA) for charge measurement, Constant Fraction Discriminator (CFD) and Time-to-Amplitude Converter (TAC) for timing measurement, and two pairs of current-sum circuits. Four AMU/ADC and eight Integrator/TAC chips are implemented per module. Both chips have been developed at the Oak Ridge National Laboratory [4,5,6].

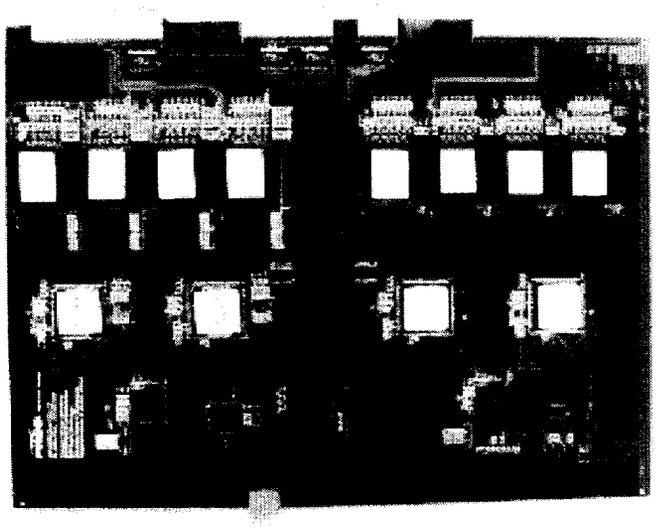

Figure 3: AMU/ADC Module. Left side in the picture is upper side in the crate.

After being amplified by the PMT preamplifiers, which are mounted on the RICH vessel, sixty-four PMT signals are fed into each AMU/ADC Module from the backplane. These pass through the backplane from a transition card inserted on its rear side. The dynamic range of the PMT signals is 16pC to 160pC before the CIA, corresponding to 1 to 10 photoelectrons. The PMT signal is split into timing and charge signals in the Integrator/TAC chip. The timing signal is discriminated and fed into the start of the TAC, while the charge signal is integrated at 3.3mV/pC and amplified at a gain anywhere from 4 to 12 by the VGA, adjusted so that the voltage satisfies the ADC dynamic range. Presetting of the VGA gain is performed via the ARCNET. The gain control data from the ARCNET are sent to the serial data register in the Integrator/TAC chip through the backplane. The programmable parameters of the AMU/ADC chip are also preset with the same method.

The AMU/ADC chip is operated at 10MHz for writing and reading the AMU and at 100MHz for the ADC ramp clock, and in 10-bit conversion mode without using the correlator function. The AMU write- and read- address are managed by the Address List Manager (ALM) on the Controller Module, while the ADC address is issued by the AMU/ADC Burst transfer Controller (ABC). The ABC, implemented in an ALTERA MAX7128 CPLD [7], is responsible for controlling the AMU/ADC and transferring the data via burst mode to the Readout Module. The pairs of AMU/ADCs for charge and TAC are implemented on the upper and lower sides of the module.

B. Controller Module

The Controller Module (Figure4) is the central processing unit of the readout system. The Controller Module consists of a Clock Distribution daughter Board (CDB), a Generic ARCNET controller daughter Board (GAB), a slow controller (K2), a Decoding and Scheduling Unit (DSU), an Address List Manager (ALM), and a Burst Transfer Sequencer (BTS). The GAB was developed at Brookhaven National Laboratory for the PHENIX experiment.

The CDB receives timing information from the MTM via the G-Link and generates timing signals and system clocks. The phase of the timing signals for AMU-write, LVL-1 trigger-sum clock (LVL1 P.P.), and TAC-Stop can be changed by a Clocker Chip in 1/8 BC step. These signals are transmitted as PECL Levels via Category-5 twisted-pair cables usually used for 100Base-T Ethernet. The system clocks BC (Beam Clock), 2BC (2x Beam Clock) and 4BC (4x Beam Clock) are generated by the Clocker and are provided to the motherboard and the Common Bus.

The initialization after reset or power-up is performed through K2 via serial line to the backplane or via special line for a single chip. The K2 is the extension I/O for the COM20051 controller on GAB. The reconfiguration of the SRAM type Complex Programmable Logic Devices (CPLD) used for the DSU and the ALM is also managed by the COM20051 through K2. Reconfiguration data are transmitted from the online control system via the ARCNET. The EEPROM type CPLDs used for the Clocker, the K2 and the BTS are not reconfigured via the ARCNET but instead are configured before installation.

The operational codes (MODE_BITS), global LVL-1 trigger signal (LVL1_Accept), and readout enable signals (ENDAT) are passed to the DSU via the Clocker. The DSU decodes the MODE_BITS and schedules the data collection. Following the commands encoded in the MODE_BITS information, DSU controls the BTS, ALM, and all other Modules. The DSU also generates header information including event number and an AMU cell address when the LVL1_Accept is received. All of the exception handling is also managed by DSU.

The LVL1_Accept and ENDAT are transmitted from the DSU to the ALM and the Readout Module only during the operation mode. Once LVL1_Accept is received, the DSU asserts an A-D conversion signal (ADC_Start) to the AMU/ADC Modules after the ALM outputs the AMU address on the bus. After the conversion, the DSU asserts a signal to start the burst transfer transaction (Transfer_Go) if no burst transfer transaction is proceeding. The BTS handles all of the

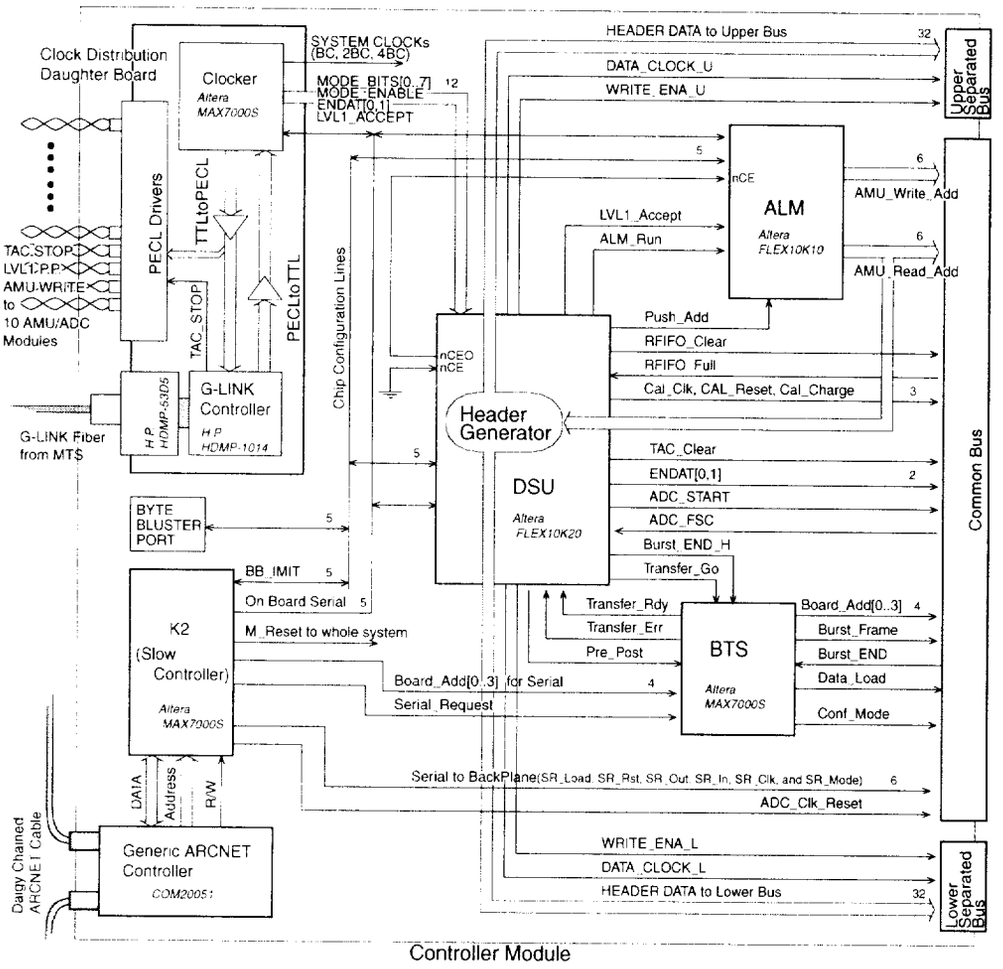

Figure 4: Block diagram of Controller Module.

burst transfer transaction in response to Transfer_Go signal from the DSU. Upon completion of the burst transfer transaction, the BTS returns the Transfer_Rdy signal that indicates the next transfer is acceptable. The BTS returns the Transfer_Err to the DSU if the burst transfer has finished with an error. The mechanism of the burst transfer is explained in the following section.

The ALM manages the AMU cell address during its write- and read- operation. The write-operation is repetitive and synchronized with BC, while the read-operation is only started when the LVL1_Accept signal is received. The ALM keeps available addresses to be written and also keeps addresses to be set aside pending A-D conversion.

Figure 5 shows a block diagram of the ALM. The ALM consists of two FIFOs and a shift register. AMU cell addresses for the write-operation are kept in the available address FIFO. The shift register provides delay for the LVL-1 latency, where AMU cell addresses are shifted with the beam clock. After a fixed delay an AMU cell address is selected at the exit of the shift register if the LVL1_Accept signal received is true. The AMU cell address is moved to the accepted address FIFO when the LVL1_Accept signal received is true, while the cell address is returned to the available address FIFO for reuse when the LVL1_Accept signal received is not true.

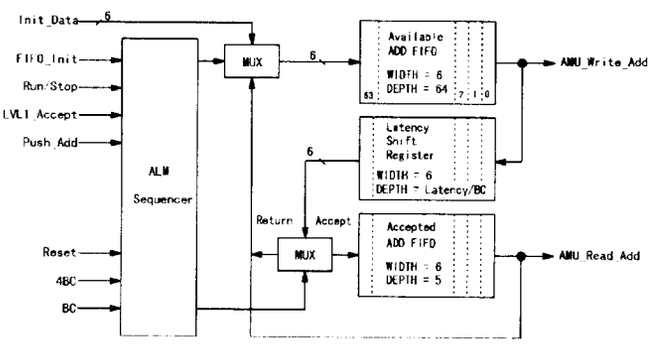

Figure 5: Block diagram of Address List Manager.

The ALM is controlled by the DSU. In START mode the ALM is circulating cell addresses and waiting for the LVL1_Accept signal. The A-D conversion is started by the DSU when a true LVL1_Accept signal is received, then the AMU_Read_Add is output onto the bus. After the A-D

conversion completes, the ALM pushes a used address back into the Available FIFO when the Push_Address signal is asserted from the DSU. In STOP mode an initialization of the available address FIFO (FIFO_Init) must be performed to download AMU cell address 0 through 63 after a reset or power-up.

The DSU and the ALM are implemented in ALTERA FLEX 10K20 and 10K10 [7], respectively. Since the FLEX 10K has embedded Array Blocks of RAM, the width and depth of the FIFOs and the latency shift register can be reconfigured from a remote computer via the ARCNET.

C. *Readout Module*

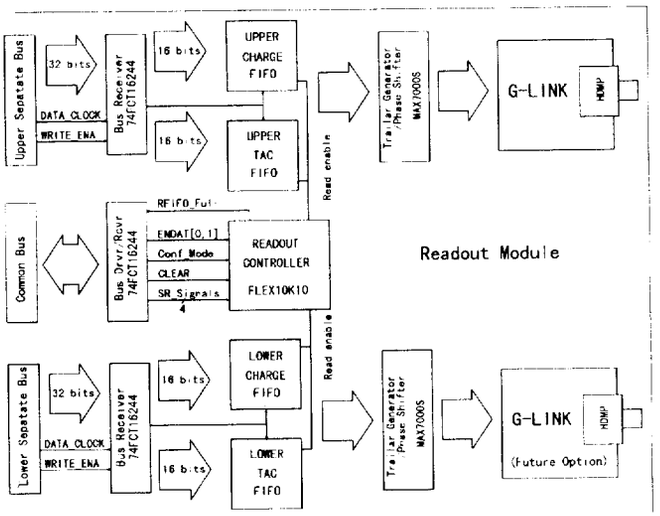

Figure 6: Block diagram of Readout Module. Data from the Lower Separate Bus are transmitted to the upper G-Link port in the initial implementation.

The Readout Module (Figure 6) collects data from AMU/ADC Modules, and sends the formatted data to the DCM. Two Readout Modules are connected, one each to the left and right 2x 32-bit Separate Bus. Each module has two identical circuit, one each in the upper and lower parts, corresponding to the pairs of AMU/ADC chips for charge and TAC measurement. Header information and charge data are transferred to the upper and lower Charge FIFOs in parallel. The header information and TAC data are also transferred to the upper and lower TAC FIFOs. The data packet is built by the Readout Controller in the order of : the header, charge data and TAC data. Although both the pre- and post- data are sent to the FIFOs, the pre-TAC data are thrown out at this readout stage. The readout controller sends the data packet to Phase Shifter/Trailer Generator chips where longitudinal parities are calculated and added to the end of the data packet. The packet data are sent to the G-Link after being shifted by a half clock cycle in order to keep setup/hold time away from the rising edge of the 4BC. Finally the trailer bit information is added.

The readout is driven by the ENDAT0 or ENDAT1 signal received from the MTM when the Readout FIFOs are not empty. In the initial implementation of PHENIX, the data are transmitted via a single G-Link port. Data from upper and lower halves are send sequentially under control of ENDAT0 and ENDAT1, respectively.

The Readout Controller and the Phase Shifter/Trailer Generator are implemented in ALTERA FLEX 10K10 and MAX7128 CPLDs [7], respectively.

D. *LVL-1 Trigger Module*

The LVL-1 Trigger Module (Figure 7) generates the local LVL-1 trigger signal and sends it to the Global LVL-1 Trigger Module via the G-Link. In the RICH subsystem the current-sum of 20 PMT signals is utilized as the trigger to find a ring image of the Cherenkov radiation. The current-sum of four PMT signals is output from each Integrator/TAC chip to the backplane. Subsequently, the current-sum from 5 AMU/ADC Modules is summed, simply by connecting to the same line, and sent to the LVL-1 Trigger Module. Sixteen sum signals, *i.e.*, 320 channels of PMT signals, are handled by a single LVL-1 Trigger Module. Reference current-sum signals from the Integrator/TAC chip are also provided to the LVL-1 Trigger Module. The range of the current signal is from 2.5mA to 7.5mA corresponding to 0 to 70 photoelectrons, and the reference current is 7.5mA. The currents are converted to voltages by pull-up resisters and are fed into an operational amplifier AD8002, which converts the differential voltage at unit gain in order to meet the dynamic range (1.6 to 3.6 V) of the input voltage for the AD876 Flash Analog-to-Digital Converter (FADC). The AD876 is 10-bit CMOS FADC with an on-chip sample-and-hold amplifier [8].

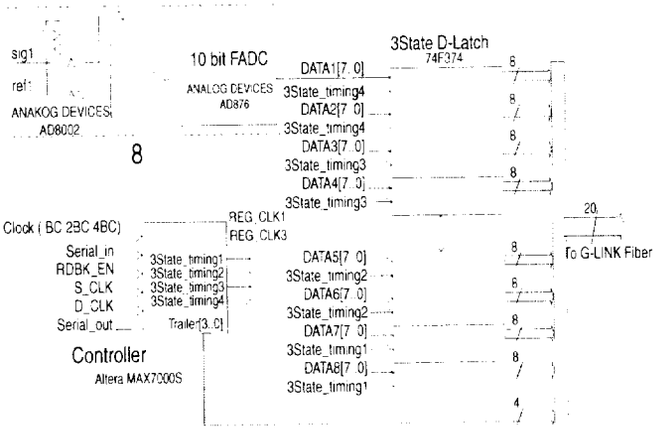

Figure 7: Block diagram of LVL-1 Trigger Module, showing a half of the circuit. Sixteen inputs and Latches are controlled by a single Controller chip.

The control clocks are fed into a Controller chip on the LVL-1 Trigger Module from the backplane. The LVL-1 Controller chip generates the FADC clock and Latch clock from these control clocks with capablity of adjustment in 1/8 BC step. The sum current signals are converted to 10-bit digital data after 3.5 BCs. The eight most significant bits are transferred to D-Latches and sent to the Global LVL-1 Module at the 4BC frequency (~38 MHz). The packet data are 20 bits

wide, formed from 16 bits (8 bits data x 2) plus 4 bits header information. Four data packets are transferred to the Global LVL-1 Module within one BC cycle.

IV. Bus Architecture and Performance

A. Source Synchronous Bus Architecture

In recent years, the source synchronous bus has been actively discussed for high clock rate board design or VME bus extension [3]. Usually in the common clock timing mode, the clock is generated elsewhere in the system and is used to launch data out of the driver and latch them into the receiver. The maximum operating speed can be estimated by

$$Period = T_{Driver} + T_{Interconnect} + T_{receiver} + T_{Skew} \qquad (1)$$

where T_{Driver} is the driver's output valid delay, $T_{Interconnect}$ is the interconnect delay, $T_{Receiver}$ is the receiver's input setup time and T_{Skew} is the skew between the clock at the driver and receiver. $T_{Interconnect}$ and T_{Skew} strongly depend on not only the trace of the signal line via the backplane but also the capacitive load of the inserted module.

In the source synchronous system design, the timing difference between the clock and the signal is compensated because they are generated on the Controller Module (see Figure 1). The speed of the bus is now given by

$$Period = (T_{Driver} + T_{Interconnect} + T_{receiver} + T_{Skew})_{Data} - (T_{Driver} + T_{Interconnect} + T_{receiver} + T_{Skew})_{Clock} \qquad (2)$$

Since the acquired data or the header information is transferred from the AMU/ADC Modules or the Controller Module, a timing mismatch between the clock and signal arises. To avoid this, the clock is generated from the same module as the data in our source synchronous system.

The bus speed is estimated with equation (1) applied inside the module itself. In other words, if the module can operate within the clock rate given by the equation (1), the system is expected to operate correctly. Hence the system can be operated at the speed of the lowest clock rate in all of the modules. Notice, however, that actual speed depends on the noise and the uncertainty of the delays of the parts.

B. Backplan

Figure 8 shows a picture of the backplane. AMP Hard Metric connectors, featuring high density (2mm pitch), low cost and low cross talk, are used. The connectors are grouped into three blocks; the upper block is utilized for the PMT signal input/LVL-1 trigger sum (P5) and the upper Separate Bus (P4), the middle is for the Common Bus (P3) and the lower Separate Bus (P2), and the lower is for the LVL-1 trigger sum/PMT signal input (P1) and power supply (P0). The Separate Buses are symmetrically divided into two individual lines on the connectors of the Controller Module, while the Common Bus is the same line on left and right. 320 digital lines and 64 analog lines for the trigger-sum are wired on the backplane. 640 channels of PMT signal pass through the backplane via the connectors on the transition cards. The power lines supply DC voltages of ±5V and ±12V from a 500W power source on the same crate.

The backplane consists of a nine layer printed circuit board with FR4 core material. The width and thickness of its trace pattern are controlled to have 50 ohm characteristic impedance. The Common Bus and the Separate Bus are driven by the IDT 74FCT16244 and 74FCT166244, respectively. They are CMOS devices with TTL level input and output. The 74FCT16244 is suited for driving high capacitance loads (200pF) and low impedance backplane, while the 74FCT166244 is suited for very low noise and point-to-point driving [9]. Active AC terminations are adopted with a 50 ohm resister and an opamp to form inactive TTL voltage levels to avoid oscillations from logic uncertainties. Terminator cards are inserted from the rear side of the backplane at the Readout Modules for the Common Bus and at the Readout and Controller Modules for the Separate Bus.

The cross-talk between adjacent lines was less than 200mV near the rising edge of the system clock. The 40 MHz clock signal was successfully transferred without problems.

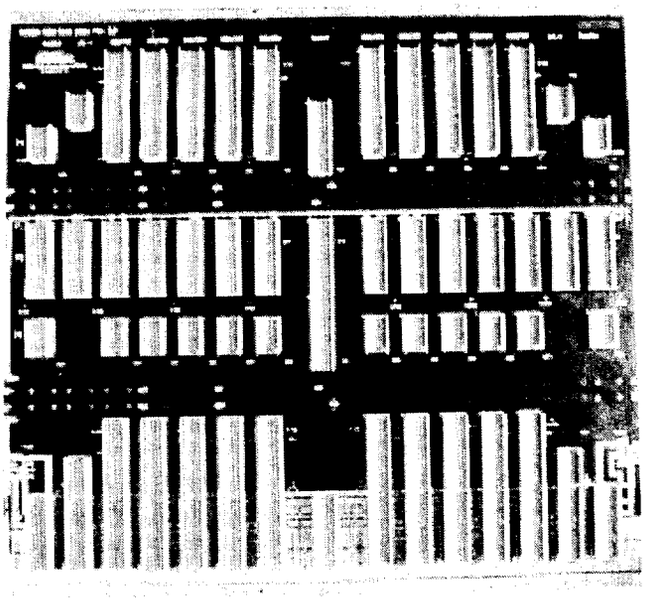

Figure 8: 9U size custom backplane for RICH FEE.

C. Burst Transfer Mechanism

Four channels of digitized data (16-bits per channel) are transferred to a Readout Module in parallel via the Separate Bus during one 4BC cycle. Thirty-two channels of 64-bit data are sequentially transferred from an AMU/ADC Module to the Readout Module during one burst transaction cycle (32 clocks plus overhead) indicated by a Burst_Frame signal, which is driven by the Burst Transfer Sequencer (BTS). The burst transfer transaction is performed on the left and right sides simultaneously using the same Burst_Add and Burst_Frame signals (see Figure 10).

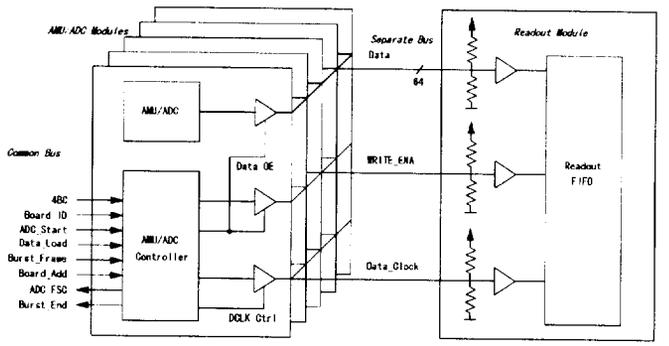

Figure 9: Burst Transfer Mechanism. In actual system, active terminations are used instead of Thevenin termination.

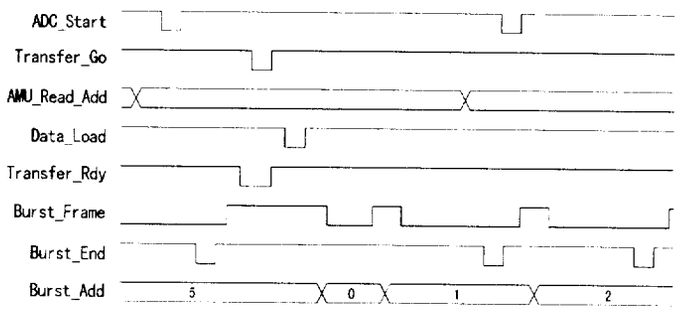

Figure 10: Burst Transfer timing diagram.

Each AMU/ADC Module detects its own board ID (Board_ID) from the backplane, which is pre-assigned to each slot. The Board_ID is 4 bit address. The MSB indicates left or right. The lower 3 bits indicate the burst transfer address (Burst_Add); 0 for the Controller Module, from 1 to 5 for the AMU/ADC Modules, 6 for the LVL-1 Trigger Module, and 7 for the Readout Module. When the Board_Add is the same as the Board_ID, the corresponding module obtains the ownership of the Separate Bus. In the case of the burst transfer transaction, only the Burst_Add is compared. Once the AMU/ADC Module obtains ownership of the Separate Bus, the ABC starts transferring the data using the Readout FIFO enable signal (WRITE_ENA), data clock (Data_Clock) and Data lines (see Figure 9).

After the Transfer_Go signal is issued from DSU, the BTS asserts the Data_Load signal first and then starts sequential transferal. At first, the BTS sets Burst_Add to 0, and header information is transferred from the Controller Module. After that, the BTS changes the address to 1, *i.e.* AMU/ADC Module 1, and asserts the Burst_Frame. The readout transactions for the AMU/ADC Modules are continued until the Burst_Add sets to 5, *i.e.* AMU/ADC Module 5. The burst transfer end signal (Burst_End) is asserted from each AMU/ADC Module after transaction. If the Burst_End signal is not asserted within the Burst_Frame, the BTS returns the Transfer_Rdy with Transfer_Err signal to the DSU.

D. Data Transmission Speed

Figure 11 shows the data processing timing diagram. Once the Controller Module receives a LVL1_Accept signal, A-D conversions are initiated on each AMU/ADC Module. Digitized data are transferred to the Readout Module via the Separate Bus and to the DCM via G-Link at about 800Mbit/s.

An analog to digital conversion completes within 8μs after the LVL1_Accept signal is received, operating in 10-bits mode with 100MHz (200MHz internal) conversion clock. This conversion time includes access time to the AMU. Since the integrated charge information is calculated from the difference between signal sample (Post-event) and baseline sample (Pre-event), two sets of data are transferred in one event cycle. For this reason, it takes another 8μs to convert the post-event. However, the conversion can be started after the pre-event is latched in the output register of the AMU/ADC chip. As soon as the post-event header is generated by the DSU, the BTS starts the burst transfer transaction. Burst transfers of the header and the event data are completed in around 1μs and within 4.3μs plus overhead, respectively. The data transfer to the DCM quickly starts if the ENDAT signal is enable. The data packet is built according to the order: header (9 words), pre-charge (320 words), post-charge (320 words), post-TAC (320 words) and trailer (10 words), and is sent out serially. Transfer time for the pre-charge, post-charge and post-TAC are 5μs, respectively. Thus, the total processing time for each event is expected to be less than 30μs (20μs in the future using 2 G-Link ports). With pipeline processing, the transfer time is expected to be less than 20μs per event.

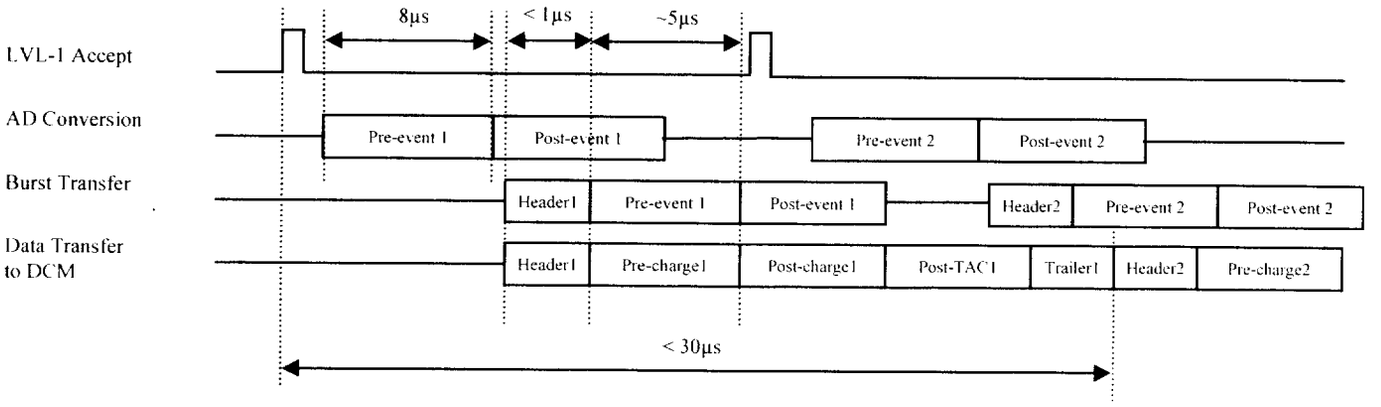

Figure 11: Data processing timing diagram

V. CONCLUSIONS

We are developing the front-end readout system for the RICH subsystem of the PHENIX experiment. A source-synchronous bus architecture is adopted for the newly designed backplane. Since the clock skew due to the difference of the transfer line length and to the load variance from absence of some modules in the testing stage can be neglected, the timing requirement for the board design is greatly reduced even for high clock rate operation. The transfer speed of the backplane has reached 640 Mbyte/s with 128-bit data bus.

The prototype boards have been tested, and final board design is in progress. The performance of the backplane is tested, and digitized data have successfully transferred at 40MHz clock rate without errors.

Total processing time for each event is expected to be less than 30μs (20μs future option). This result indicates that the performance satisfies the requirements of the PHENIX experiment.

VI. REFERENCES

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