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ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Catania

INFN/TC-98/25
7 Ottobre 1998

THE MULTIDETECTOR "CHIMERA" MOTHERBOARDS SYSTEM

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SIS–Pubblicazioni
dei Laboratori Nazionali di Frascati

Istituto Nazionale di Fisica Nucleare
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A B S T R A C T

This report describes a system, designed for the analog front-end of the multidetector "CHIMERA" and the adopted procedures for reduce the crosstalk, due to electromagnetic coupling or through the preamplifiers common power supply lines.

An accurate study of the current limiting circuit and of the power supply filter, which are provided the motherboards, by using SPICE simulation is also presented.

1. Introduction

In the setups where a considerable number of detectors are used the crosstalk levels represent a serious problem. They are very often caused by an inadequate grounding system and a bad power filtering. Indeed it is possible that undesired signals can easily be induced in adjacent channels by electromagnetic coupling or through the common power supply lines.

Due to the short risetimes of the nuclear physics detectors signals, their treatment, in electronics projects, is very similar to the high frequency circuits. The accuracy of the choice of the components and the geometrical configuration of the circuits, to minimize transmission line problems, are also important.

We will describe the procedures and the tests results in a prototype system, which support the charge preamplifier (PAC) chains of the first wheel of the CHIMERA[1] multidetector, which is made of several sets of double telescopes located in a cylinder structure divided into 9 wheels and a center ball.

The detectors to be used are 1192 Si and 1192 CsI(Tl), each one connected to a preamplifier. A single motherboard (M.B.) houses two preamplifiers for Silicon detectors and two preamplifiers for CsI(Tl) detectors.

The system processes the output signals of the detectors and enter them into the electronic chains, located out of the vacuum chamber, for a codification and an identification procedure, allowing the multidetector to work with the requested performance, which are:

- Energy dynamic range from 500KeV up to 4GeV.
- Very low energy threshold (E/A = 0.5 MeV).
- Low crosstalk ($\approx$ 80dB).
- Reduced cost.
- Good thermal stability in a vacuum ambient.

2. General description

The heart of the system is the motherboard, which is a multilayers (six) board where we allocated 5 charge preamplifiers (PAC): 4 are used for the base configuration (2 for Si and 2 for CsI(Tl) detectors), the 5th may be inserted optionally. In this configuration the M.B. supplies the detectors high voltage up to 2kV.

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[1] CHIMERA is a 4π multidetector for heavy-ion physics. Si and CsI(Tl) detectors are used for the ΔE-E, Time of Flight identification techniques and pulse shaping [1].

In the motherboard are also allocated the components of the π cells power supply filter and of the electronics overloads circuits, that respectively, allows suitable separation between channels and controls each power supply line.

Figure 1 shows the block diagram of the motherboard, the figure 15 and the figure 16 show, respectively, its schematic diagram and a picture.

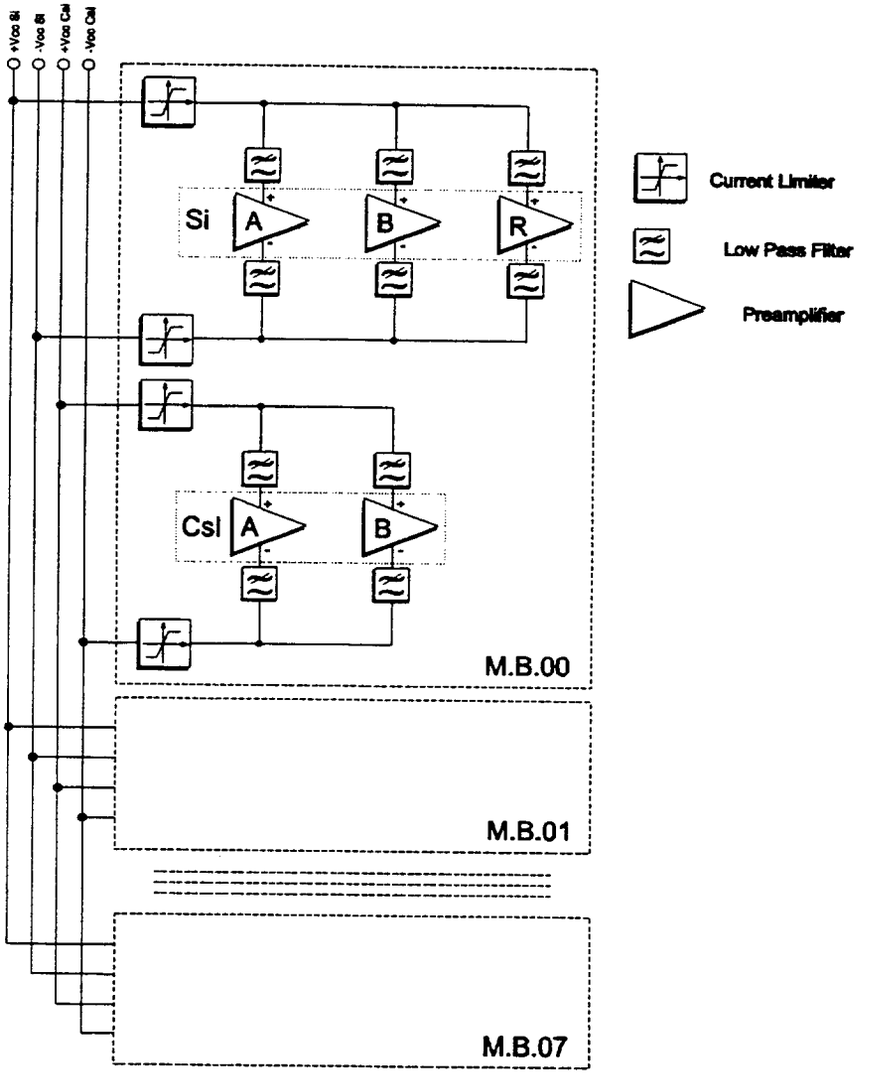

Fig. 1 : Motherboard functional block diagram.

The first wheel of the multidetector is a set of 16 double detection cells (telescopes), each one composed of a Silicon detector and a CsI(Tl) detector. Indeed its has been necessary to optimize the cabling configuration in order to accomodate 32 + 32 detectors-preamplifiers .

The power supply bus drives the voltages (high voltage for detectors and low voltage for PAC) in such a way that a 50 conductors flat cable includes 16 power supply lines and the sensing lines, to compensate the voltage losses due to the line resistance. In particular a (positive and negative) power supply lines pair configuration has been designed to supply 16 homogeneous PAC Si or CsI(Tl) for Low Voltage, a single High Voltage line supplies 8 detectors Si or CsI.

Figure 2 shows the general scheme of the power supply configuration of the first wheel, the figure 17 shows a detail of the "composite bus".

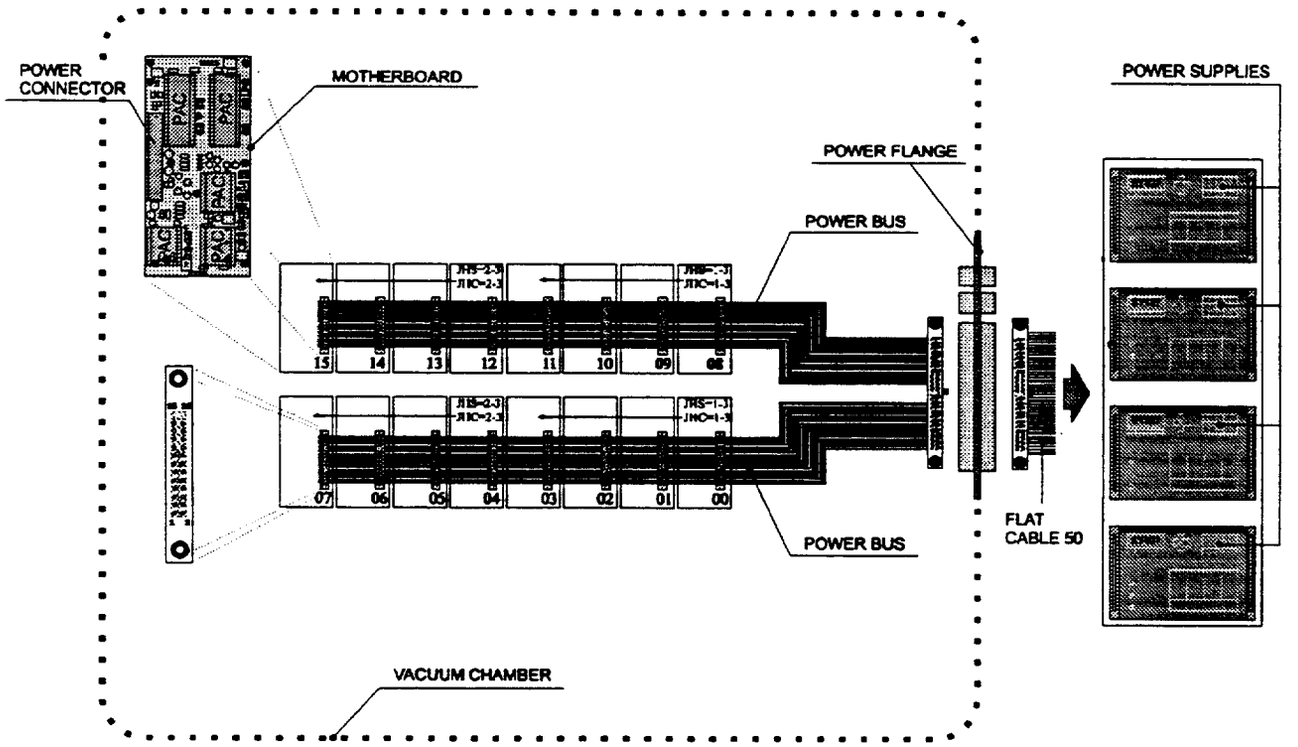

Fig. 2 : General scheme of the power supply configuration.

The output and test signals are conveyed by an array of 8 lines, coming from the M.B.s to the signals flange of the vacuum chamber, where they are grouped in a special housing [(2)]. The results of a functional test, performed to verify the housing power transfer in the adjacent lines, are shown in figure 19.

Figure 3 shows the configuration of the outputs and the tests for 4 M.B.s, in which a test signal supplies 8 homogeneous PAC.

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[2] The adopted housings have been projected on the base of the mechanical and electrical specifications we indicated in collaboration with the I.P.N. of Orsay (Fr) and produced by the 3M (figure 18).

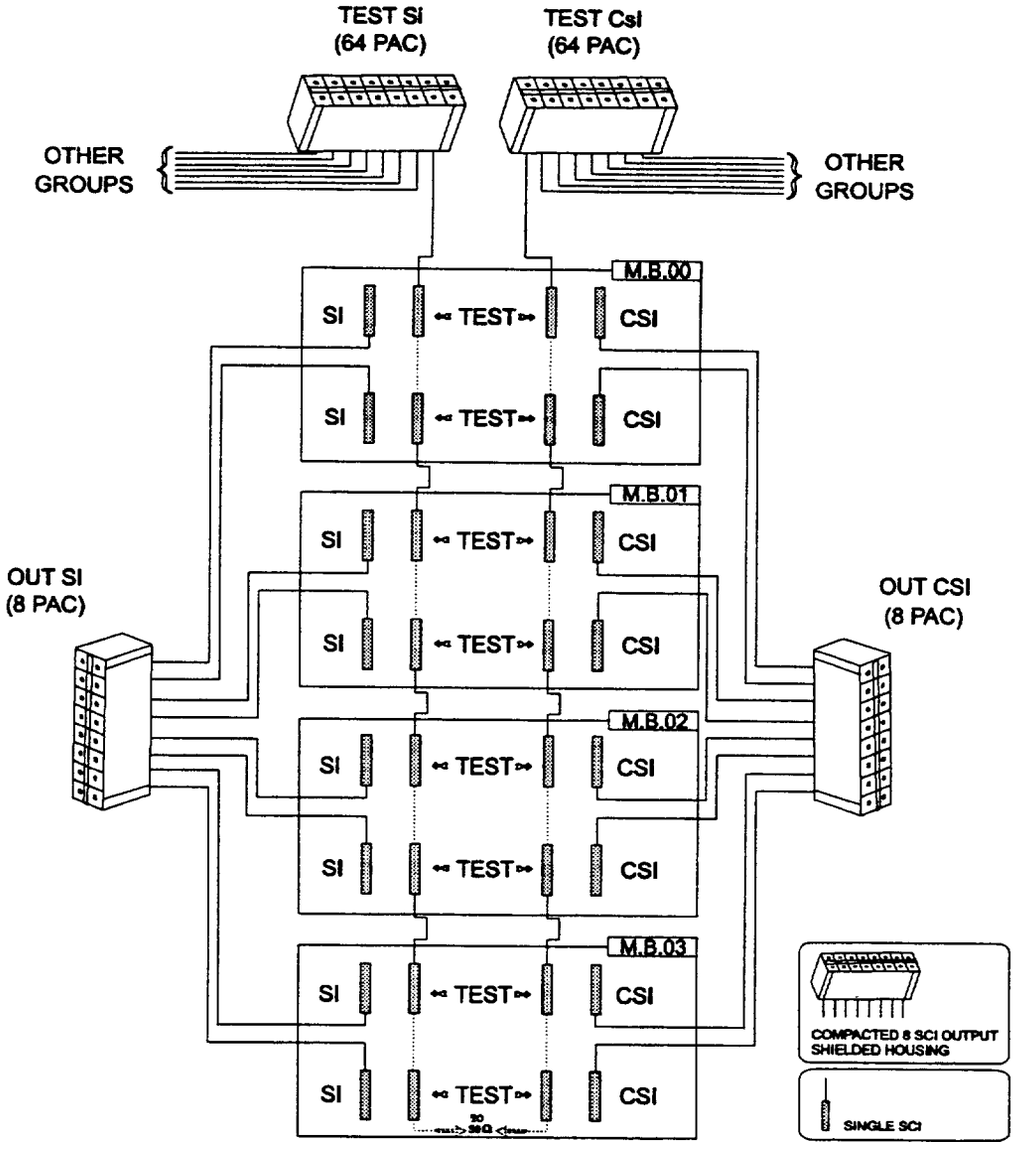

Fig. 3 :General scheme of output and test scheme configuration.

3. Current limiter circuit

Dynamic protection against the overloads is performed by connecting a LP395 which is a very high gain transistor that include on the chip current limiter, power limiter and thermal protection. The LP395, in overload condition, operates the thermal protection by decreasing to few mA the flowing current (OFF state). When the overload is removed the LP395 turn on automatically.

Figure 4 shows the test configuration used to verify the under vacuum reliability of this device.

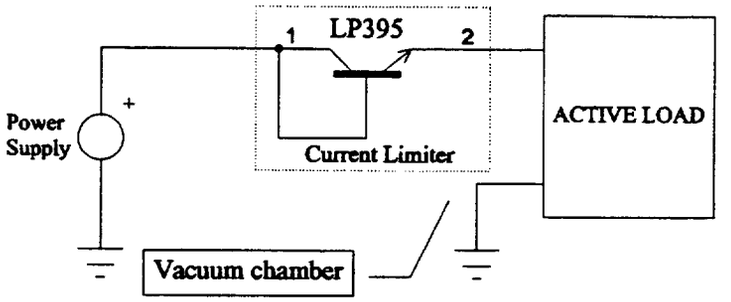

Fig. 4 :Current limiter test scheme.

Two steady states of the mentioned LP395 are possible:

- Ic < 100 mA ON state
- Ic > 100mA OFF state

The normal running corresponds to the ON state. The OFF state is strongly dependent on the environment in which the LP395 is used.

The saturation collector current Ic_{sat} is set to be 100 mA at atmospheric pressure.

Under vacuum, the thermal resistance between the case and the environment increases and Ic_{sat} become 40 mA. At atmospheric pressure, $Rth_{Case-Amb}^{AtmPressure} = 160[°C/W]$, while under vacuum, for the same case temperature, the thermal protection acts for lower dissipated power and consequently Ic_{sat} decreases (see formula 4).

$$t_{Case} = Rth_{Case-Amb}^{AtmPressure} \cdot P_{AtmPressure} \quad (1)$$

$$t_{Case} = Rth_{Case-Amb}^{UnderVacuum} \cdot P_{UnderVacuum} \quad (2)$$

$$\frac{P_{UnderVacuum}}{P_{AtmPressure}} = \frac{Rth_{Case-Amb}^{AtmPressure}}{Rth_{Case-Amb}^{UnderVacuum}} << 1 \quad (3)$$

$$Ic_{sat}^{UnderVacuum} << Ic_{sat}^{AtmPressure} \quad (4)$$

As seen in Figure 5 the static model of the component may be obtained from the slope of the linear part of the LP395 collector characteristic.

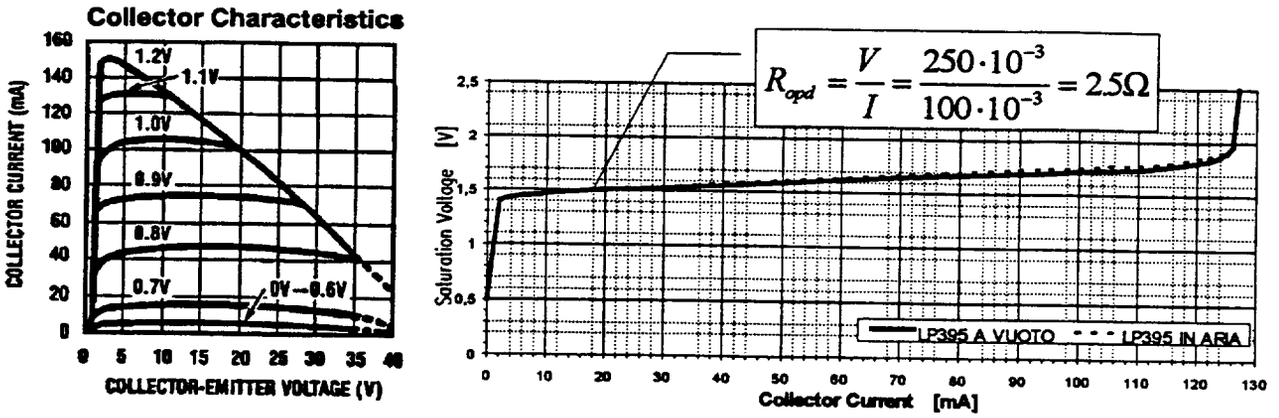

Fig. 5 : LP395 collector characteristic.

The dynamic state is composed of the switching transient during the transitions from the ON state to the OFF state and vice-versa. Its scheduled switching time is 2μsec, which is enough for the request dynamic.

4. PAC Power Supply Rejection Ratio (PSRR)

Generally, a non ideal preamplifier transfers the noise, added to the power supply inputs, to its output, according to a transfer function.

The amplifier network analysis, around a linearizable working point of the device, allows, because of the principle of superposition, to detect three transfer functions as shown in figure 6:

- $G_1(s) = \frac{V_0'(s)}{V_{in}(s)}$, between output signal $V_0'(s)$ and the corresponding input signal,
- $G_2(s) = \frac{V_0^+(s)}{E_r^+(s)}$, between output signal $V_0^+(s)$ and the noise $E_r^+(s)$ added to the positive power line,
- $G_3(s) = \frac{V_0^-(s)}{E_r^-(s)}$, between output signal $V_0^-(s)$ and the noise $E_r^-(s)$ added to the negative power line.

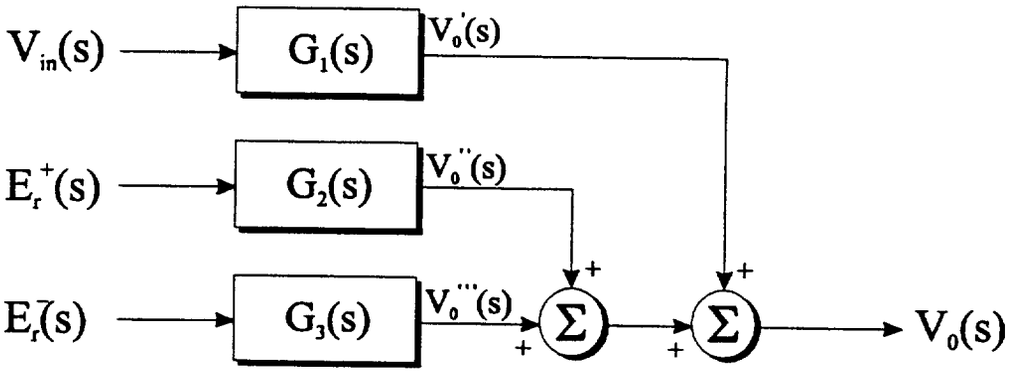

Fig. 6 : Equivalent block diagram of the transferring to the output of a noise on the power inputs.

The above mentioned transfer functions calculation is beyond this report, but it is important to know the noise power supply rejection to build an adequate power supply filter circuit, since, in each M.B., the PACs are supplied through two common pairs of lines.

With a signal $e_r(t)$ applied to one of the power supply input, the equivalent noise $e_{r,eq}(t)$, at the input signal, can be determined.

From figure 6 we have:

$$V_0'(s) = G_1(s) \cdot E_{r,eq}(s) \tag{5}$$

$$V_0''(s) = G_2(s) \cdot E_r(s) \tag{6}$$

If the signal gives the corresponding output signals $v_0'(t)$ and $v_0''(t)$ with the same spectral composition, $G_1(s) \propto G_2(s)$, for the same output signal we have:

$$e_{r,eq}(t) = \frac{e_r(t)}{PSRR} \tag{7}$$

For low PSRR[3] preamplifiers to a power supply noise $e_r(t)$ corresponds an equivalent input noise, $e_{r,eq}(t)$, of the same order of the precedent, so that the preamplifier capability to discriminate a signal from a noise is insufficient and consequently the S/N ratio gets worse.

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[3] The well know definition of PSRR is:

$$PSRR[dB] = 20\log\frac{v_0'(t)}{v_0(t)} \tag{8}$$

where, in the case of the same spectral composition, $v_0'(t)$ and $v_0(t)$ are the output signals corresponding respectively to a noise applied to the signal input of the preamplifier and to one of the power supply input.

5. PSRR measurements

The measurements of the PSRR is performed in two different steps. In the first one (figure 7a-b) the pulsed signal $e_r(t)$ is added to the PAC power supply level, in the second one it is applied to the PAC signal input (figure 7c).

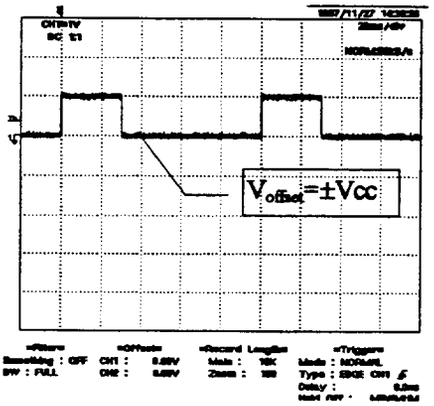

Fig. 7a:$e_r(t)$ added to ± Vcc.

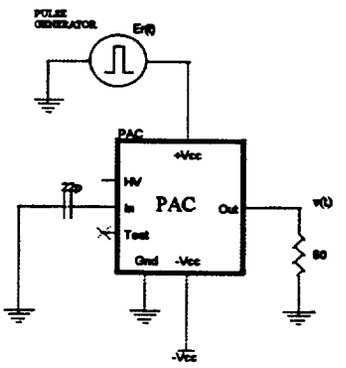

Fig. 7b:$e_r(t)$ on the pos. power input

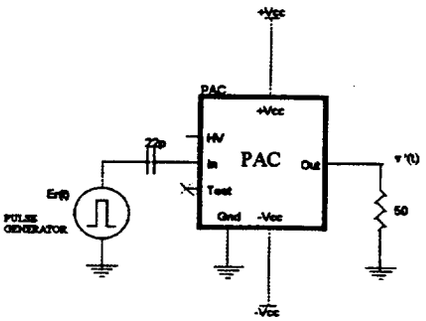

Fig. 7c: $e_r(t)$ on the signal input.

The measurements are made for a set of 10 PACs (both Si and CsI) and the typical output signals relative to this test are shown in figure 20. In table 1 we report the mean peak value of the output signals and the standard deviation σ of the distributions.

	$\hat{v}_0$ [mV] $e_r(t)$ added to +Vcc	$\hat{v}_0$ [mV] $e_r(t)$ added to -Vcc
PAC Si detectors	113.6 σ=5	650 σ≅0
PAC CsI detectors	131 σ=18	1660 σ=69

Table 1

By using the equation (8) one can evaluate the $PSRR^+$ (on the positive power supply) and the $PSRR^-$ (on the negative power supply) for the PACs (see table 2).

	PAC Si detector	PAC CsI(Tl) detector
$PSRR^+$	13 dB	18 dB
$PSRR^-$	-2.5 dB	-5 dB

Table 2

6. Crosstalk

The crosstalk we can detect is mainly due to the power supply net. Indeed the layers structure of the M.B.s, the shortness of the strips connecting the output connectors of the PACs, the metal bus bars, which divide the M.B. plane in sectors for the housing of the PACs, make the EMI effects not measurable (see par. 8).

The current limiter (see par. 3) increases the M.B. power supply lines impedance. Since in a M.B. two PACs are supplied by the same power supply line, a RC decoupling networks is needed to reduce the inductive effects of this device.

By taking into account that all the power supply lines come from the same module, the coupling between "homonym" channels (e.g. SiA ⇔ SiB and CsIA ⇔ CsIB) and "non homonym" channels (e.g. SiA ⇔ CsIA) is represented in figure 8 by the transfer functions K_{Si}, K_{CsI} e $K_{Si \Leftrightarrow CsI}$.

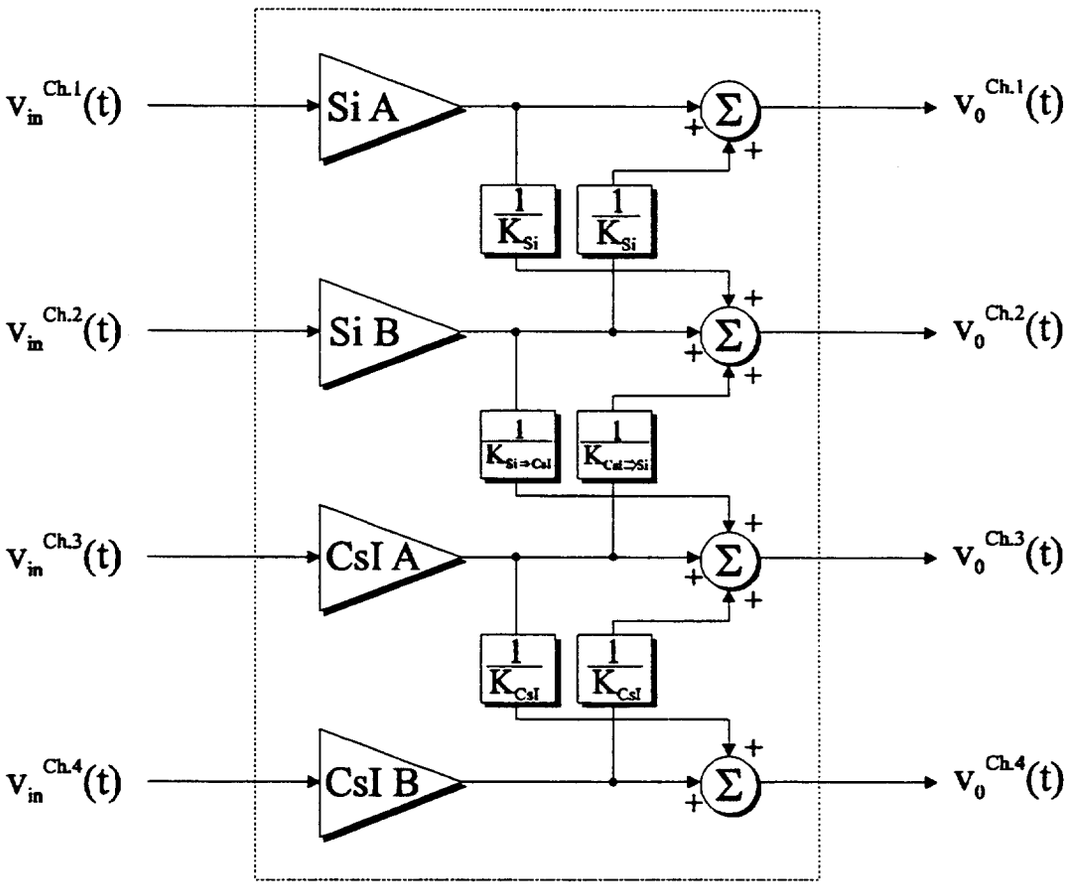

Fig. 8 : Output channels coupling equivalent block diagram.

The channels separation in dB is given by :

$$k_{A\Rightarrow B}[dB] = 20\log\frac{\hat{v}_0^A}{\hat{v}_0^B} \tag{9}$$

where $\hat{v}_0^A$ e $\hat{v}_0^B$ are the peak values of the A and B channels outputs.

K_{Si} and K_{CsI} are increased by an adequate choice of the PAC power supply filter components values. The low value of the PAC PSRR, especially in the -Vcc, is coherent with the relatively high values of the filter capacitors.

$K_{Si\Rightarrow CsI}$ is extremely high because the power supply channels of the Si PAC and CsI PAC, in the same M.B., are different.

Once the PSRR on the positive and negative PAC power supply is known (par. 5) it is possible to make a model of the coupling between homonym channels trough the power supply lines. If the channel A, by generating an output signal $v_0^A(t)$ on a load impedance R_{LOAD} of 1 KΩ, interferes with channel B, it is possible to choice as a model of the PAC A a current generator :

$$I_0(t) = \frac{v_0^A(t)}{R_{LOAD}} \tag{10}$$

The outputs signal $v_0^B(t)$ of PAC B (subjected to the effect of A) is due to the ripple on the power supply terminal input, caused by $I_0(t)$ and R_{opd} (figure 5) and it is equal to the product of the ripple and the PSRR in the corresponding power supply line.

The small signals analysis of the signal transfer between channels A and B of both the Si and CsI PAC is represented by the equivalent circuit in figure 9. C1, C2, C3, R2 and R3 are the elements of the real filter ; R1 represent the static model of the current limiter in linear zone (see par. 3) while R4 is the resistive load equivalent to the PAC B when the transitory ends :

$$R_4 = \frac{|-V_\infty|}{|I_\infty|} = \frac{12}{7.5\cdot 10^{-3}} = 1.6K\Omega \text{ for Si PAC}$$

$$R_4 = \frac{|-V_\infty|}{|I_\infty|}\frac{12}{6.9\cdot 10^{-3}} = 1.7K\Omega \text{ for CsI PAC}$$

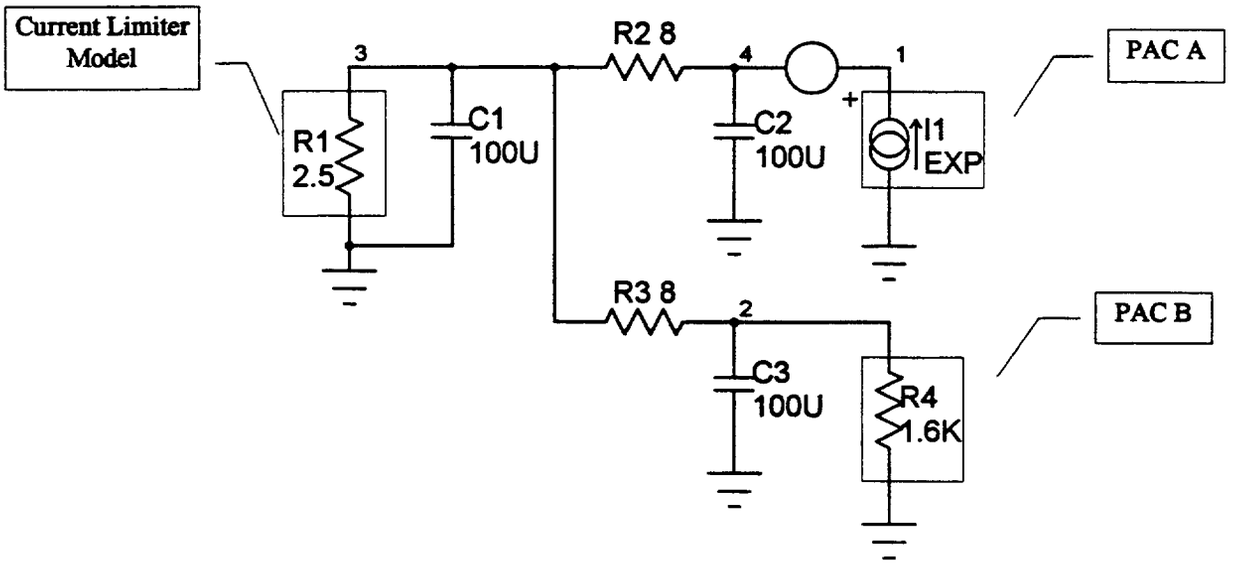

Fig. 9 :Channel separation equivalent circuit.

The SPICE simulation shows that, to obtain a good decoupling between homonym channels (≈ 80 dB), the power supply filtering circuit must be composed of capacitors and resistors of 100 μF and 8 Ω respectively (see figure 10).

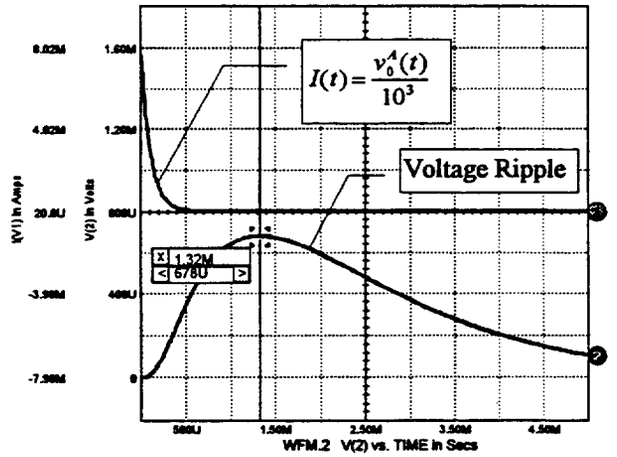

Fig. 10a :Si output adjacent channels simulation.

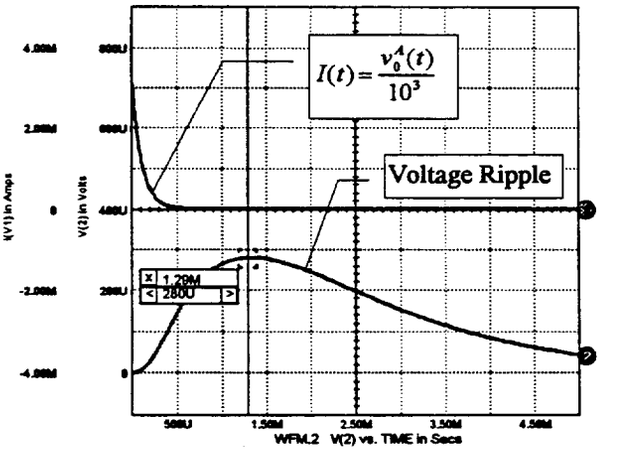

Figura 10b : CsI output adjacent channels simulation.

For Si channels, with $PSRR^- = 0.75 = -2.5$ [dB], by using (9) we have :

$$K_{Si} = 20\log\left[\frac{\hat{V}_1}{\hat{V}_2 \cdot \left(PSRR^-\right)^{-1}}\right] = 20\log\frac{8}{700 \cdot 10^{-6} \cdot 1.33} \approx 78[dB] \qquad (11)$$

For CsI(Tl) channels, with $PSRR^- = 0.56 = -5$ [dB] :

$$K_{CsI} = 20\log\left[\frac{\hat{V}_1}{\hat{V}_2 \cdot (PSRR^-)^{-1}}\right] = 20\log\frac{33}{280\cdot 10^{-6}\cdot 1.77} \approx 76[dB] \tag{12}$$

7. Homonym channels decoupling measurement

By sending a signal to channel A of a M.B. and by measuring the output of the adjacent channel B we have respectively the signals $v_0^A(t)$ and $v_0^B(t)$ both for the Si PAC (figure 11a) and for the CsI PAC (figure 11b).

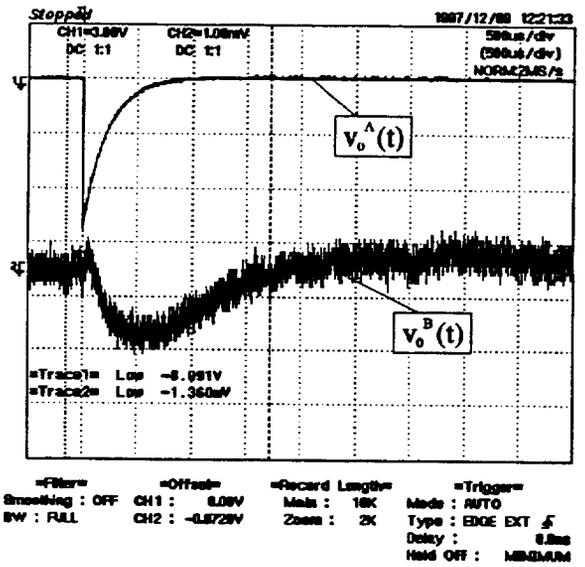

Figure 11a : Si adjacent channels.

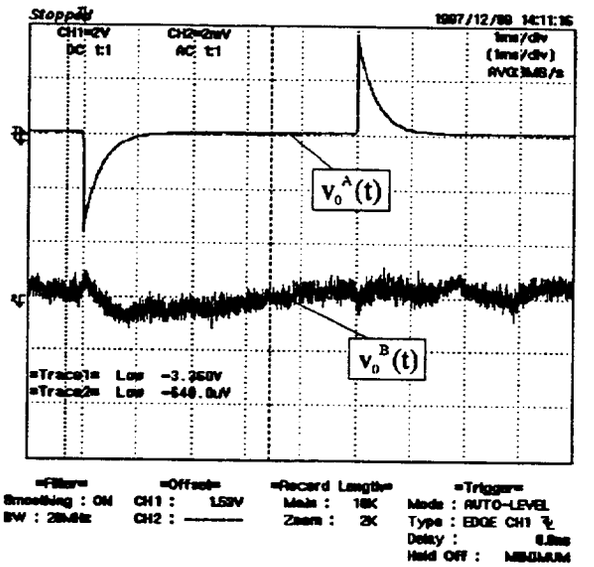

Figure 11b : CsI(Tl) adjacent channels.

By using the maxima in figure 11a and 11b, we obtain (by formula 9) the following values for the constants K_{Si} and K_{CsI} :

	PAC Si detector	PAC CsI(Tl) detector
Channel separation	K_{Si}=76 dB	K_{CsI}=74 dB

Table 3

By comparing the (11) and the (12) with the table 3 we remark that the simulated values of K_{Si} and K_{CsI} are almost equal to the measured values.

8. Minimizing the crosstalk and the input capacitance

The 6 layers structure of the board in figure 12 has been considered the most adequate.

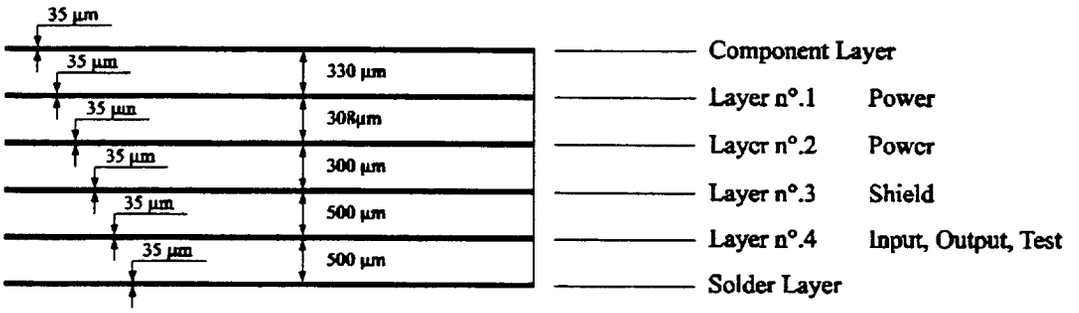

Fig. 12 : Motherboard layers.

As usually, in the regrouping of the lines, we separate the power supply lines and the signal lines. The latter have been housed between two ground planes which assure a good shielding efficiency. The signal lines have a length and follow a path such that these are short and symmetric for homogeneous channels (Si or CsI).

The width (w = 330 µm) and the thickness (t = 35 µm) of the line, the thickness of the dielectric (h=500 µm) and the distance between the two ground planes (b = 2h+t) have been fixed in such a way that, by taking into account the relative dielectric constant of the G-10 fiber glass epoxy board used ($\varepsilon_r = 5.0$), we can obtain a value of the impedance Z_0 near to 50 Ω :

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4b}{0.67\pi w\left(0.8+\frac{t}{w}\right)}\right) \cong 50.55\Omega \qquad (13)$$

In three different layers we have been housed the power supply strips which have been overdimensioned, for the currents requested by the preamplifiers, in order to minimize the line resistance.

The last of the six layers is a ground plane uniformly tinned, so that the heat is transferred by thermal conduction to a radiator, just housed under the M.B., which has an appropriate cooling system.

To reduce the parasitic capacitance and the signal losses, the preamplifiers output and the test input connectors have been allocated very near to the preamplifiers corresponding pins.

We preferred to use single connectors because this choice allows us to avoid tortuous strips paths which could determine loss of symmetry and homogeneity of the lines, causing an increase of the crosstalk and of the noise.

A special housing for each output contribute to improve the shielding of the signals.

Even the paths of the preamplifiers input lines have been conceived in order to keep the maximum symmetry.

The measured contribution of the M.B. input lines capacitance is < 7 pF ; this must be summed to the detectors capacitance (figure 13).

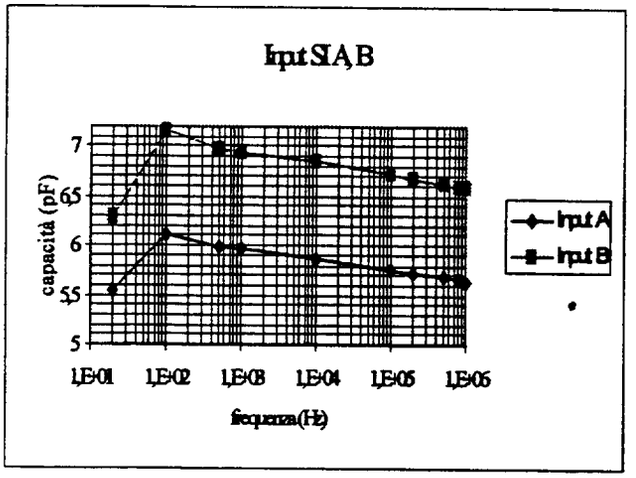

Fig. 13a : Si input lines capacitance.

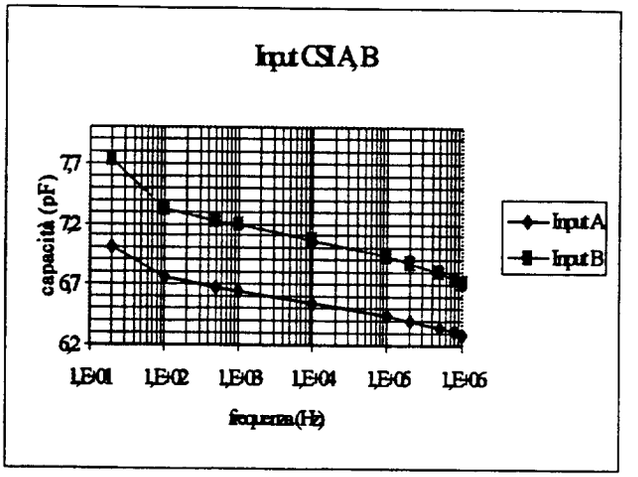

Fig. 13b : CsI(Tl) input lines capacitance.

9. Heat dissipation

The heat dissipation system of the M.B. has been projected according to the preamplifiers characteristics. A large number of ground pins of the PAC has been agreed with the manifactures.

Through the pins, the heat is transferred to the metallic wheels of the multidetector which are submitted to a cooling system.

This matter has been object of a report (*D. Nicotra et al. SIS-Pubblicazioni - INFN/TC 97/27 - 25Settembre 1997*)

10. Conclusions

In an experiment [2] at GANIL laboratory, the first ring of CHIMERA multidetector was coupled with the 4π detector INDRA [3]. This experiment gave the occasion for a proper test under beam of a prototype of 16 M.B.s for the first wheel set up described above.

In this experiment the M.B.s have been supplied for a long time (up to 48 hours) and the gain parameters of the preamplifiers have well confirmed the performance relative to the coupling and noises problems that we have reported, so that no considerable induced signals in adjacent channels have been measured.

The figure 14 shows a typical signal that we have obtained, during the experiment, for Si detectors output.

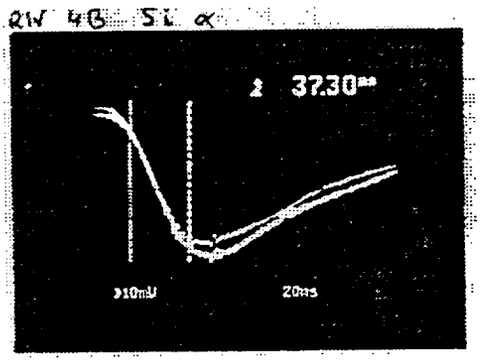

Fig. 14 : Typical Silicon detectors output.

ACKNOWLEDGEMENTS

The authors are very grateful to Santo Reito for his contribution in the design of the first prototype of the M.B. We wish to thank Francesco Librizzi for his technical support and Salvatore Urso for the assistance during the vacuum tests. We would like to tank also Angelo Pagano for fundamental discussion. Finally, the authors are very grateful to Roberto Fonte for his invaluable contribution on the technical approaching of this text.

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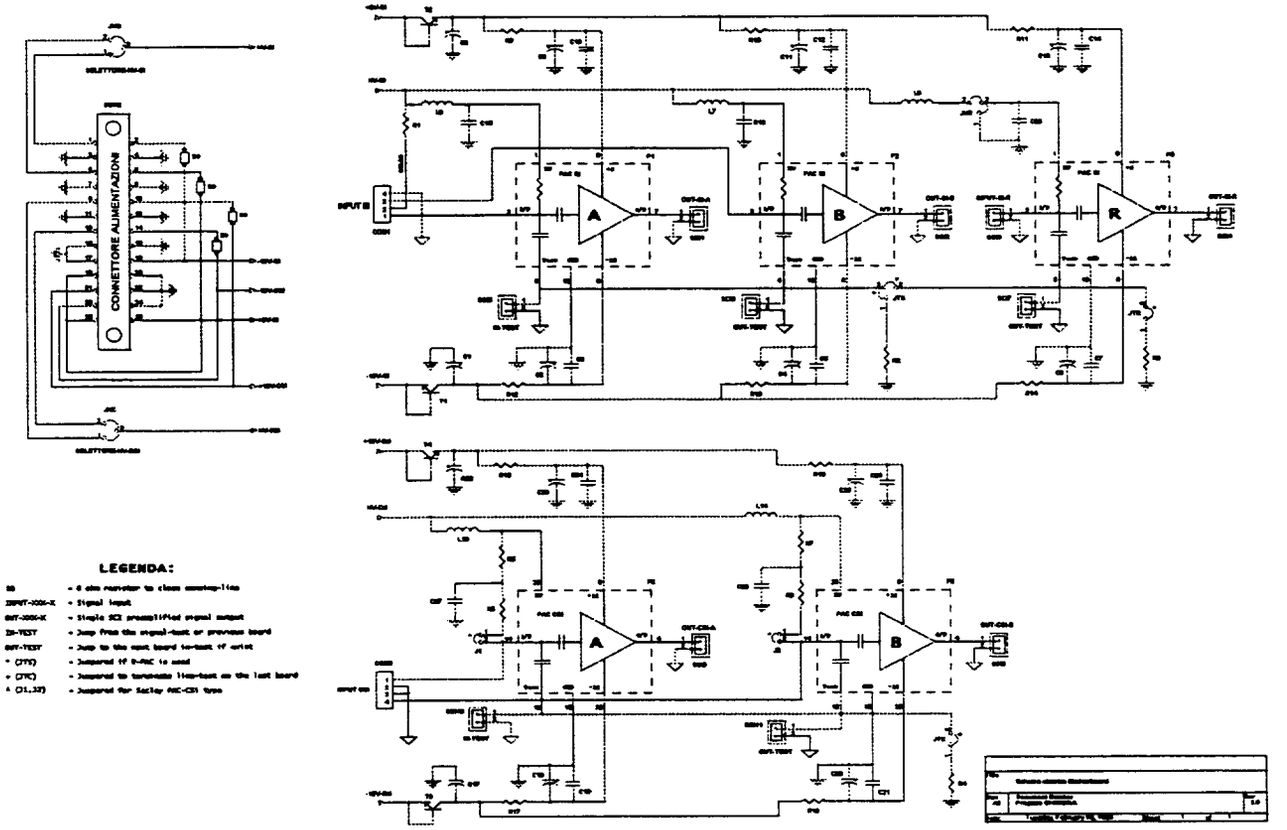

Fig. 15 : Motherboard schematic diagram.

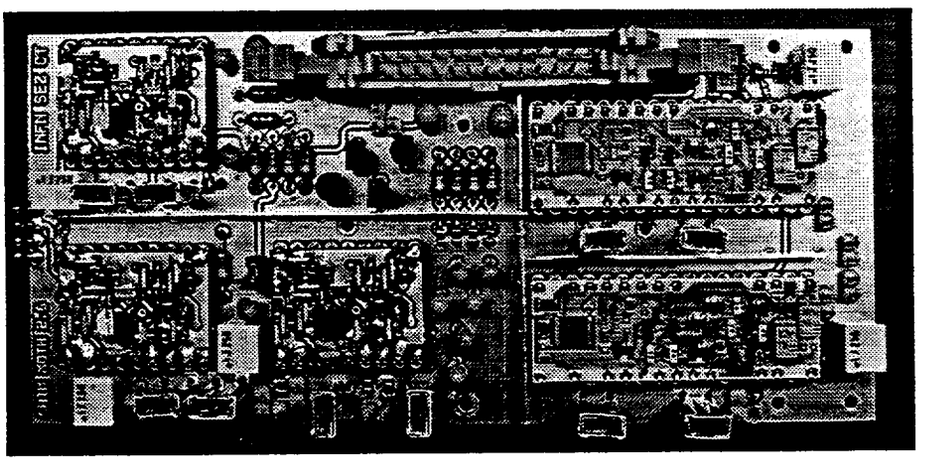

Fig. 16 : The motherboard.

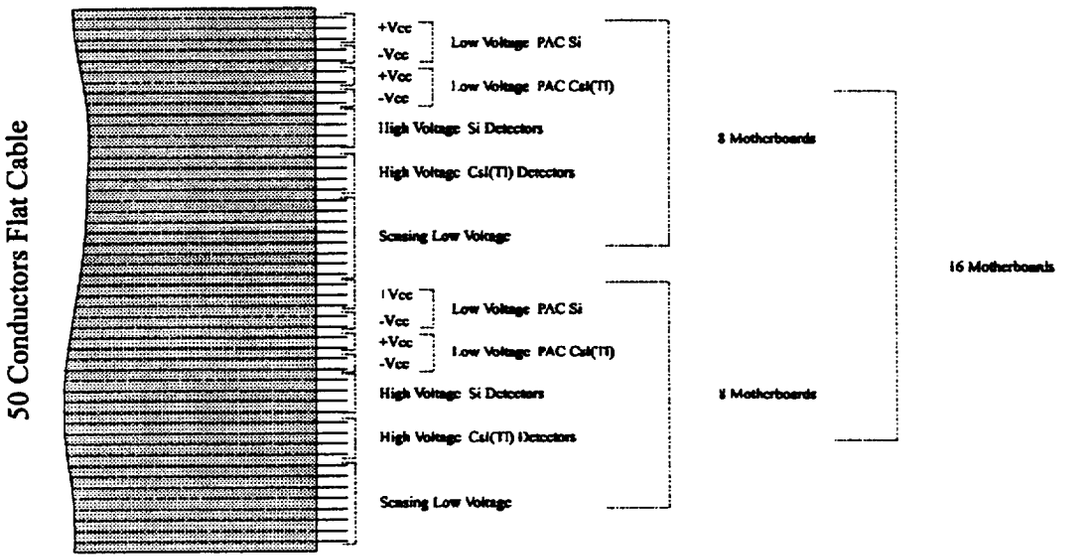

Fig. 17 : Composite bus.

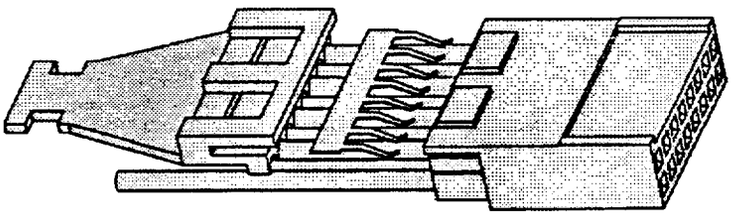

Fig. 18 : Housing design.

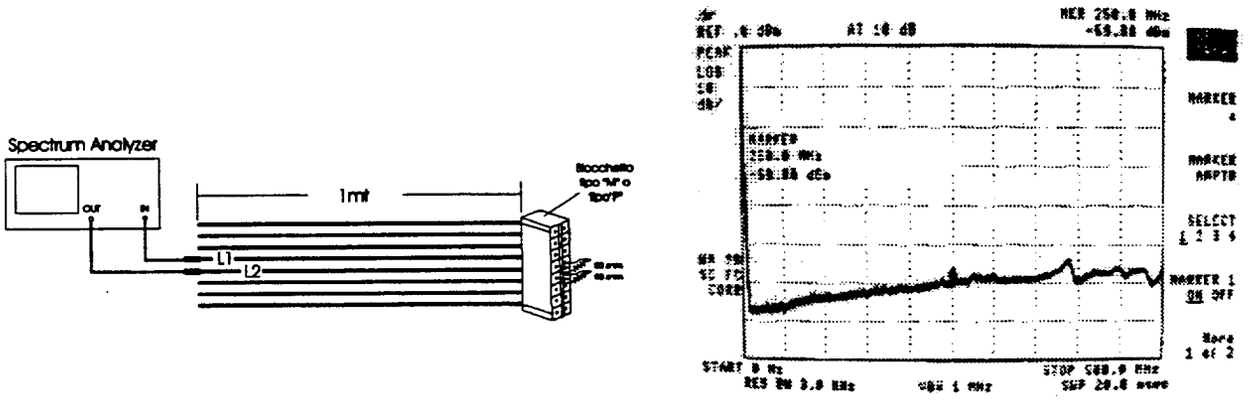

Fig. 19 : Housing test scheme and near-end crosstalk characteristic.

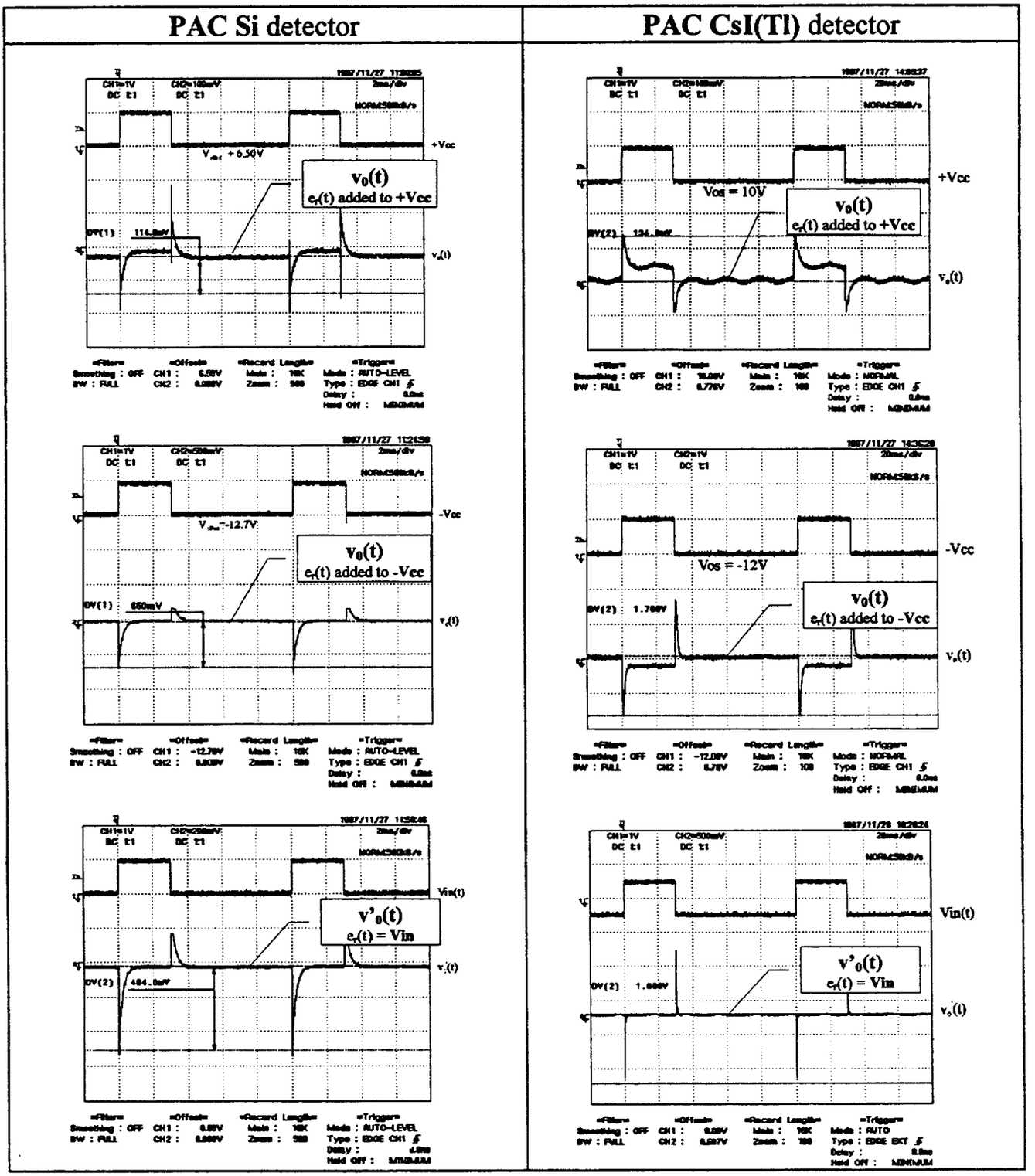

Fig. 20 : Typical output signals.