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RD9 FINAL STATUS REPORT

A Demonstrator Analog Signal Processing Circuit in a Radiation Hard SOI-CMOS Technology

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1 Introduction

The RD9 DRDC project started in 1991 at a time when it was not known whether any commercial radiation hard process would fullfil the design requirements of the complex ASIC chips needed for the LHC experiments with hardening levels of more than 10 Mrad. The primary goals of RD9 were the understanding of the hardening techniques for electronics chips in SOI-CMOS processes and the development of analog demonstrators in the radiation hard 1.2µm SOI-CMOS process HSOI3HD from THOMSON TCS (F). The fact that it was the only available European radiation hardened process at the level of 10Mrad at the time, was the main reason for its selection. In addition, properties of SOI-CMOS processes were considered promising in terms of speed and robustness against Single Event Latch up (SEL) and Single Event Upset (SEU).

The RD9 project was focused on characterisation of samples provided by THOMSON TCS, development of simulation models for analog design, and the design and characterisation of analog demonstrators, such as amplifier, analog memory and ADC. All these goals have been fully reached and have been reported in previous RD9 status reports and at the LERB workshop [1]. The main obstacles we have identified were a lack of uniformity and stability of the HSOI3HD process, due to a too small volume of

production in the TCS wafer fab, and the large series body contact resistance which significantly affects performance of analogue functions. In particular, the MOS transistor in HSOI3HD exhibits a higher noise due to the excess thermal noise of the body contact [2].

We have also learned that the promise of high speed and high density for digital circuits implemented in SOI processes are unfortunately cancelled by the hardening layout design rules used in HSOI3HD. Source and drain regions have a smaller capacitance than in a bulk process, but the gate capacitance is higher, in particular for analogue switches with separate body contacts. This results in inferior speed and device density figures than a bulk CMOS process with comparable gate length. A CRIAD ADC designed in HSOI3HD was 40% larger than the same design done with the 1.5μm "soft" bulk CMOS process from MIETEC N.V.(B).

In view of the limitations of the HSOI3HD process, RD9 started to collaborate with RD29 in 1994 in order to compare the performance of DMILL and HSOI3HD. This work has resulted in the development in 1995 of 2 demonstrators (SCTA and SCTB in the DMILL process) by the RD9 team in collaboration with CEA Saclay, and Cracow. Successful results have been obtained from these chips [3,4].

In 1995, they were rumours that THOMSON would phase out all rad hard SOI processes. This was confirmed at the beginning of 1996: a letter was sent to inform CERN that all their rad hard processes were definitively stopped. At the end of 1996, the decision of the French governement to privatise THOMSON CSF resulted in the closure of the Grenoble TCS site and the wafer fab.

2. The 1995-1996 Milestones

The milestones recommended by the 24th meeting of the DRDC in September 1994 were the following:

1.Finish irradiation tests with the 1993 demonstrator circuits and prove validity of the simulation model.

The 1993 demonstrator circuits, an ICON amplifier and a transimpedance amplifier, have been irradiated up to 10Mrad. Analogue characteristics and noise have been measured before and after irradiation. These results have been presented in the LERB workhop (Lisbon) in 1995, and at the NSREC conference in 1995 and published [1,7]. The validity of the simulation model has been checked for a track-and-hold circuit, and results have also been presented at the LERB workshop [1]. After 10 Mrad, amplifier circuits are fully functional, and noise increases by 40%.

2. Evaluate the performance of the 1994 demonstrator circuits.

This second task has been carried out in 1995. The CRIAD ADC demonstrator has been fabricated, tested and irradiated up 20 Mrad. Experimental results are reported in section 3.3.

3. Evaluate prototype devices in HSOI4-HD (0.8μm) technology

At the end of 1994, we have submitted to THOMSON-TCS a demonstrator in HSOI4-HD. In 1995, TCS decided to phase out HSOI4-HD. Therefore this project was very rapidly stopped. Subsequently, it was decided to collaborate with RD29 on an advanced demonstrator project in using the DMILL process, which is also a 0.8 μm CMOS and bipolar rad hard process. Experimental results of this project are briefly reported in section 4 and have been published [3,4]

3. Report on 1995 and 1996 HSOI3HD studies

The radiation hardness of digital circuits in the HSOI3HD process reaches the expected level of 10 to 20Mrad. The change in static parameters of transistors after 25 Mrad is acceptable and within the parameter spread of the HSOI3HD process. Nevertheless, we have found several problems which limit the use of the HSOI3HD process, in particular for analogue and mixed signal functions.

Despite the high density typical for SOI-CMOS processes which should offer high speed and low power characteristics, we have found that HSOI3HD does not exhibit better performance than bulk CMOS processes with the same feature size. The conservative layout rules applied for radiation hardness together with the additional body contact, significantly decrease the density of circuits. For instance, the gate capacitance is increased by a factor 2. Therefore, the power consumption of a CRIAD-ADC demonstrator chip was found to be significantly higher than the corresponding version fabricated in a commercial bulk 1.5μm CMOS process.

Another severe limiting factor to the use of HSOI3HD for analog functions comes from the body contact effect. This is a common problem of medium thickness film (150nm) and thin film (80nm) SOI processes. The body effect is caused by a dynamic, and in some case also by a static inefficiency of the body contact. The most severe effects we have studied are an unstable and unpredictable charge injection from analog switches in mixed signal circuits, and an additional noise component in amplifier circuits .

Although the lot-to-lot reproducibility of the radiation hardness was in general acceptable, we have nevertheless noticed sometimes large differences in the radiation response of transistors coming from different fabrication lots. We explained this by the very low volume production in TCS wafer fab, and by the variation of characteristics of SIMOX wafers.

3.1. Device characterisation

The measurement of ionization effects on NMOS and PMOS devices in the HSOI3HD process when irradiated by a Co-60 source has been performed for devices implemented on different types of SIMOX SOI substrate. V_T shift, weak inversion slope, back channel threshold, mobility, annealing effect and leakage current for several fabrication lots have been extracted. As an exemple, Fig.1a-d shows variations of Vt shift and mobility of p-

channel and n-channel devices as a function of the total dose for 6 different lots fabricated between 1991 and 1995. Lots 100 and 90 have a totally different radiation response.

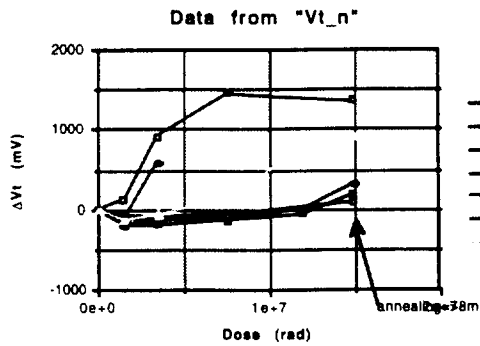

Figure 1a

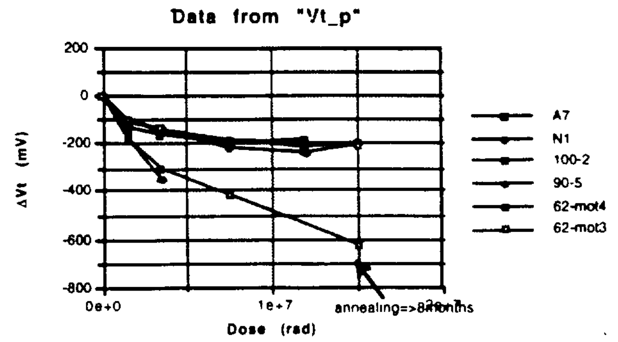

Figure 1b

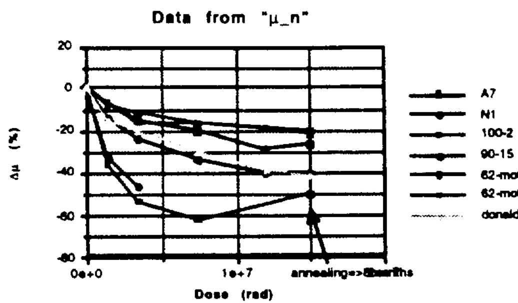

Figure1 c

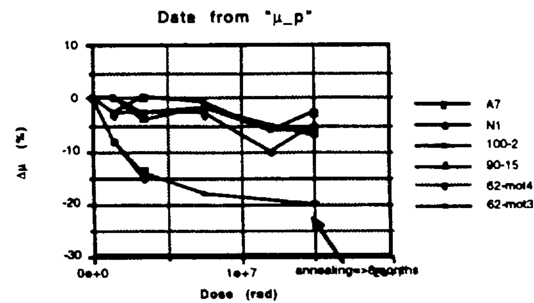

Figure1 d

3.2. Noise characterisation

MOS transistors usually exhibit 2 noise components: 1/f noise caused by random trapping of carriers in traps located at the interface or within gate oxide, and white noise caused by thermal motion of carriers in the channel. Complete results on 1/f noise and white noise of the HSOI3HD up to 25 Mrad are reported in references [5,6]. In addition, transistors in HSOI3HD have a third noise source. A detailed study including the design and integration of dedicated test structures has led to the conclusion that this additional component originates from the body resistance. This resistance is high and bias dependent. The result of this study has been presented at the 1996 SOI conference [2].

3.3. HADC11 demonstrator

The CRIAD ADC, the block diagram of which is shown in fig.2, was originally designed in a commercial soft bulk CMOS, but has now been redesigned in HSOI3HD.

Pre-irradiation results

The functionality of the HSOI3HD version was satisfactory, although the timing sensitivity of the track-and-hold was higher than expected. As a consequence, the best

results were obtained with a synchronisation of the clock between track-and-hold and comparators different from the simulation. In those conditions, the maximum sampling rate was 16 Mhz, but above 8 Mhz the LSB precision of 1 mV is not kept. This is shown in Fig.3 which depicts the digitization of a 20Khz sinus wave of 64 mV amplitude at different ADC sampling frequencies. Simulations predicted a maximum data conversion speed of 20 Mhz. The yield evaluated on few samples, 20, was 70% for a circuit area of 15 mm^2.

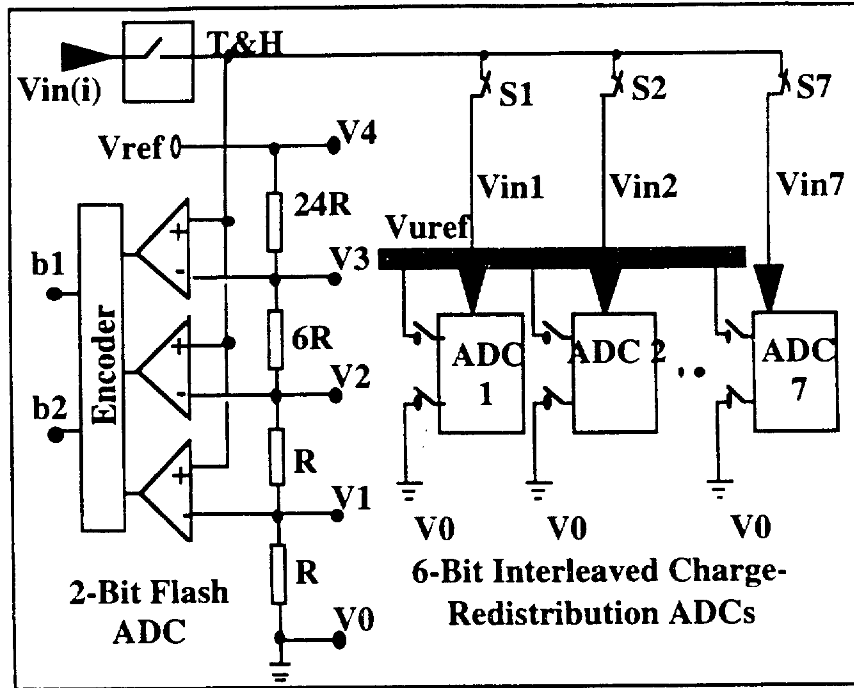

Figure 2. CRIAD ADC Block Diagram

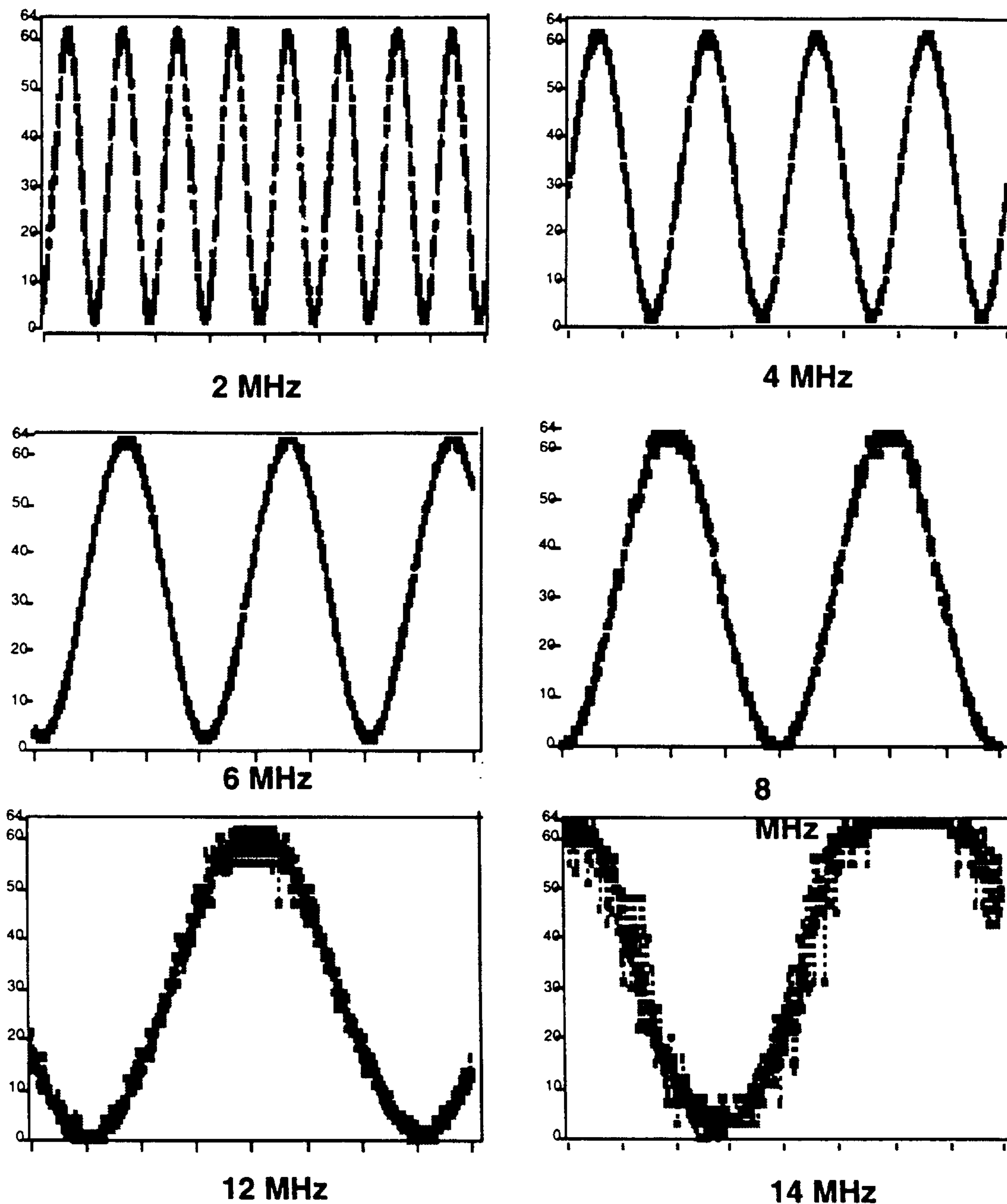

Figure 3. Digitization of a 64 mV 20Khz sine wave at different sampling frequencies

The total power consumption of the chip has been separately measured for the analog and digital blocks, and the resistor network of the 2bit flash ADC, and the result is given in Fig.4. The resistor network is made up of 32 equal elements for a total of 480Ω. The power supplies voltages were different for analog and digital circuits, being ±3V for the analog and ±2.5V for the digital. For 8Mhz conversion rate, the power consumption of the HSOI3HD ADC-CRIAD version is about 40% higher that the version in a "soft" commercial bulk CMOS. The increase of power is mainly due to the additional parasitic gate capacitance in HSOI3HD.

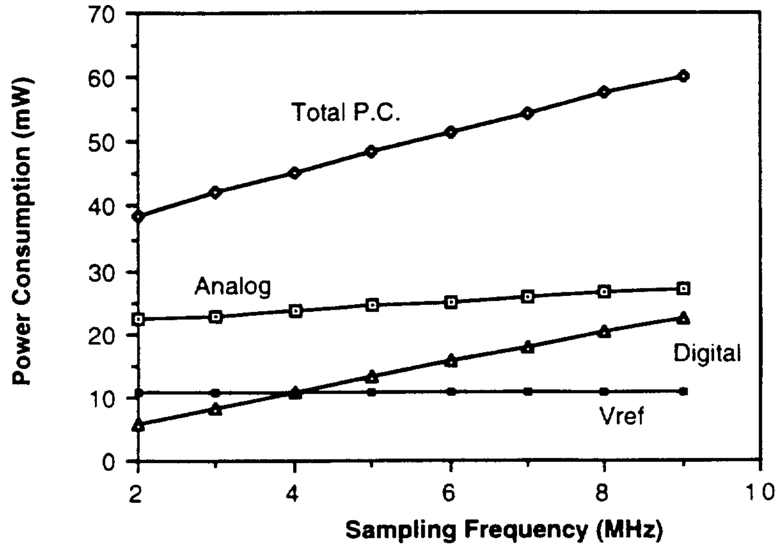

Figure 4. Power consumption of CRIAD ADC in HSOI3HD

The linearity measurement indicates a precision of 1mV as expected for the first range of 64mV, for conversion frequencies less than 8Mhz. The differential non-linearity is 0.2 LSB in each conversion range, and the integral non-linearity is 0.37 LSB in the first range and 0.15 LSB in the 3 others.All these results were similarly measured on circuits coming from the same production but using 2 different SIMOX wafers: simple and double implanted. This was done to study the impact of the buried oxide implant technique on the performance of VLSI circuits. No significant difference was observed between circuits fabricated with these 2 different substrates.

Results after irradiation, 10Mrad – 20Mrad

After irradiation, several problems in the ADC operation appeared.The range conversion (2 MSB bits) performed by the flash ADC stage does not work, as shown in Fig.5a for the full dynamic range. The failure is probably due to a very high input voltage offset of the comparators of the 2-bit flash ADC. By forcing the conversion in the largest range, as shown in Fig 5.b-e, it is possible to study the performance of the 7 interleaved ADC stages. Even in this case, the offset of the comparator is so high that the resolution becomes very poor. Other parasitic effects occured, such as the presence of a pattern in the digitized output code which indicates a non-uniformity of the offset through the 7 interleaved ADC stages. Large charge injection in analog switches in the comparator is assumed to be the origin of the failure. This also causes the failure of the offset correction circuit embedded in comparator stages.

After irradiation to a total dose of 10Mrad, the total power consumption increased only by about 20%.

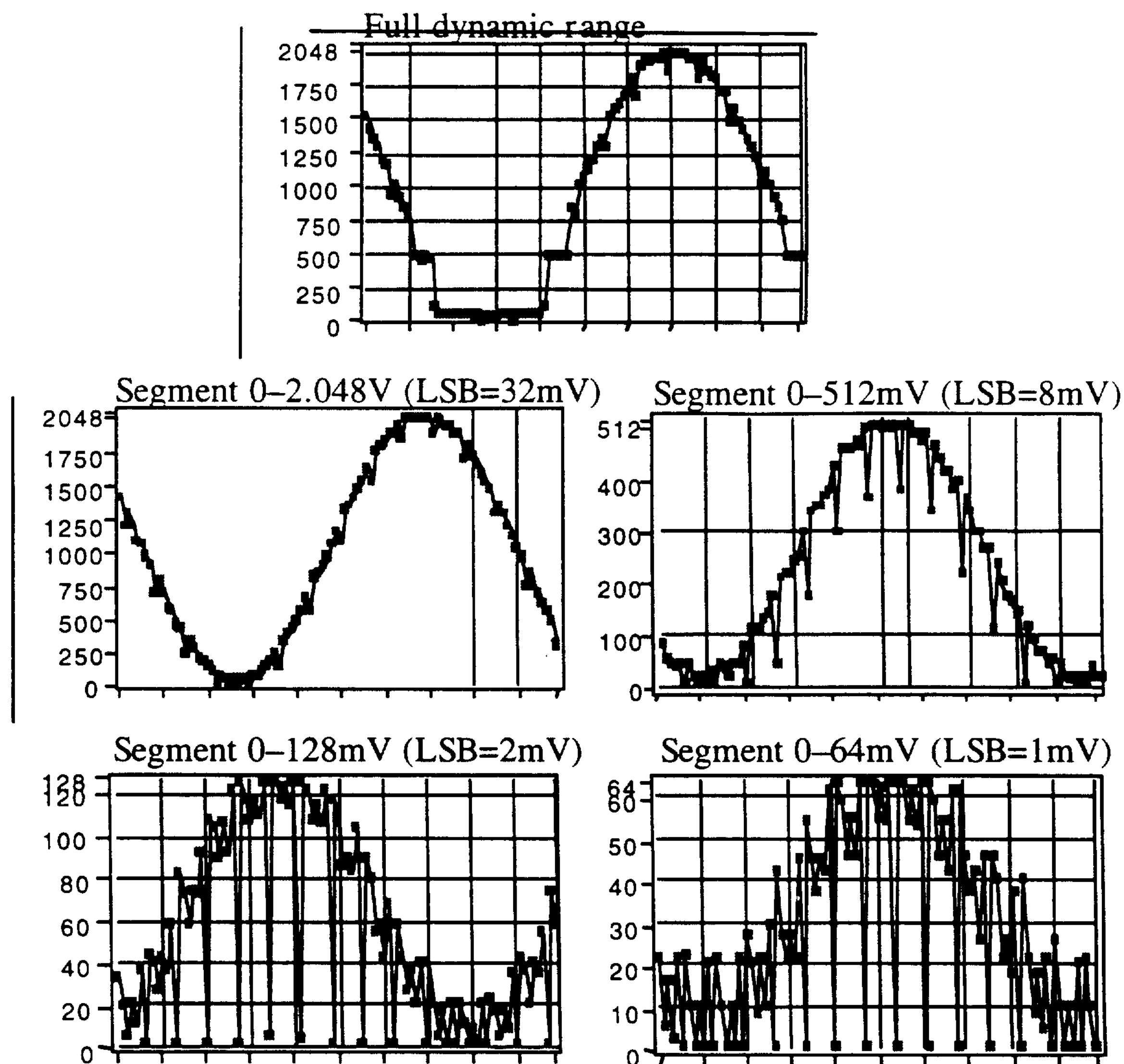

Figure 5. CRIAD ADC performance after irradiation

4. Report on last year's DMILL development

The technical issues of HSOI3HD related to body effects, and the rumours of the possible stopping of rad hard processes at THOMSON TCS lead us to dedicate a significant effort in the evaluation of the DMILL process. RD9 in collaboration with RD29, CEA Saclay DAPNIA and the Faculty of Physics and Nuclear Techniques of Cracow/PL has pursued in 1995 and 1996 the development of BiCMOS front-end electronics demonstrators in the 0.8µm BiCMOS DMILL radiation hardened process.

Two prototype chips, SCTA and SCTB, respectively for the analogue and binary readout of silicon strip detectors in the ATLAS Semiconductor Tracker (SCT) have been designed and manufactured in 32 channel versions using the DMILL process.

The SCTA chip [4] comprises three basic blocks: front-end amplifier, analogue pipeline and output multiplexer. The front-end circuit is a fast transresistance amplifier followed by an integrator, providing fast shaping with a peaking time of 25 ns, and an output buffer. The front end output values are sampled at 40 MHz rate and stored in a 112-cell deep analogue pipeline. The delay between the write pointer and trigger pointer is tunable between 2 μs and 2.5 μs. The chip has been tested successfully and subsequently irradiated up to 10 Mrad. Full functionality of all blocks of the chip has been achieved at a clock frequency of 40 MHz both before and after irradiation. Noise figures of ENC = 720 e^- + 33 e^-/pF before irradiation and 840 e^- + 33 e^-/pF after irradiation have been obtained.

The SCTB chip [3], comprises three basic blocks: front-end amplifier, discriminator and a binary pipeline. The preamplifier and shaper implemented in this architecture use the same concept as used for the front-end in the analogue architecture. The shaper is followed by a discriminator providing only 1 bit yes/no information which is stored in a binary pipeline based on a dynamic FIFO digital circuit in order to achieve low power and high density. The chip has been irradiated by a Co-60 source up to 10Mrad under nominal static bias. After irradiation, the SCTB chip is fully functional and performance is maintained. The power consumption increased from 200μW to 360μW/channel for a clocking frequency of 40Mhz.

5 Conclusion

After these 4 years of RD9 study, we have learned that HSOI3HD is a good process for digital circuits, but has severe limitations for analog and mixed-signal circuits. After irradiation, analog performance of amplifiers was poor and complex circuits did not work anymore (ADC). We have understood this issue 2 years ago, and we therefore turned our efforts towards the DMILL process. This has resulted in demonstrator circuits, SCTA and SCTB, those results have convinced HEP community that rad hard circuits can be built that meet the requirements of LHC experiments. These two circuits are now seriously considered by ATLAS for the readout of the silicon tracker.

References

[1] P.Aspell et al., Study of a radiation hard SOI-CMOS technology for mixed analog-digital IC design for applications in LHC, First Workshop on Electronics for LHC Experiments. Proceedings of the LERB meeting, Lisboa Sept. 1995, CERN/LHCC/95-p.56

[2] F. Faccio et al., An additional contribution in the noise spectrum of SOI MOSFETs, presented at the 1996 SOI conference, Fort Meyers Fl, USA (Oct. 1996).

[3] F. Anghinolfi et al., Development of front-end electronics for LHC experiments, Ballaton, Hungary (Sept. 1996), CERN/LHCC/96-39.

[4] F. Anghinolfi, et al., SCTA - A Rad-Hard BiCMOS Analogue Readout ASIC for the ATLAS Semiconductor Tracker, presented at IEEE Nucl. Sc. Symp, Anaheim (Nov.1996).

[5] F. Faccio et al., Noise Characterization of Transistors in a 1.2 μm CMOS-SOI Technology up to a Total-Dose of 12 Mrad (Si), presented at IEEE NSREC Symposium 1994.

[6] F. Faccio et al., Analog Performance of SOI MOSFETs up to 25 Mrad (Si), Proc. RADECS' 95 Conference, F (Sept. 1995).

[7] P. Aspell et al., A fast, low power CMOS amplifier on SOI for sensor applications in a radiation environment of up to 20 Mrad(Si), IEEE Trans. NS vol 42, p.636.

Appendices

Papers published in 1994, 1995 and 1996.

Study of a radiation hard SOI-CMOS technology for mixed analog-digital IC design for applications in LHC

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ABSTRACT. The HSOI-3HD CMOS on SOI technology has been studied in order to assess its suitability for use as a radiation hard VLSI process in LHC detector frontend electronics. In particular the study has concentrated on the analog characteristics of transistors and the design and measurement of a number of demonstrator circuits.The transistor measurements have shown threshold shifts of 250mV and -350mV for n and p channel respectively. The noise study has shown that in addition to the white noise and 1/f noise sources, a third generation recombination (G-R) noise source is apparent. This G-R component appears as a hump in the noise spectra and can be moved in frequency by varying the body-source (Vbs) potential of the device. A |Vbs| of 1.3V is sufficient to move this component out of the frequency range of interest for LHC and hence make it negligible. Two amplifiers, namely a grounded gate amplifier and a low noise transimpedance amplifier, and also a track and hold circuit have been designed and fully measured. The results show full operation after doses up to 20Mrad(Si) with little degradation with respect to gain and speed. There is however a significant deterioration in the noise behaviour.

1. INTRODUCTION

Complex ICs for signal processing in experiments at the LHC will sit in a high radiation environment. Radiation hardness for total dose up to a level of 10 to 30 Mrad and for single event phenomena is required. Silicon on Insulator (SOI) technologies are immune from Single Event Latchup (SEL) and have a higher threshold than bulk technologies for Single Event Upset (SEU), therefore they are good candidates for applications in the LHC environment.
The only commercially radiation hard process on SOI available in Europe is the HSOI3-HD, a 1.2 μm polycide gate CMOS technology manufactured by Thomson TCS (St. Egrève, France) on a SIMOX substrate. It is optimised for high total dose for digital circuits. We have investigated the analog performance of this process and its potential for LHC applications.

2. ANALOG CHARACTERIZATION OF THE TRANSISTORS

A series of test transistors of different size and geometry and coming from several processing batches has been measured. The full characterization involved extraction of the static parameters (threshold voltage, mobility, transconductance, leakage current) and study of the noise. Irradiation has been performed at several total dose levels, up to a maximum of 25 Mrad (Si). A constant bias with a current density of 0.2 μA/μm has been kept during both irradiation and room temperature annealing.
The threshold voltage shift as a function of total dose is depicted in figs. 1 and 2 for n- and p-channel transistors. Relative contributions of interface states and oxide trapped charge are shown. The prerad threshold voltage for p-channel transistors is about -1.3 V, whilst it is 900 mV for the n-channel. This values were extracted with the back interface in accumulation. Room temperature annealing under bias does not have a major importance in the threshold evlution. The threshold voltage shift after 25 Mrad is of the order of 250 mV for n-channel and -360 mV for p-channel transistors. For the p-channel this can impose to use a power supply of at least 3.5V. Threshold voltage shift is reasonably predictible at any total dose and therefore circuit performance after irradiation

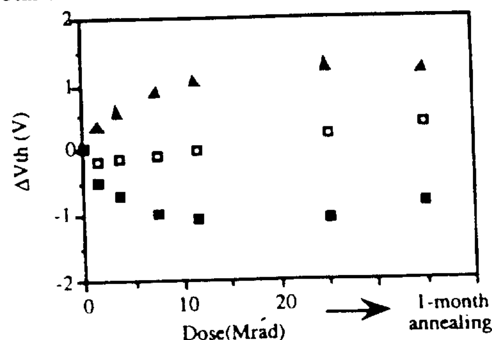


Figure1: Threshold voltage shift for n-channel transistors. Empty squares represent the overall shift, which is due to the contributions of trapped oxide charge (black squares) and interface states (black triangles).

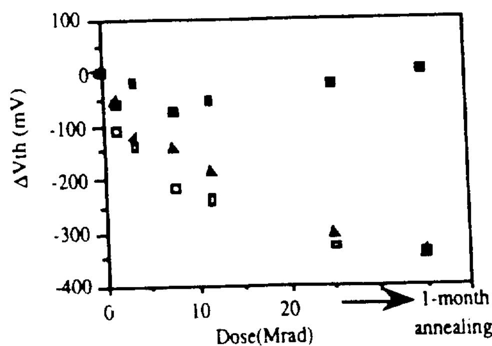


Figure 2: Threshold voltage shift for p-channel transistors. Empty squares represent the overall shift, which is due to the contributions of trapped oxide charge (black squares) and interface states (black triangles).

can be estimated in the design phase.
Transconductance in saturation decreases respectively of about 44% and 18% for n- and p-channel transistors. In

every case the drain leakage current stays below a few tens of pA.

The spectral power density of the equivalent input noise voltage of NMOS and PMOS transistors has been measured before and after ^{60}Co irradiation. Measurements were performed in strong inversion and in saturation, with a constant current density of 0.5 $\mu A/\mu m$. The noise spectrum is composed of three different sources: white noise, 1/f or flicker noise and generation–recombination (G-R) noise. This G-R noise is visible as a hump in the noise spectra only under particular bias conditions, and can be moved widely in frequency by acting on the body or backgate bias.

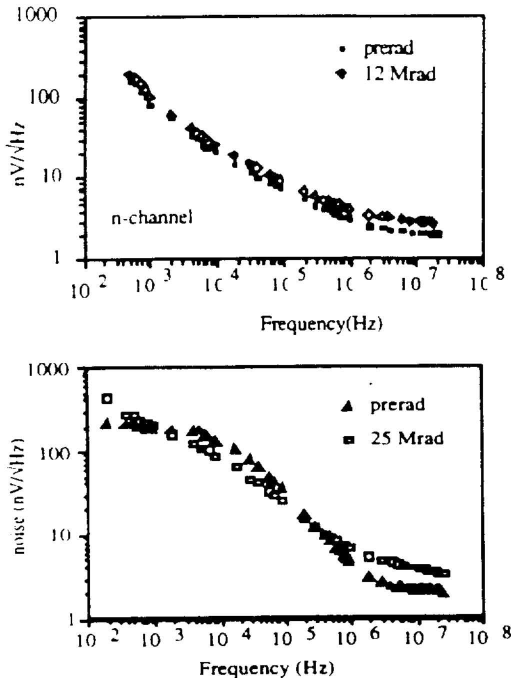


Figure 3: Noise spectra of n-channel transistors from lots 1 (upper picture) and 2 before and after 12 and 25Mrad and annealing. In the spectra shown for lot 1, the applied body bias could move the G–R hump under the 1/f noise. This was not the case for lot 2, due to a different backgate threshold voltage.

The p-channel transistors, which are buried channel devices, have lower 1/f noise. The parameter K_f characterizes the 1/f noise and increases from $1.37 \cdot 10^{-9}$ to $6.9 \cdot 10^{-9}$ $fC^2/\mu m^2$ for PMOS transistors after a 25 Mrad irradiation. Therefore, in the measurement conditions for W/L=1000/1.4, the corner noise frequency Fc (defined for equal 1/f and white noise contributions) stays below 200 Khz even after irradiation.

Figs. 3 and 4 show the noise spectra before and after 12 and 25Mrad for transistors coming from 2 different fabrication lots. The G-R noise contribution is still visible in some of the depicted spectra. Owing to the particular layout of the test structures (common terminals for the n-channel and p-channel transistors), we could not apply a sufficiently high body bias to move this contribution further in the low

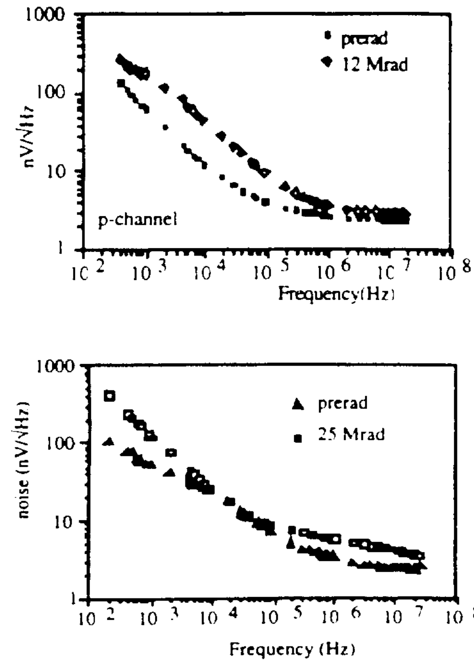


Figure 4: Noise spectra of p-channel transistors from lots 1 (upper picture) and 2 before and after 12 and 25Mrad. Even after 12 Mrad, the noise in the 10–20 MHz region increased significantly more for lot 2.

frequency region in all cases. The backgate threshold voltage determined whether the applied bias was sufficient to make the G–R hump disappear under the dominant 1/f noise. Transistors from lot 2 had higher noise after irradiation. For the n-channel white noise, this was determined by a sharper decrease in transconductance. For p-

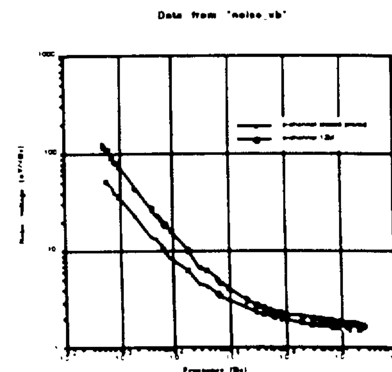


Figure 5: Noise spectra of p-channel transistors from lot 3. Noise at 10 Mhz is 1.65 nV/√Hz before irradiation and 1.76 nV/√Hz after 12Mrad

channel transistors from the same lot it was difficult to clearly identify the white noise after irradiation, but the noise increase in the 10-20 MHz region was much higher than for lot 1.

Noise results of figs. 5 and 6 were obtained from transistors of W/L=2000/1.4 coming from a third fabrication lot. These test transistors were differently layed out to allow more freedom in the bias and to study eventual parasitic effects from the edges. The measurements were performed

with I_d=1mA to keep the same current density in the channel as for lots 1 and 2. Voltage spectral density (Sv) in the white noise region and 1/f corner noise frequency (Fc) of these 3 different lots are summarised in table 1 before and after irradiation and annealing.

We have observed a variation of the radiation hardness

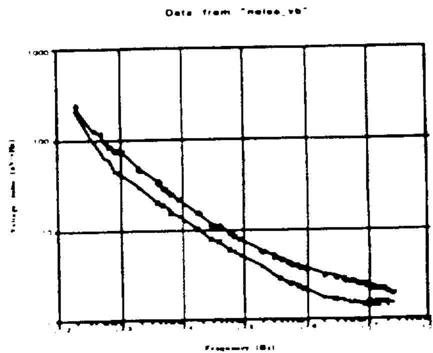


Figure 6: Noise spectra of n-channel transistors from lot 3. Noise at 10 Mhz is 1.51 nV/√Hz before irradiation and 2.1 nV/√Hz after 12Mrad.

between transistors coming from different fabrication lots. In particular, lot 2 shows higher noise and lower transconductance after irradiation.

Table 1. Voltage spectral density in the white noise region and 1/f corner noise frequency values for transistors coming from the three different production lots. These results refer to transistors with W/L=1000/1.4 biased at Id=500μA for lot 1 and 2 and W/L=2000/1.4biased at Id=1mA for lot 3. Sv is in nV/√Hz and Fc in KHz

LOT	Sv prerad	Sv 12Mrad	Sv 25Mrad	Fc prerad	Fc 12Mrad	Fc 25Mard
lot 1 n	1.98	2.73	-------	1000	800	-------
lot 1 p	2.16	2.5	-------	132	179	-------
lot 2 n	2.16	3.10	3.19	1260	1760	1520
lot 2 p	2.25	3.14	3.29	69	143	202
lot 3 n	1.51	2.1	-------	995	2840	-------
lot 3 p	1.65	1.76	-------	71	89	-------

3. GROUNDED GATE CURRENT AMPLIFIER

The design of the grounded gate amplifier is shown in Fig.7. It consists of the grounded gate input MOSFET MN1, the cascode stage MN2 and the current sources MP3, MP4 and MN5. The output node Vo acts as an integrating node of capacitance Co. The slow speed error amplifier (Ae) ensures a stable DC potential of the output node and defines a discharge time constant of Co through the controlled current source MN6.

The technique also provides self adjustment for the effect of the sensor dark current which becomes significant as the total dose accumulates. Detector leakage currents of up to 20mA can be compensated for, enabling a DC connection to the sensor. This, in turn reduces the processing cost of the detector.

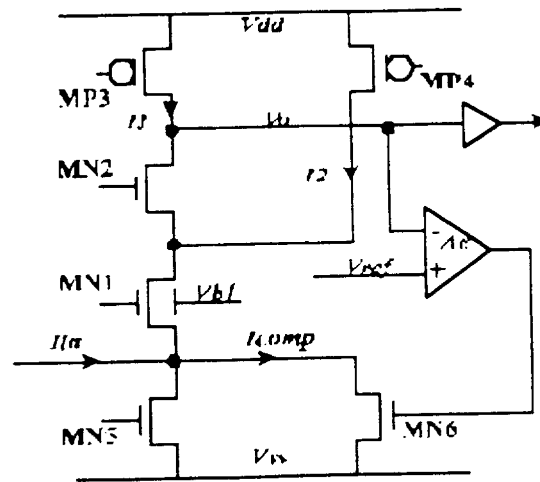


Figure 7 Grounded gate amplifier as implemented in HSOI3HD

The chip consists of 12 channels each with vertical pitch of 100mm and length 800mm. Including the pads the total surface area is 7.9mm2.

A total of 10 chips were irradiated, five at 10 Mrad and five at 20 Mrad using a 60Co source. The exposure was over a 76 hour period giving dose rates of 133 Krad/hour and 266 Krad/hour.

The noise slope before and after irradiation has been measured. The prerad. result is 78e⁻/pF (rms) which corresponds to approximately 2nV /$Hz^{1/2}$. After 10 Mrad there is an increase in the parallel noise of approximately 23% whilst the series noise increases by nearly 60%. The degradation thereafter is small and only apparent in the parallel noise, increasing by a further 9%. The majority of the radiation effects is apparent within the first 10 Mrad with only a small change thereafter. Satisfactory operation at higher levels of total dose would therefore seem probable but further study would be needed to confirm this.

4. LOW NOISE TRANSIMPEDANCE PREAMPLIFIER

A transimpedance amplifier using a fast active feedback loop presented elswere [5] in a commercial 0.7μm bulk CMOS technology[1] has been designed and fabricated in HSOI3HD. This amplifier has been sized for a detector capacitance of 10 to 20pF.

Fig.8 shows the circuit diagram. T1 and T2 forms the amplifier stage with the load MPL. Transistor MPf The input device the p-channel T1 has an aspect ratio W/L=2000/1.4. The sizing of all transistors is very similar to the MIETEC design, except minor modifications due to different parasitic capacitances and body connection of the SOI technology. After 10 Mrad, pulse shape does not change indicating no further radiation damage between 3 to 10 Mrad. The noise result is different, the noise increase continue from 3 to 10 Mrad. These preliminary experimental results are obtained without annealing and must be confirmed after few weeks of annealing time.

[1] MIETEC NV, Oudenaarde Belgium.

Fig.9 shows the output pulse waveform of the SOI active feedback transimpedance amplifier prerad, after 3 Mrad and 10 Mrad for a feedback current of 40nA and an input capacitor Cin=10pF. After 3 Mrad the gain decrease is 15%, but the peaking time of 80ns does not change.

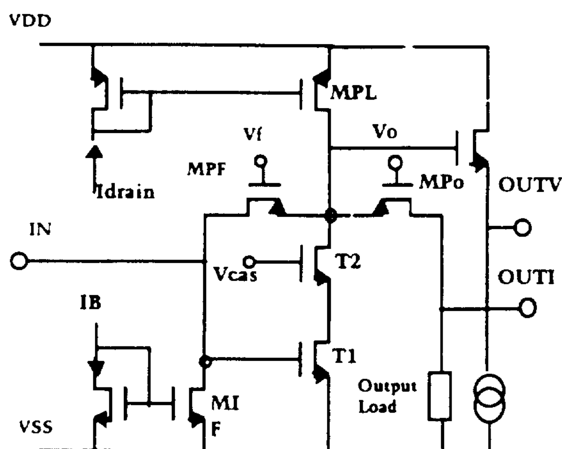


Figure 8 Circuit diagram of the active feedback transimpedance implemented in HSOI3HD process.

Fig 10 shows the noise characteristic ENC=f(Cin) of the active feedback preamplifier fabricated in 0.7µm CMOS bulk process and in HSOI3HD. The fit to the has been obtained by applying a least mean square on the expression,

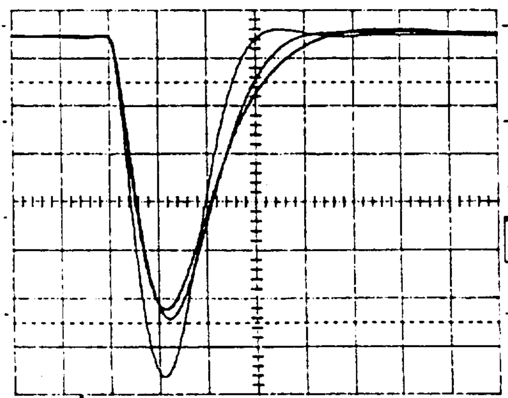


Figure 9 Output pulse waveform of the active feedback transimpedance for prerad (larger pulse height), 3Mrad and 10 Mrad. Input charge is 4fC,time axis is 100ns/div and y-axis is 10mV/div.

$$ENC = \left[\frac{\left(3.03 10^4 e_n^2 C_{in}^2\right)}{\tau_{ro} + \kappa C_{in}} + 2.76 10^4 i_n^2 \left(\tau_{ro} + \kappa C_{in}\right) \right]^{1/2} \quad (2)$$

where ENC is the equivalent noise charge in electrons rms, e_n is the equivalent series noise voltage in nV/√Hz, i_n is the equivalent parallel noise current in pA/√Hz, Cin the input capacitance in pF, τ_{r0} is the rise time 10%-90% in ns for Cin=0, κ the rise time dependence with the input capacitance in ns/pF. This technique of calculation takes into account the peaking time variation for the different input capacitors Cin.

Noise measurement indicates a larger noise for the SOI process. It must be noted that the input transistor is an n-

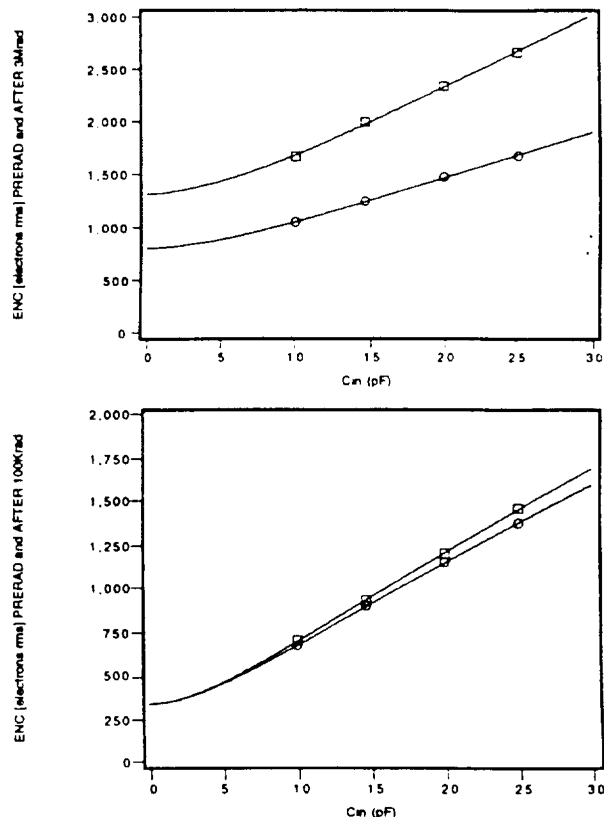


Figure 10 Noise measurement ENC=f(Cdet) of the active feedback transimpedance amplifier for a peaking time of 45ns and a bias current of 500µA in the HSOI3HD process(top graph) and in CMOS bulk submicron process(bottom graph). Bottom curves are prerad, top curves are after 3Mrad for HSOI3HD and 100Krad for 0.7µm CMOSprocess.

channel. A p-channel version will be submitted for fabrication end of 1995 and will exhibit a better noise figure before and after irradiation. The noise parameters extracted from the fit calculation are shown in table 2.

Table 2 Evolution of the preamplifier noise with radiation in HSOI3HD and MIETEC CMOS 0.7µm processes. e_n [nV/√Hz] and i_n [pA/√Hz] are respectively the equivalent series noise voltage and parallel noise current referred to the input and extracted with eq (2).

CMOS processes	e_n	i_n	τ_{r0}	κ
Bulk 0.7µm prerad	1.93	0.37	30	0.4
Bulk 0.7µm 100 Krad	2.31	0.33	40	0.45
HSOI3HD pre-rad	2.64	0.67	48	0.7
HSOI3HD 3 Mrad	4.5	1.01	60	0.7

After 3 Mrad the series noise voltage increase is 70 % which is close to what has been observed with a single n-channel device. In addition, there is an increase of the parallel noise of 50% which is not presently explained.

This effect is not observed on the bulk submicron CMOS process for which series and parallel noise are stable after 100Krad. These experimental results indicate also that the soft submicron CMOS process tested exhibits a better noise figure than HSOI3HD technology.

5.FAST TRACK-AND-HOLD

This circuit was designed to be used in the 11-bit CRIAD Analog-to-Digital converter. Its objective was a good tradeoff speed-to-accuracy. The circuit diagram is shown in fig.11. It comprises a Track-and-Hold switch ($S_{t\&h}$) and a p-channel differential OTA with Miller compensation. The capacitance at each node of $S_{t\&h}$ is equal, thus the charge injection is assumed to be symmetrical at both ends of the switch. This injection is reduced by two dummy switches half the size of $S_{t\&h}$ integrated symmetrically.

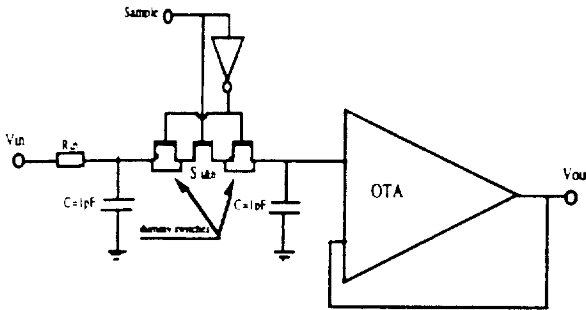


Figure11 : circuit diagram of the fast track–amd–hold implemented in the HSOI3HD technology.

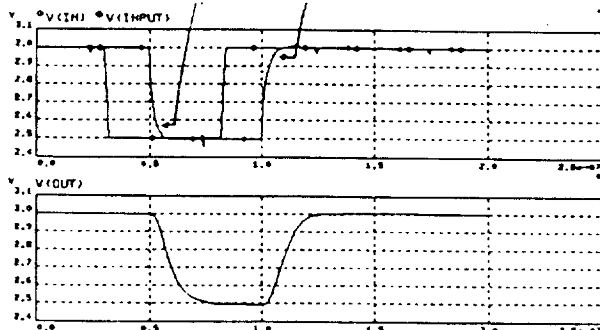


Figure 13 : Results from the ELDO simulation of the T&H circuit. The upper picture shows the signal at the input and at the T&H node, whilst the lower one shows the output of the circuit charged with a 10 pF load.

The circuit has been fabricated and tested, and showed a rise time of 17.5 ns and a gain of 0.94, with a power consumption of 12.5 mW. The measurements were in good agreement with the simulation performed with the specially developed SOI model implemented in ELDO. Simulation results are shown in Fig.13.

The high power consumption was caused by an excessively high threshold voltage of the p-channel transistors for the processing lot in which the circuit was implemented. We had therefore to increase Vdd to keep all the transistors in saturation during operation. Another consequence of this problem was a relatively high charge injection at the T&H node, especially after irradiation.

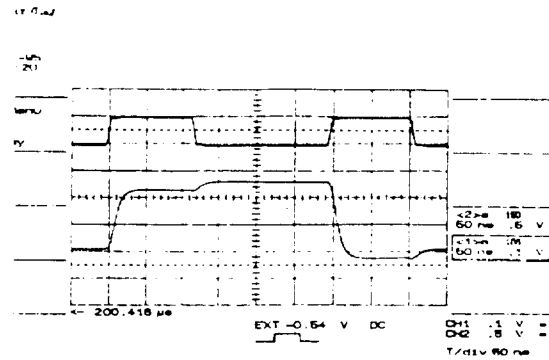


Figure 14 : Output waveform of the track and hold stage measured after 12Mrad. They show the clock and the output of the T&H when an input signal of 800 mV is applied. An important parasitic charge injection from the clock is visible, this effect is strongly enhanced by irradiation.

The shape of the response of the track-and-hold after 12Mrad is shown in Fig.14. We have measured a rise time of 19.7ns and a gain of 0.9, the circuit being still fully functional.

6. 11-BIT LOW POWER ADC

This circuit was the translation in HSOI3-HD of an already existing circuit. fabricated in a bulk 1.5 μm radiation soft technology. The specification requiring low power, speed higher than 5 MHz and a resolution higher on low-level signals (11-bits), the architecture of Fig.15 has been chosen. It performs a two-step analog-to-digital conversion using a 2-bit flash nonlinear converter for segmentation and 7 6-bit charge-redistribution ADCs.
It performs a two-step analog-to-digital conversion using a 2-bit flash nonlinear quantizer for segmentation and 7 6-bit charge-redistribution ADCs.
The circuit is currently in fabrication, and results should be available by the end of 1995. The speed performance, according to the simulation, should approach 20 MHz.
Compared with the bulk realization, minor modification were required on the comparator to achieve better radiation hardness. Lateral body ties needed to be added to every analog device for noise and stability reasons.

In HSOI3-HD, the parasitic gate capacitance is significantly higher, requiring an oversizing of the driving logic gates. Therefore, a full re-sizing of the whole logic circuitry was necessary to keep the aimed speed performance. Power consumption is thus also increased, as well as silicon surface. An opposite trend towards lower area is given by the smaller metal lines and by the possibility to place n- and p-channel transistors very close to each other.

The total area of the ADC chip in HSOI3-HD is 15 mm², whilst it was 10 mm² for the 1.5 μm bulk technology as shown in Fig.15.

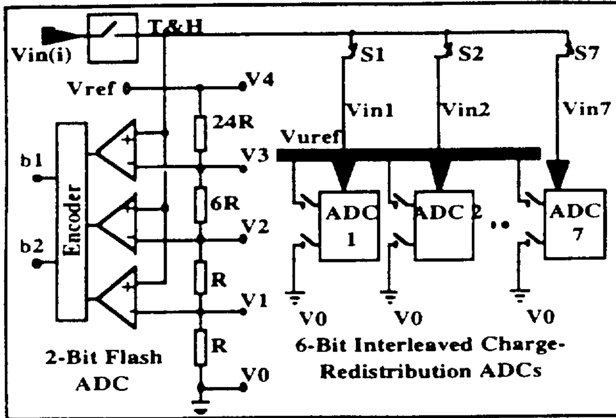
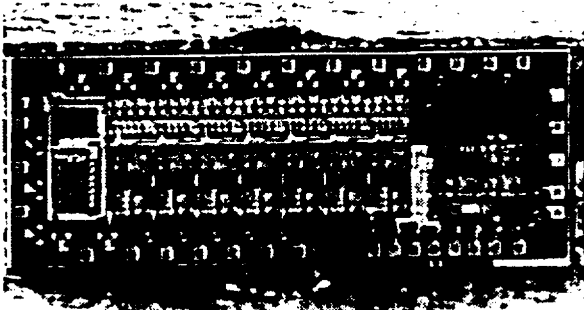


Figure : ADC architecture principle. The 2-bit flash part performs a segmentation of the reference voltage, whilst the 7 interleaved charge-redistribution ADCs need 7 clock cycles to perform the 6-bit conversion.



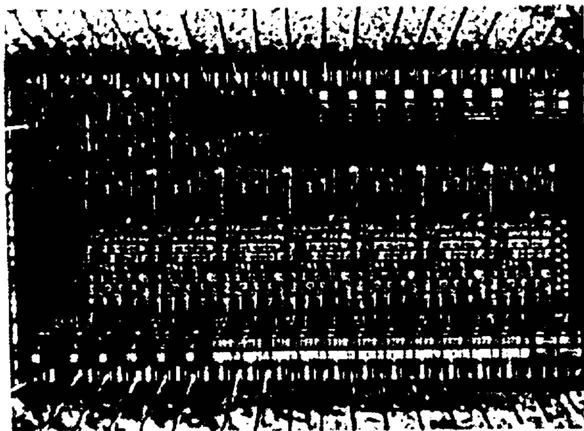


Figure 15 photograph of the CRIAD 11-bit ADC chip in 1.5µm CMOS soft process (upper picture) and in HSOI3HD (lower picture). The active chip area is respectively 6 and 8 mm^2.

necessary to keep the aimed speed performance. Power consumption is thus also increased, as well as silicon surface. An opposite trend towards lower area is given by the smaller metal lines and by the possibility to place n- and p-channel transistors very close to each other.

The total area of the ADC chip in HSOI3-HD is 15 mm^2, whilst it was 10 mm^2 for the 1.5 µm bulk technology as shown in Fig.15.

7. CONCLUSION

The study of the analog characteristics of the HSOI3HD technology has been carried out on both test transistors and circuits. Transistors threshold voltage shift, studied up to 25Mrad, is acceptable (maximum=-350mV for p-channel) and predictable. The noise and transconductance degradation is much lower for p-channel transistors, which should be preferred as input devices in low noise circuits. The presence of a G-R component in the noise spectra can be made negligible by an adequate body bias. This introduces nevertheless a further complication in circuit design, and studies to understand its origin and to eliminate it are under way. We have designed test circuits to evaluate the mixed mode capability of the technology, namely two amplifiers, a track-and-hold and an 11-bit low power ADC. The noise of the two amplifiers does not meet the LHC requirements, but better results are expected after a redesign which will approach the technology limits. All irradiated circuits still perform with full functionality after as much as 20Mrad, an increase of the noise of about 60% being the only real concern. A comparison with bulk radiation soft CMOS processes shows that the use of this technology has its major drawback in integration density and power consumption.

REFERENCES

[1] J.L.Leray et al., "From substrate to VLSI: investigation of hardened SIMOX without epitaxy, for dose, dose rate and SEU phenomena", IEEE Trans.Nucl.Science NS-35(1988)1355

[2] F. Faccio, M.Bianchi, M. Fornasari, E.H.M. Heijne, P. Jarron and G. Rossi, Noise characterisation of transistors in a 1.2µm CMOS-SOI technology up to a total dose of 12 Mrad (Si). IEEE Trans. On Nucl. Sci., Vol. 41, N0.6, pp. 2310-2316, December 1994.

[3] L.D.Yau and C.T.Sah, "Theory and experiments of low-frequency generation-recombination noise in MOS transistors", IEEE Trans.El.Devices 16(1969)170

[4] Y.P.Tsividis, Operation and modeling of the MOS transistor, New York, McGrow-Hill, 1988

[5] P.Jarron, F. Anghinolfi and W. Dabrowski, A novel current mode feedback technique for low noise transimpedance amplifier transimpedance amplifier using a. Presented at the 7th Europeen Symposium on semiconductor Detectors, Schoss Elmau, May 1995. To be published in NIM A.

[6] V.Valencic et al, "A low-power piecewise linear analog to digital converter for use in particle tracking", IEEE Trans.Nucl.Science NS-42, No4(1995)772

AN ADDITIONAL CONTRIBUTION IN THE NOISE SPECTRUM OF SOI MOSFETs

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Introduction

In view of possible analog applications, we have studied the noise characteristics of a medium-thickness SOI technology in the 200 Hz – 25 MHz bandwidth. We have found an additional noise contribution in the form of a hump in the noise spectrum, which can be moved widely in frequency and amplitude by changing the transistor bias. In this paper we present our hypothesis concerning its origin, and some measurements that support our interpretation.

Experimental details

The technology we have tested is a medium-thickness SOI. The silicon film can be completely depleted or not depending on the bias applied to the backgate and body electrodes [1]. The thickness of the gate oxide, silicon film and buried oxide is respectively 23 nm, 150 nm and 380 nm. The support for the technology is a SIMOX substrate. The silicon film is contacted to avoid floating body effects [2], and this is done via a lateral contact placed symmetrically on every edge of the transistor. This, moreover, prevents the formation of parasitic lateral conduction paths between source and drain even after exposure to ionising radiation. The width of all the measured transistors was 2000 μm, obtained by connecting 200 elements with W=10 μm in parallel. The noise measurements were performed, where not specified, in saturation and in strong inversion.

Model for the additional noise contribution

The noise spectrum of the measured transistors, referred to the gate, is qualitatively as shown in figure 1 for both n- and p-channel devices.

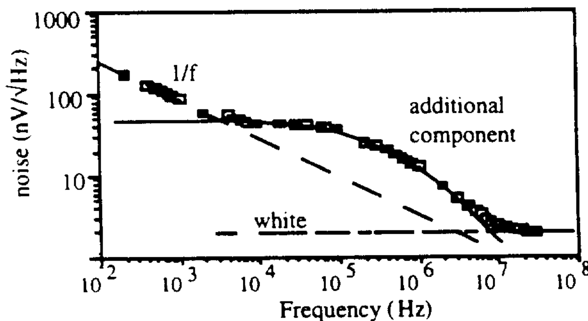

Figure 1: qualitative noise spectrum referred to the gate.

The standard 1/f and white noise components are still visible, though the superposition of an additional source increases considerably the overall noise. This component can be described with a set of two parameters: the noise level at the plateau and the cutoff frequency, which is the frequency where the noise is 3 db under the value at the plateau. A change in the potential applied to the backgate or body electrodes moves the cutoff frequency and modifies the amplitude dramatically. This occurs in a bias range where the depletion condition of the silicon film and hence its resistance are strongly sensitive to the bias.

The potential of the silicon film which constitutes the body is imposed by an external bias. The resistance seen from the power supply to the film is significant, and we assume that it increases with the depletion of the film itself. We call this resistance R_{body}. If we then introduce the capacitance of the gate and backgate oxides, we obtain the model shown in figure 2.

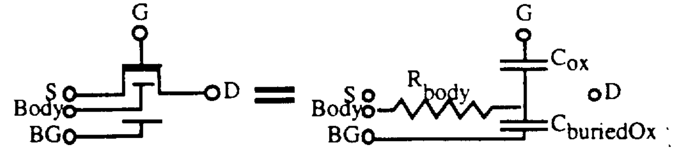

Figure 2: equivalent model

This resistance gives a thermal voltage noise spectral density

$$S_{Vbody}{}^2=4kTR_{body} \quad (1)$$

which is transmitted as a current noise to the drain through the body transconductance. When we measure the noise of the device, we convert the current noise at the drain into voltage noise by using a transimpedance amplifier, and we then refer all to the gate of the transistor. As a result of this, the voltage noise of R_{body} gives the following contribution to the total equivalent voltage noise to the gate:

$$S_{Vgate}{}^2=4kTR_{body}\,(g_{mb}/g_m)^2 \quad (2)$$

This is independent of the frequency. The resistance together with the capacitances C_{ox} and $C_{buriedOx}$ make a low pass RC filter with a cutoff frequency

$$f_c=1/2\pi RC \quad (3)$$

The resulting filter cuts the white noise at the cutoff frequency, therefore in the noise spectra referred to the gate it is seen as a hump. The schematic of the process is depicted in figure 3.

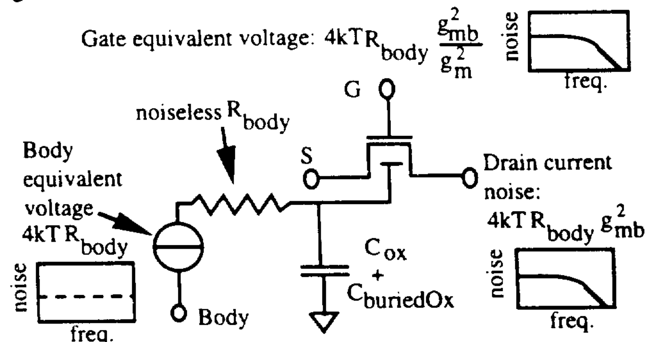

Figure 3: transmission of the white noise due to R_{body}.

Experimental observations

Our model is supported by the following experimental results:

i) there is a correlation between the magnitudes of R_{body} and the hump;

ii) when R_{body} is equal in different bias conditions, also the equivalent voltage noise referred to the body is equal;

iii) the correlation is valid also when the transistor works in the ohmic regime;

iv) the RC filter is effective for all signal injected through the body terminal.

We now detail these observations for the case of the n-channel transistor; they are similar for the p-channel.

i) In order to get a very rough estimate of R_{body}, we have designed a special transistor with the two edges of the body film extracted on two separate contacts, as shown in figure 4. The resistance R_{meas} measured between the two body contacts (Body 1 and Body2) should be related to the actual R_{body}.

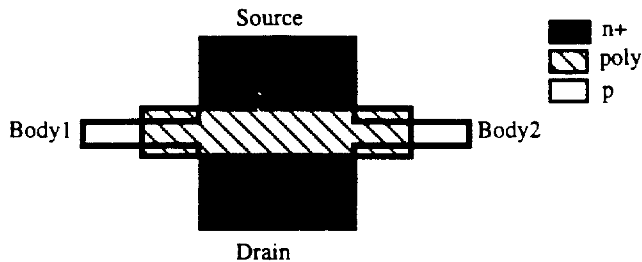

Figure 4: layout of the transistor designed to estimate R_{body}.

R_{meas} varies between about 1.5kΩ and more than 1MΩ when the body and backgate bias are changed to deplete the film. This happens in the voltage range over which the noise hump moves widely in amplitude and frequency. This correlation between R_{meas} and the additional noise is then confirmed from the measurement on transistors with the same width but with different gatelength. Both the noise at the plateau and R_{meas} increase for the shortest transistors.

ii) We have chosen two different bias conditions, one with the body grounded (and V_{BG}=9V) and the other with the backgate grounded (and V_{body}=-0.7V), for which R_{meas} is the same. The value at the plateau referred to the gate is different, but referring it to the body using (2), we get $Sv_{gate}^2 \approx 7.2nV/\sqrt{Hz}$ in both cases. Similar results are obtained for other bias values.

iii) When the same body and backgate bias is applied in the saturation and ohmic working regimes, the value of R_{meas} is the same, whilst the ratio between the transconductances is different. The gate-referred noise at the plateau is therefore different in the two regimes, as shown in table I. The body-referred noise is instead equal within 20%, which is reasonable when considering the error on the measurements and its propagation in the calculations.

Table I: noise at the plateau referred to the gate and body. The body bias was 0V in both cases, and R_{meas} was equal in saturation and ohmic region for each bias condition.

		Gate-referred noise at plateau (nV/√Hz)	Body-referred noise at plateau (nV/√Hz)
V_{BG}=13V	saturation	45	69
	ohmic	14.7	67.1
V_{BG}=12V	saturation	17.5	25.5
	ohmic	6.6	30.2

Using the body-referred noise value in (1), we extract R_{body}. For the two bias values of table I, we get respectively about 50kΩ (V_{BG}=13V) and 290kΩ (V_{BG}=12V). In both cases, this value is a factor 5 less than R_{meas}. We insert the extracted resistance values in (3), where f_c is estimated from the cutoff frequency of the hump in the noise measurement, and we extract the capacitance of the RC circuit to get C≈7pF. For the transistor under test, C_{ox}≈13.5pF and $C_{buriedOx}$≈1.6pF. Considering that for the small signal model of a transistor the capacitance seen from the body is equal to a fraction of the total gate capacitance, the extracted C fits well our RC model.

iv) The final evidence that supports our model comes from the gain analysis of the transistor for a signal injected through the body. The hump in the two bias conditions chosen has a different f_c, as shown in figure 5. As expected from the model, the low pass filter is effective for every signal injected through the body terminal.

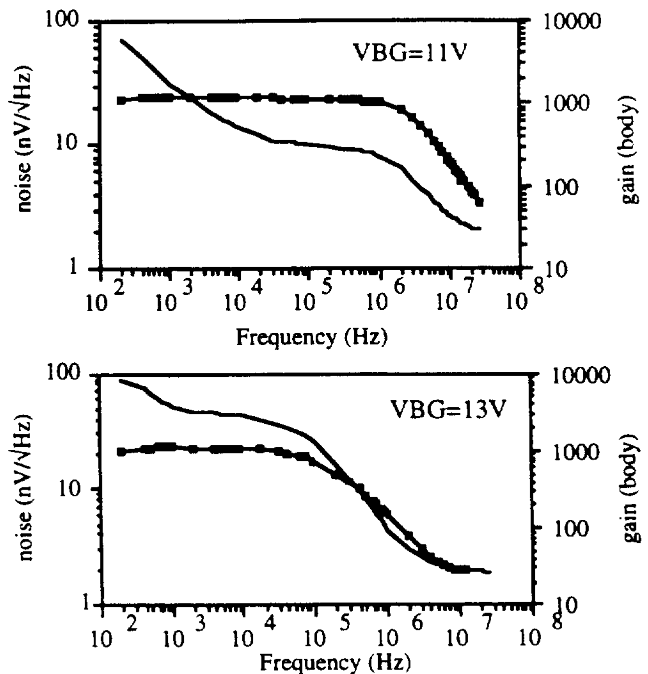

Figure 5: noise referred to the gate (solid line) and gain for a signal injected through the body (line with black squares) for two bias conditions. V_{body}=0V.

Finally, we can use the gain in figure 5 to refer the noise of the same figure to the body terminal. The resulting spectra show no hump, but a white noise whose value is in agreement with the one foreseen by the model.

Conclusion

We have identified an additional noise source in the spectrum of SOI medium-thickness transistors. Its origin is the resistance of the silicon film which constitutes the body of the transistor, coupled to the gate capacitance to form an RC equivalent low pass filter.

References

[1] J.P.Colinge, *Silicon-on-insulator technology: materials to VLSI*, Kluwer academic publishers, 1991, p. 109

[2] T.Ouisse et al., "Investigation of floating body effects in silicon-on-insulator metal-oxide-semiconductor field-effect transistors", *J. Appl. Physics*, Vol. 70, No. 7, pp. 3912-3919, october 1991.

DEVELOPMENT OF FRONT-END ELECTRONICS FOR SILICON STRIP DETECTORS USING THE DMILL BICMOS RAD-HARD PROCESS.

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ABSTRACT

An overview of development of front-end electronics for silicon strip detectors using the DMILL 0.8 μm BiCMOS radiation hard process is presented. The DMILL technology offers an excellent radiation hardness performance for a wide variety of devices: MOSFETs, BJTs, JFETs and high value resistors. Our development follows the two basic readout architecture, analog and binary, considered for the ATLAS Semiconductor Tracker at the LHC. Two 32-channel demonstrator chips: SCT32A for the analog architecture and SCT32B for the binary one have been designed and manufactured successfully. Following the 32-channel demonstrator chips the 128-channel versions of both architectures have been designed. The results obtained for the 32-channel demonstrator chips as well as the designs of the 128-channel versions is presented. The performance of the front-end circuit based on a fast transimpedance BiCMOS preamplifier which has been implemented in both architectures is discussed. Along with the results on fabricated chips the radiation effects in DMILL bipolar transistors is presented.

1. INTRODUCTION

The DMILL technology offers an excellent radiation hardness performance for a wide variety of devices: MOS transistors, fast bipolar transistors, junction field effect transistors and high value resistors with low stray capacitance [1]. It is therefore suitable for mixed signal chip architectures and offers a unique possibility to integrate fast low noise analog circuits and digital functions in a single chip. Our development follows the two basic readout architectures, binary and analog, considered as the baseline and the fall-forward solution respectively for the ATLAS Semiconductor Tracker. As a first step, two 32-channel demonstrator chips: SCT32A for the analog architecture and SCT32B for the binary one have been developed. Based on the results obtained for these demonstrator chips we have designed 128-channel versions of both readout architectures following the system specification for the SCT readout.

The development of the readout chips was carried on in parallel with the development and radiation hardness study of the DMILL technology. A fast transimpedance front-end amplifier based on a bipolar transistor is employed in both readout architectures. This solution offers a very good noise vs power figure of merit for relatively large detector capacitances, in the range of 15 - 20 pF, as foreseen for the ATLAS tracker. Therefore the noise performance and radiation hardness of bipolar transistors available in the DMILL technology have been studied in detail in order to understand whether these transistors are suitable for our applications and to verify their stability.

2. ANALOG READOUT ARCHITECTURE

The basic blocks of the analog readout architecture as implemented in the SCT32A and SCT128A chips are shown in fig. 1. The chip comprises four basic blocks: front-end amplifiers, analog pipeline, control logic including the derandomizing FIFO and output multiplexer. The front-end circuit is a fast

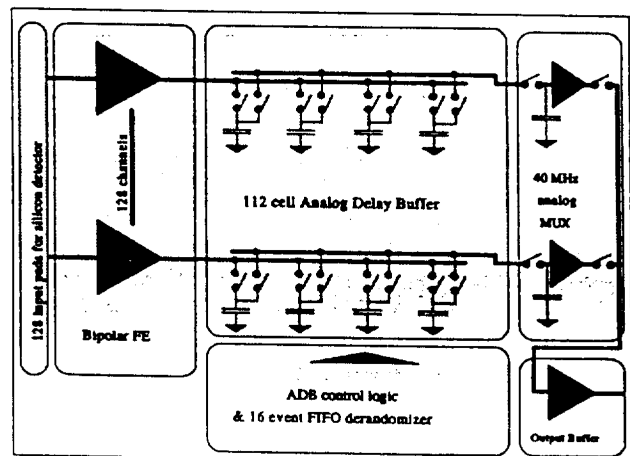

Fig. 1. Block diagram of the complete analog readout chip SCT128A.

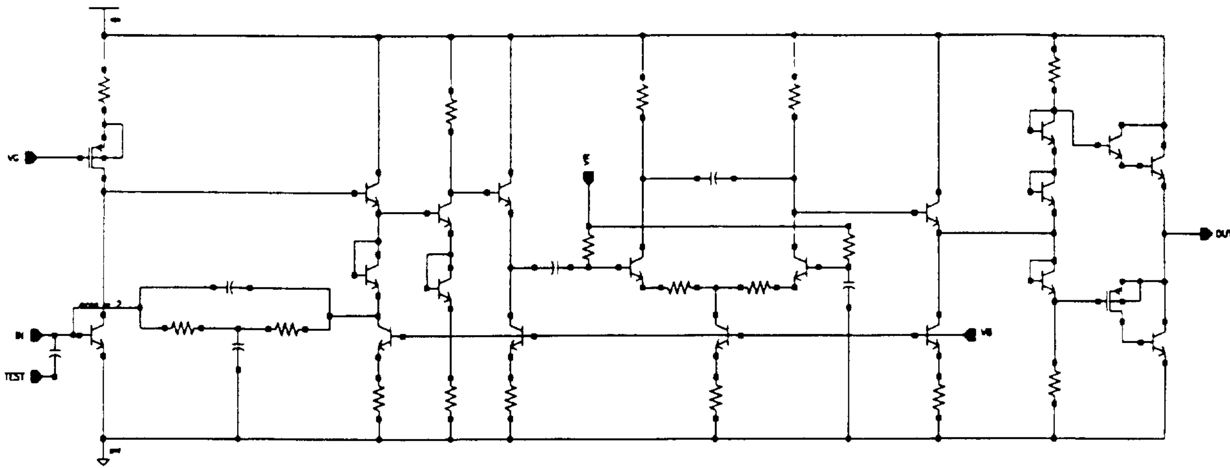

Fig.2. Schematic diagram of front-end circuit implemented in the SCT128A chip

transimpedance amplifier followed by an integrator, providing a fast semi-gaussian shaping with a peaking time of 25 ns, and an output buffer. The peak values are sampled at 40 MHz rate and stored in a 112-cell deep analog pipeline. The mean amplitude corresponding to 1 MIP input signal is about 70 mV and it is sufficiently high so that the noise figure obtained for the front-end amplifier will not be degraded by the second stage contribution. A storage capacitor of 310 fF for a single cell has been chosen. The concept of the pipeline and of the control logic is similar to the APC3 chip [2].

Once the trigger signal arrives, the analog values from a 128-channel memory column chosen by the read pointer are read out via the output multiplexer. The delay between the write pointer and trigger pointer is tuneable between 2 μs and 2.5 μs. In the first 32-channel version a moderate speed multiplexer working up to 10 MHz has been implemented to test the performance of the front-end circuit and the analog pipeline. For the 128-channel version a 40 MHz multiplexer has been designed which allows to multiplex 256 channels (2 chips) onto one optical link for the level 2 trigger rate of 100 kHz as foreseen for the ATLAS experiment.

1.1. FRONT-END CIRCUIT

The front-end circuit is based on a transimpedance amplifier with a bipolar input transistor since for large detector capacitances and short shaping time constants bipolar devices offer a superior noise vs power figure of merit [3]. The schematic diagram of the preamplifier-shaper circuit is shown in fig. 2. The input stage designed as a BiCMOS transimpedance amplifier is followed by a single gain stage and an integrator providing the proper peaking time. The output stage is designed as a class AB amplifier and provides sufficient driving capability to drive the analog pipeline at relatively low quiescent current of 100 μA. The total power dissipation of the front-end circuit, including the output buffer is below 1.5 mW/channel for a collector current of 200 μA in the input transistor.

There are two critical issues concerning bipolar transistors which determine their low-noise and radiation hardness performance, i.e. the base spread resistance and the degradation of current gain factor β caused by radiation damage. Radiation tests performed on individual bipolar transistors manufactured in the DMILL technology have shown a similar behavior of β as observed for other bipolar technologies [4], i.e. the β is more degraded when the current density is low. The size of the input transistor has to be optimized taking into account the series voltage noise contribution from base spread resistance and the parallel current noise due to the base current. The later will increase after irradiation since we need to keep a constant value of the collector current in order to keep the voltage noise low.

Transistors of different emitter area from 1.2 x 1.2 μm^2 up to 2 x 1.2 x 10 μm^2 have been tested. For all types of transistors the base spread resistance has been evaluated from the noise measurements. Based on the radiation test results of individual transistors we have chosen a geometry for the input device which provides a relatively low value (of the order of 100 Ω) of the base spread resistance and a reasonable high current density.

The degradation of the current gain factor β for the transistor geometry as used in the input stage after different radiation tests is shown in fig. 3. One set of devices was irradiated with photons in a Co-60 source up to a total dose of 10 Mrad and the other one in a high energy proton beam up to a total fluence of 1.7 x 10^{14} p/cm^2. In both cases the devices were kept under bias during and after irradiation at the room temperature. For the nominal collector current of 200 μA as foreseen for the input transistor the β is still above 60 after irradiation to the maximum doses expected for the ATLAS Semiconductor Tracker. This value of β is sufficiently high so that the parallel shot noise of the base current will not be a limiting factor after these extreme radiation

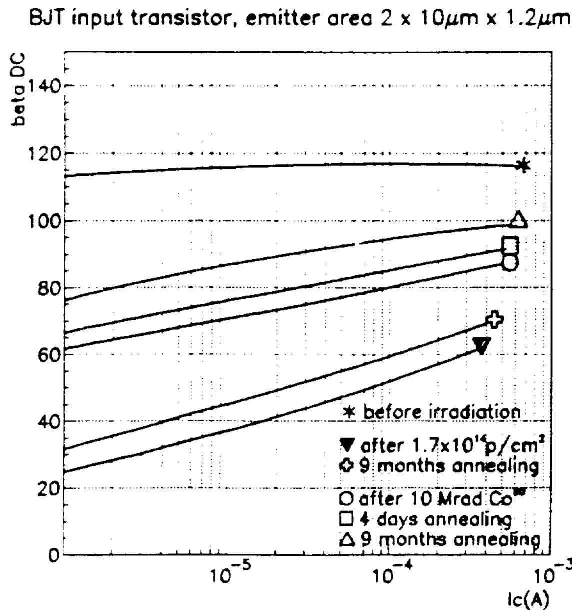

Fig. 3. Degradation of the current gain factor β for the transistor geometry used for the input device.

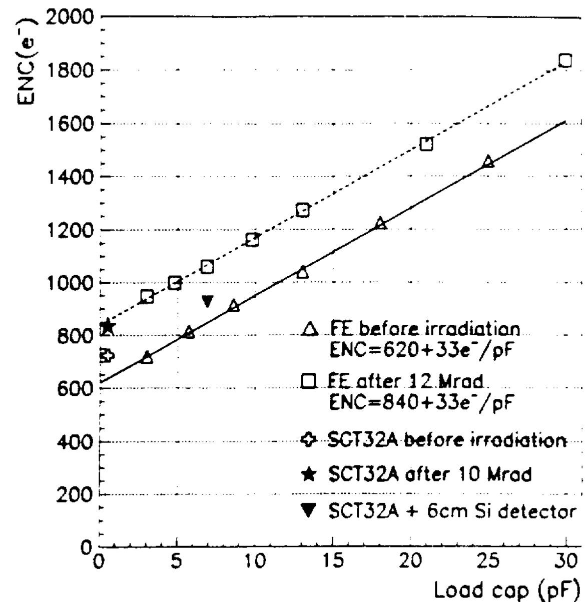

Fig.4. Summary of noise measurement performed for the BICMOS front-end only or with the full chip running.

doses. At room temperature a long term annealing is clearly visible for both sets of devices.

2.1. NOISE MEASUREMENTS

The noise measurements have been performed for the front-end circuit standing alone as well as for the full chip operating at a nominal clock frequency of 40 MHz. For the front-end amplifiers not connected to the pipeline the noise figures of ENC = 620 e^- + 33 e^-/pF has been obtained before irradiation and ENC = 840 e^- + 33 e^-/pF after 12 Mrad of gamma irradiation for a collector current of 220 μA in the input transistor. Performing the noise measurements while reading the signal and noise via the complete readout chain, including the pipeline clocked at 40 MHz and the multiplexer, a noise figure of 720 e^- was obtained for zero input capacitance. The noise (without signal) was measured reading randomly the cells of the pipeline so the measured value includes fluctuations introduced by cell-to-cell variation of the pipeline. Comparing the results of these two measurements, without the pipeline and with the pipeline, we obtain the cell-to-cell amplitude variation of 1 mV rms, to be compared with the 70 mV signal amplitude for 1 MIP input signal.

The obtained results indicate that additional sources of fluctuations, i.e. the pick-up of digital noise and the non-uniformity of pipeline storage cells, add only a marginal contribution to the noise figure of the front-end amplifier. For the detector capacitances of the order of 15 pF, as foreseen for the ATLAS Semiconductor Tracker, we do not expect any significant contribution from these additional noise sources.

The results of various noise measurements are shown in fig. 4. The noise figure obtained for the chip connected to a 6 cm long strip detector is consistent with other measurements performed for discrete capacitors connected to the input.

3. BINARY READOUT ARCHITECTURE

The block diagram of binary readout architecture realized in SCT32B and SCT128B chips is shown in fig. 5. The preamplifier and shaper implemented in this architecture use the same concept as used for the front-end in the analog architecture. The shaper is followed by a discriminator providing only 1-bit yes/no information which is stored into a 128-cell deep FIFO module.

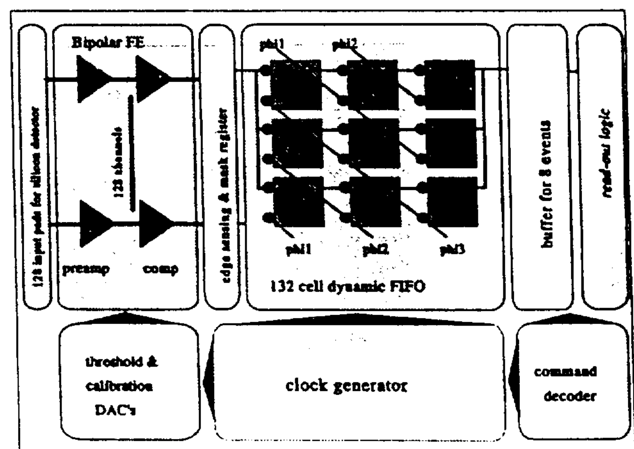

Fig. 5. Block diagram of the complete binary readout chip SCT128B

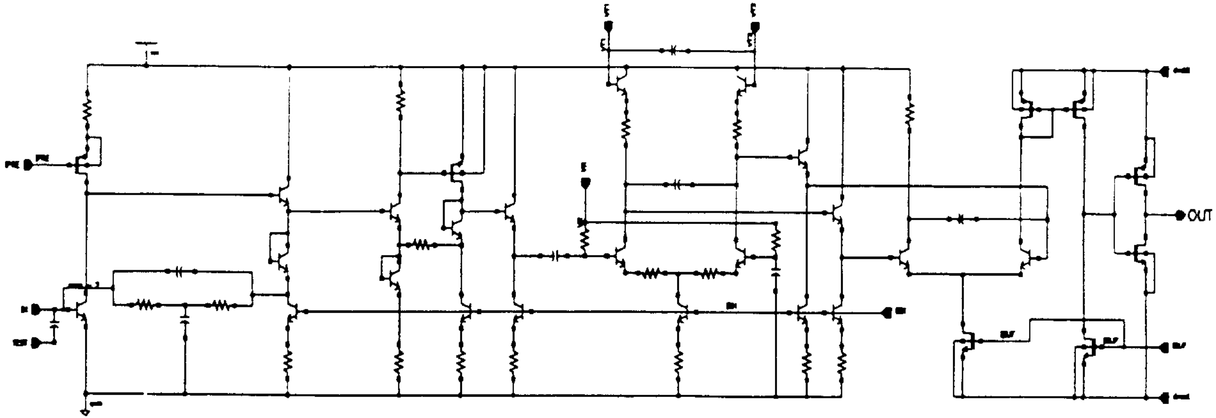

Fig. 6. Schematic diagram of the binary front-end circuit implemented in the SCT128B chip.

The SCT128B chip has been designed following the specification for the binary readout architecture. Originally the binary readout architecture has been proposed for the ATLAS semiconductor tracker by former SDC collaboration as a two separate chip solution, bipolar front-end and CMOS digital pipeline. The DMILL process allows us to implement both, the front-end and the binary pipeline in a single chip. The SCT128B chip, in addition to the basic functional blocks mentioned above, comprises in addition a calibration circuitry for internal generation of calibration pulses, one DAC for control of the amplitude of calibration pulses, another DAC for control of the discriminator threshold, and a 8-bit deep derandomizing readout buffer. The back-end control and readout logic is compatible with the HAC chip architecture [5].

4.1. BINARY FRONT-END CIRCUIT

The front-end circuit for binary readout architecture includes, in addition to the preamplifier and shaper, a discriminator. The schematic diagram of the front-end circuit implemented in the SCT128B chip is shown in fig. 6. The preamplifier is the same transimpedance BiCMOS configuration as used in the analog architecture. A key issue for the binary architecture is the channel-to-channel matching of gain, noise, and dc levels at the shaper output since a common threshold is applied for all 128 channels. The required uniformity is obtained by: (i) an ac coupling between the amplifier and the discriminator so that the dc offsets originated in the front-end circuit, which is a single ended structure due to noise requirements, are cut off, (ii) high enough gain in the preamplifier-shaper circuit, of the order of 100 mV/fC, so that the input offsets in the discriminator are negligible compared to the signal amplitude, (iii) applying a differential scheme for setting the discriminator threshold so that common mode effects are canceled.

The noise and gain measurements for a typical channel are shown in fig. 7. The upper plot shows the noise occupancy as a function of threshold applied to the discriminator. Since the threshold is applied differentially, the discriminator is sensitive either to positive or to negative pulses depending on the setting. By scanning the effective differential threshold around zero a full gaussian distribution of noise is obtained as shown in fig.7. From another threshold scan for a given signal applied to the input (lower plot) the signal amplitude at the input of discriminator and so the gain of the front-end circuit is measured. The noise figure can be evaluated from these two measurements as ENC = 670 e^-

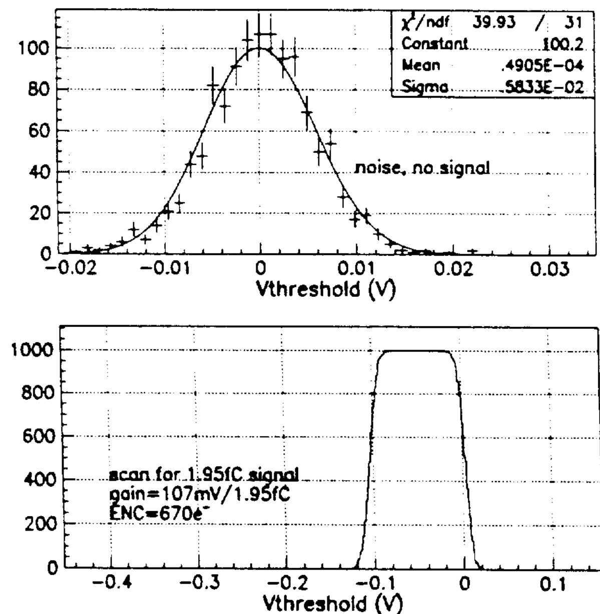

Fig. 7. Noise and gain measurement for a single channel of the SCT32B chip. The number of noise counts when no signal is applied and the number of signal counts is plotted as a function of the discriminator threshold voltage.

for the zero input capacitance. This value agrees well with the number obtained for the analog chip SCT32A in which a similar front-end circuit has been implemented. Also for the binary architecture we do not observe any significant noise increase when the chip is fully operating at 40 MHz clock frequency.

4.2. BINARY PIPELINE

The binary pipeline is realized as a multiplexed FIFO circuit. The principle of operation of this circuit is shown schematically in fig. 8. An array of *n x n* dynamic memory cells is controlled by *n* non-overlapping clock signals. In each clock cycle only *n* cells out of *n x n* are switched while the effective delay provided by such a block is equal *n x (n-1)* clock cycles. The applied architecture results in two very valuable features: low power consumption and a very compact layout. The pipeline block of 128 channels, each 132-bit deep, occupies only the area of 9 mm^2. The expected power consumption for this block is of the order of 140 μW/channel at clock frequency of 40 MHz and does not depend on the data rate.

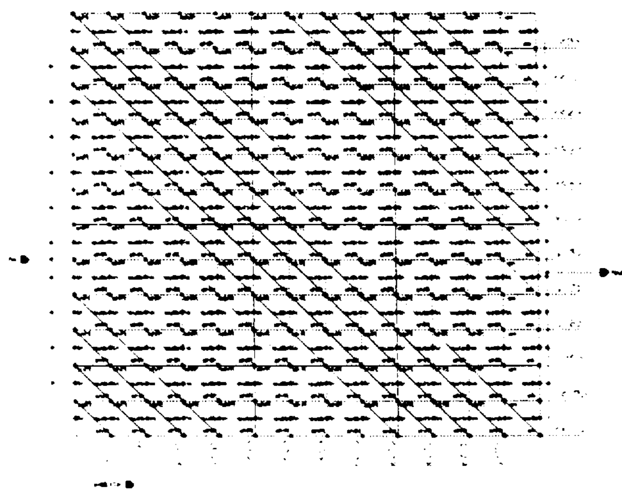

Fig. 8. Circuit principle of the binary pipeline based on a multiplexed FIFO circuit.

The chip has been irradiated in Co-60 source up to 10 Mrad under nominal static bias. The main goal of this test was to check the radiation hardness of the digital pipeline structure. The chip has been tested successfully at different clock frequencies up to 50 MHz before and after irradiation. After irradiation an increase of the power consumption is observed as expected (fig. 9). The measured power shown in fig. 9 is higher compared to the expected 140 μW/channel but it includes a contribution from the ECL-to-CMOS converters for the clock and control signals implemented in the SCT32B. In the final design the clock and signal receivers will be designed according to the LVDS standard resulting in a lower power consumption.

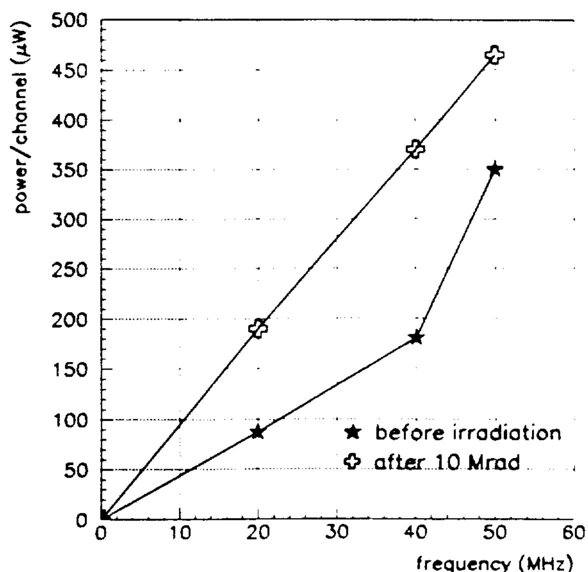

Fig. 9. Power consumption per channel of the 132-bit deep pipeline as a function of clock frequency before and after irradiation in Co-60 source up to 10 Mrad. The measured values include the power consumption of the ECL-to-CMOS clock and control signal receivers.

4. CONCLUSIONS

The results obtained for the prototype chips SCT32A and SCT32B prove that the DMILL technology offers the performance and appropriate radiation hardness required for the readout electronics for the ATLAS Semiconductor Tracker. The completed designs of the full size 128-channel chips, SCT128A and SCT128B, show that the DMILL technology is suitable for either readout architecture.

REFERENCES

1. M. Dentan et al., First Workshop on Electronics for LHC Experiments, CERN/LHCC/95-56, 1 October 1995, p.41.
2. K. Borer et al., IEEE Trans. Nucl. Sci. NS-41/4 (1994) 1091.
3. P. Jarron et al., First Workshop on Electronics for LHC Experiments, CERN/LHCC/95-56, 1 October 1995, p.130.
4. P. Barberis et al., Nucl. Phys. B32 (1993) 540.
5. J. DeWitt, IEEE Nuclear Science Symposium, Conference Record, Vol.2, p. 749, San Francisco 1993.

SCTA - A Rad-Hard BiCMOS Analogue Readout ASIC for the ATLAS Semiconductor Tracker

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Abstract

Two prototype chips for the analogue readout of silicon strip detectors in the ATLAS Semiconductor Tracker (SCT) have been designed and manufactured, in 32 channel and 128 channel versions, using the radiation hard BiCMOS DMILL process. The SCTA chip comprises three basic blocks: front-end amplifier, analogue pipeline and output multiplexer. The front-end circuit is a fast transresistance amplifier followed by an integrator, providing fast shaping with a peaking time of 25 ns, and an output buffer. The front end output values are sampled at 40 MHz rate and stored in a 112-cell deep analogue pipeline. The delay between the write pointer and trigger pointer is tunable between 2 μs and 2.5 μs. The chip has been tested successfully and subsequently irradiated up to 10 Mrad. Full functionality of all blocks of the chip has been achieved at a clock frequency of 40 MHz both before and after irradiation. Noise figures of ENC = 720 e^- + 33 e^-/pF before irradiation and 840 e^- + 33 e^-/pF after irradiation have been obtained.

I. INTRODUCTION

The readout of silicon tracker systems for the LHC experiments requires high density multichannel mixed signal ASICs combining several analogue processing functions with high speed digital circuits. The analogue readout of tracker systems with several millions of channels requires the use of low power design techniques such as the analogue memory CMOS circuit which locally store analogue signals during the level 1 trigger latency [1], [2], [3], [4], [5], [6]. The analogue memory technique performs simultaneous read and write operations enabling detector readout without dead time. We present here an approach based on the same architecture principle as developed before, but the analogue front end has been designed with bipolar devices available in the DMILL technology [7]. The DMILL technology offers an excellent radiation hardness performance [8], [9] for a wide variety of devices: MOS transistors, fast bipolar *npn* transistors, junction field effect transistors and high value resistors with low stray capacitance. It is therefore suitable for mixed signal chip architectures and offers a unique possibility to integrate fast low noise analogue circuits and digital functions on a single chip.

In the DMILL technology we have at our disposal all three types of transistors, JFET, MOSFET and BJT, which can be used as input devices. The *npn* bipolar transistor offers the highest g_m/I_c ratio and the lowest input capacitance. For this reason, the *npn* bipolar transistor is intrinsically the best input device for a low noise preamplifier when the series noise contribution dominates. This is a particularly relevant issue for silicon strip trackers at the LHC with a typical strip capacitance of 20 pF and signals with a peaking time of 25 ns in the front-end signal processor.

For comparison of the noise performance between front-end systems with the bipolar and the MOS transistor we assume triangular shaping offering an effective noise suppression for both series and parallel noise sources. For a readout system using a bipolar input device biased with collector current I_c the equivalent noise charge (ENC) is given as

$$ENC = \sqrt{\frac{4kT\left(r_{bb} + \frac{kT}{2qI_c}\right)\left(C_a + C_d\right)^2}{T_p} + \frac{2qI_cT_p}{3\beta}} \quad (1)$$

where r_{bb} is the base spread resistance and β is the current gain factor of the input transistor, C_a is the amplifier input capacitance, typically below 0.5 pF, C_d is the detector capacitance and T_p is the peaking time of the filter. The parallel noise contribution from the feedback resistor is ignored here since for an optimized preamplifier this contribution is negligible.

For a given peaking time, detector capacitance and current gain factor one can find an optimum value of the collector current which gives the minimum noise. Degradation of the β factor due to radiation damage of the bipolar transistors should be taken into account as this will result in some degradation of noise and a different optimum value of the collector current. The contour plot of constant ENC as a function of the collector current and β factor is shown in fig. 1.

The plot shown in fig. 1. indicates that a noise below 1200 e^- rms can be obtained for a detector capacitance of 20 pF and a relatively low collector current, about 200 μA. A degradation of β, even down to 50 as expected for DMILL transistors irradiated up to 2×10^{14} p/cm^2, causes only a minor increase in noise (up to 1300 e^- rms). Accepting this increased noise one can then use the transistor with a lower collector current, about 150 μA. The low value of the optimum collector current matches the low power requirements of the Atlas Semiconductor Tracker readout very well.

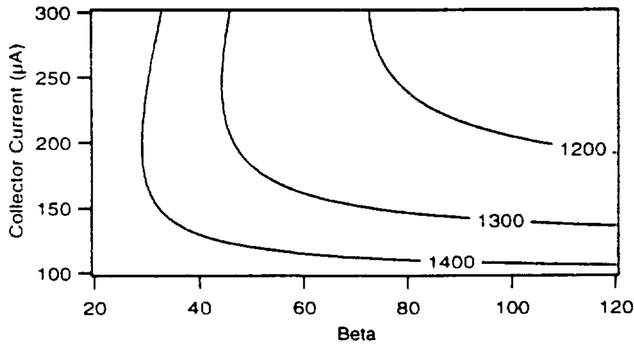

Figure 1: Constant noise contours for a bipolar input transistor and ideal triangular shaping of 25 ns peaking time. Base spread resistance of 50 Ω and detector capacitance of 20 pF is assumed.

For a MOS input device and triangular shaping the equivalent noise charge is given as

$$\mathrm{ENC} = \sqrt{\frac{4kT\frac{2\Gamma}{3g_m}\left(C_a + C_d\right)^2}{T_p}} \tag{2}$$

where g_m is the transconductance, Γ is the excess noise factor and C_a is the input capacitance of the input MOS transistor. Compared with a bipolar transistor the amplifier input capacitance is not negligible since a large Width/Length ratio (W/L) for the input transistor is required to give a high transconductance. Given a minimum length allowed by the technology and short channel effect a large W/L can be obtained by increasing the width and so the total gate area. For a comparison of the noise vs power figure of merit, it is important to notice that transconductance is proportional to collector current in a bipolar transistor while for a MOS transistor it is proportional only to the square root of the drain current. Thus for a given detector capacitance and shaping time there are two parameters, the width of the input transistor and the drain current which should be optimized in a system using MOS input transistors.

The constant ENC contour plot for typical parameters of a PMOS transistor in a submicron technology is shown in fig.2.

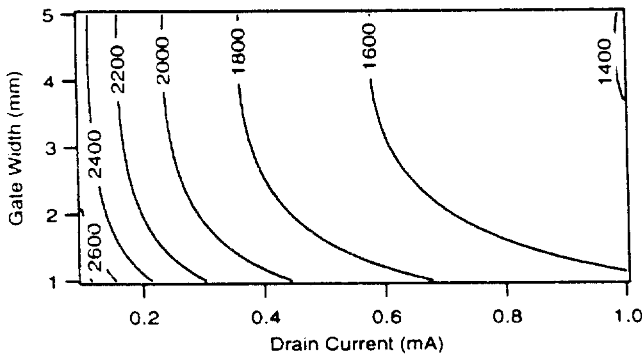

Figure 2: Constant noise contours for a PMOS input transistor, ideal triangular shaping of 25 ns peaking time and a detector capacitance of 20 pF. Minimum gate length of 1.5 µm, gate capacitance of 1.5 fF/µm² and Γ factor of 1.5 has been assumed.

The contour plot shows that an ENC of 1800 e⁻ rms is achieved for a drain current of 400 µA and a gate width ranging from 2000 µm to 4000 µm. This result indicates that with a bias current twice as high in the MOS device, the minimum achievable noise is still 60% more than for a bipolar device. The lower series noise factor, 1/2 for a bipolar device compare to 1 for a p-channel MOS, and the lower input capacitance, 0.5 pF for a bipolar device and 5 pF for a large p-channel MOS input device explain this significant difference in noise performance.

In addition, radiation damage increases the series noise factor of the MOS transistor whereas bipolar series noise is unchanged. The additional parallel noise caused by the beta drop of an NPN device in the DMILL process, typically 100 to 60 after 2×10^{14}protons/cm², is not significant when compared to the detector shot noise after irradiation.

The measurements of ENC versus C_d for a bipolar transistor as shown later in sect. IV indicate that the contributions from parallel and series noise add almost linearly. This indicates that the two noise sources in a bipolar transistor are significantly correlated for high frequencies. For a relatively large detector capacitance, about 20 pF, this effect does not play a major role since the total noise is dominated by the series noise.

II. CHIP ARCHITECTURE

Fig. 3 shows the block diagram of the SCTA chip architecture which has been designed in two versions, 32 channels and 128 channels. The chip comprises four basic blocks: front-end amplifier, analogue pipeline, control logic including a derandomizing FIFO, and an output multiplexer. The front-end circuit is a fast transresistance amplifier followed by an integrator, providing a semi-gaussian shaping with a peaking time of 25 ns, and an output buffer. The peak values are sampled at 40 MHz rate and stored in the 112-cell deep analogue pipeline. The mean amplitude obtained for a 1 MIP input signal is about 100 mV. It is sufficiently high that analogue signal processing after the front end does not contribute significantly to the overall noise figure.

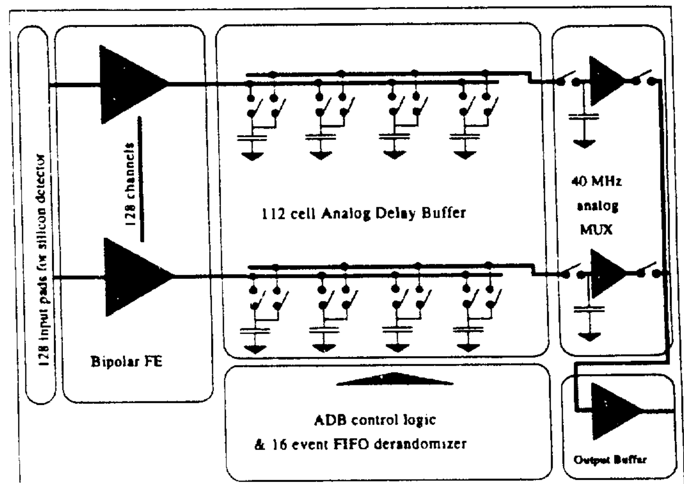

Figure 3: Block diagram of the SCTA - a full analogue readout chip.

A. BiCMOS preamplifier Shaper

The front-end circuit is based on a transresistance amplifier with a bipolar input transistor for the reasons presented in sec. I. The schematic diagram of the preamplifier-shaper circuit is shown in fig. 4. The input stage designed as a BiCMOS transimpedance amplifier is followed

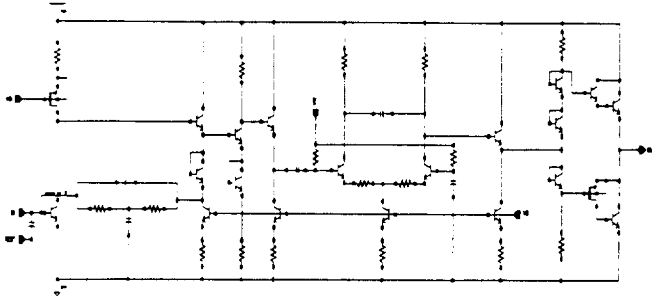

Figure 4: Schematic diagram of the front-end circuit implemented in the SCT128A chip.

by a single gain stage and an integrator providing the proper peaking time. The output stage is designed as a class AB amplifier and provides sufficient capability to drive the analogue pipeline at a relatively low quiescent current of 100 μA, so no extra write amplifier is needed in front of the analogue pipeline.

The transresistance preamplifier is built around a single ended NPN feedback pair circuit configuration which offers a low noise characteristic associated with a sufficient gain-bandwidth product. A phase margin of about 70° is achieved by a compensation network associated with the feedback resistor. The load of the input device is built with a p-channel MOS degenerated current source which offers a low output conductance and parasitic capacitance.

B. Analogue memory

The SCT128A memory samples the analogue signal voltage from the front end every 25 ns into a storage capacitor of 310 fF. The system performs a very simple and reliable voltage sampling. The readout need only retrieve the sample belonging to the peak of the pulse to recover the full time and amplitude information. Once the trigger signal arrives, the analogue values from the pointed physical address of the 128-channel memory column are read out via the output multiplexer. The delay between the write pointer and trigger pointer is tunable between 2 μs and 2.5 μs in the present version of the circuit.

C. Control logic of the analogue memory

Refering to fig. 5. the pipeline control of the memory allocation is done by two registers clocked at 40 Mhz, the Write column Register WR and the Trigger column Register TR, and one buffer, the Unused column Buffer UB. Register pointers have a delay between them such that the TR pointer passes memory cells later than the WR pointer by a delay equal to the trigger latency. The WR pointer controls writing of data into unused columns. The TR pointer sets a flag in the UB buffer at the request of an external trigger signal. The UB buffer thus holds flags to memory columns belonging to successive triggers. Because the readout time is generally longer than the loop pointer time, WR and TR pointers skip over columns where flags are set in the UB buffer. Each time a trigger generates a flag in the UB buffer, the Address Encoder generates the 7-bit binary address of the column. The encoded words are stored in the Read Address FIFO. Once a read signal is received, the first available address in the FIFO is decoded through the Address Decoder, enabling the readout of the column. The decoding of this address is used to free the corresponding flag in the UB buffer.

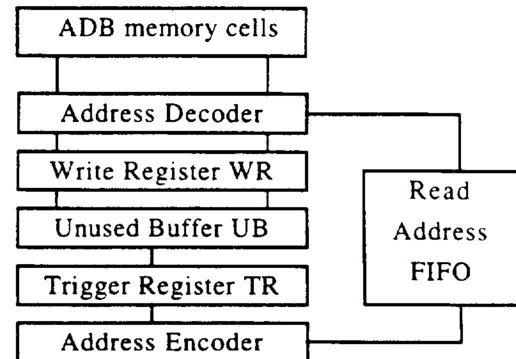

Figure 5: Block diagram of the memory control logic.

D. Analogue Multiplexer

The multiplexer chip contains 128 channels with sample-and-hold circuits and the output buffer. Each channel consists of an input switch, a storage capacitor and a sample-and-hold buffer designed as a source follower based on an NMOS transistor biased with 50 μA. In the readout phase this current is increased in the readout channel up to 600 μA which is sufficient to drive the parasitic capacitance of the internal bus line of the multiplexer. To provide a driving capability for 40 MHz operation of the chip placed on the final hybrid when the load capacitance is in the range of 60 pF, an additional output stage was necessary. A PMOS source follower biased with 5 mA current has been employed as an output buffer. The multiplexing function is implemented as a simple array of 128 NMOS switches controlled by a shift register. The 32-channel SCTA version has a moderate speed multiplexer working up to 10 MHz.

III. CHIP LAYOUT

The two versions, 32 channels and 128 channels, have essentially the same floor planning. Fig. 6 shows a photo of the 128 channel version, SCT128A. The front-end channels and the analogue pipeline are laid out with a pitch of 50 μm. The BiCMOS circuitry implemented in the front-end results in a very compact layout so that the front-end channel is only 800 μm long. The input bonding pads are laid out with 50 μm pitch. The die size is $9.3\times6.9 mm^2$.

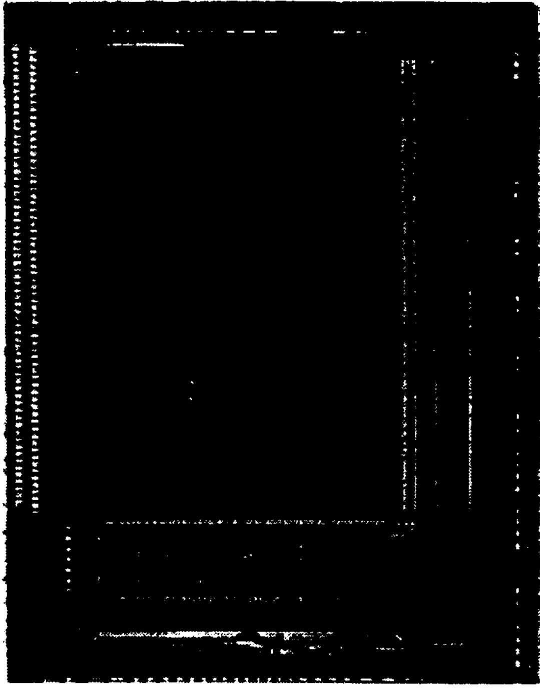

Figure 6: Photo of the SCT128A chip implemented in the DMILL BiCMOS process

IV. EXPERIMENTAL RESULTS AND PERFORMANCES

A. Output Signal

The response of the full chain to a 4 fC (≈1 MIP) charge impulse was measured by injecting a known voltage step across an on-chip calibration capacitor at the input. The pulse shape was traced by varying the time of the injected pulse with respect to the readout time so that a different time slice of the pulse is readout for each delay. The result is shown in fig. 7, whence it can be seen that the peaking time is indeed 25 ns, including the loading effect of a 6 cm strip detector bonded at the input.

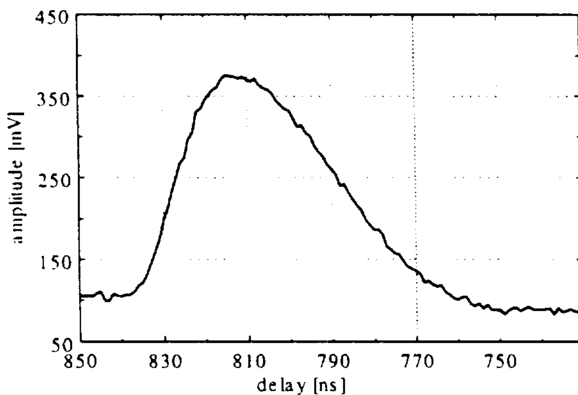

Figure 7: Output signal traced through the full processing chain, demonstrating the 25 ns peaking time. The injected charge was 4 fC and an additional external gain of 2.6 was applied.

B. Noise performance

Noise measurements have been performed for the front-end circuit alone and for the full chip operating at a clock frequency of 40 MHz. For the front-end amplifiers alone, a noise figure of ENC = 620 e⁻ + 33 e⁻/pF has been obtained before irradiation and ENC = 840 e⁻ + 33 e⁻/pF after 12 Mrad of gamma irradiation for a collector current of 220 μA in the input transistor. Measuring the noise through the complete readout chain, including the pipeline clocked at 40 MHz and the multiplexer, a figure of 720 e⁻ was obtained for zero input capacitance. The noise was measured by randomly reading the cells of the pipeline so the measured value includes cell-to-cell variations in the pipeline. Comparing the results of the measurements with and without the pipeline, we obtain a cell-to-cell amplitude variation of about 1 mV rms, to be compared with 100 mV signal amplitude for 1 MIP input.

The results indicate that additional sources of fluctuations, i.e. the pick-up of digital noise and the non-uniformity of pipeline storage cells, add only a marginal contribution to the noise of the front-end amplifier. For detector capacitances of the order of 20 pF, as foreseen for the ATLAS Semiconductor Tracker, we do not expect any significant contribution from these additional noise sources.

The results of various noise measurements are shown in fig. 8. The noise figure obtained for the chip connected to a 6 cm long strip detector is consistent with other measurements performed with discrete capacitors connected to the input.

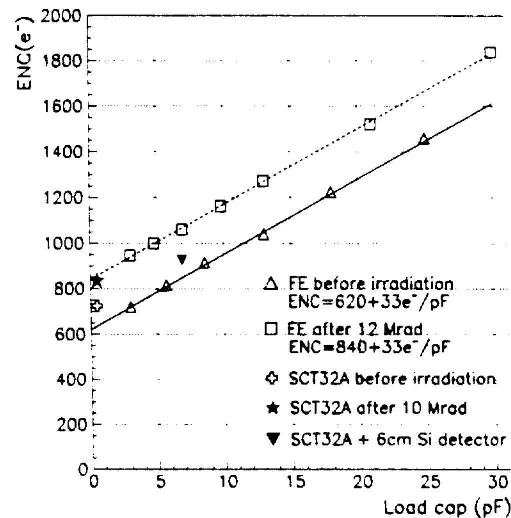

Figure 8: Summary of noise measurement performed for the BICMOS front-end alone, or with the full chip running.

C. Detector readout with ^{106}Ru beta source

The chip was bonded to a 6 cm long 280 μm thick n type detector with n⁺ strips at 112 μm readout pitch with one intermediate strip to optimize charge sharing. The strips were isolated by individual p⁺ implanted boxes. The detector was biased to 140 V and a scintillator trigger was used to initiate

the readout control sequence of the SCTA. In order to ensure only the peak of the pulses was read, an 8 ns time window was defined in phase with the 40 MHz clock and used as a veto against all events falling outside of this time. A ^{106}Ru beta source was placed above the detector and the multiplexed data read into a digital oscilloscope and stored for further analysis. The histogrammed result of cluster signal/noise is shown in fig. 9.

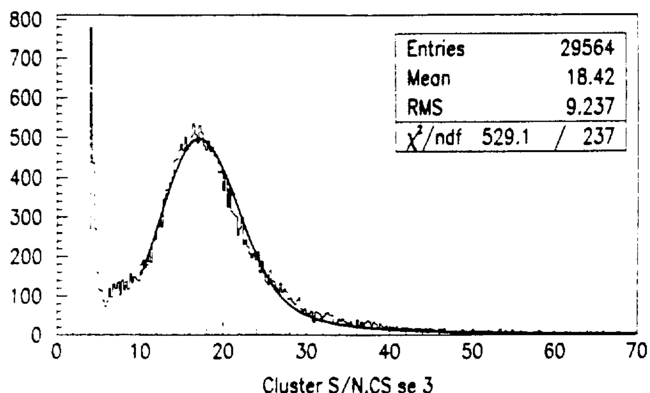

Figure 9: Histogram of data taken with a detector and a beta source, showing Landau peak at signal/noise = 18

V. RADIATION HARDNESS CHARACTERISTICS

A. NPN Bipolar device

Two critical issues determine the noise performance and radiation hardness of bipolar transistors, i.e. the base spread resistance and the degradation of β with irradiation. Radiation tests performed on individual bipolar transistors manufactured in the DMILL technology showed a similar behavior for β to that observed in other bipolar technologies [3,4], i.e. for lower current density a larger degradation of β is observed.

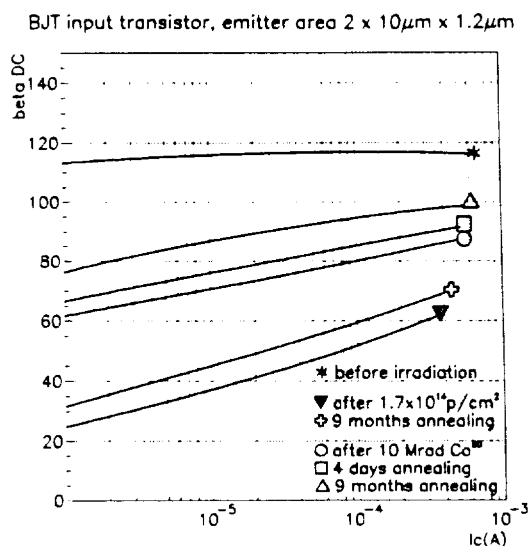

Figure 10: Degradation of the current gain factor β for the transistor geometry used for the input device.

The size of the input transistor has to be optimized taking into account the series voltage noise contribution from base spread resistance and parallel noise due to shot noise of the base current. The latter will increase after irradiation since a constant collector current should be maintained to keep the voltage noise low.

Transistors of different emitter areas from 1.2 x 1.2 μm^2 up to 2 x 1.2 x 10 μm^2 have been tested. For all types of transistors the base spread resistance has been evaluated from the noise measurements. Based on the radiation test results of individual transistors we have chosen a geometry for the input device which provides a relatively low value (of the order of 100 Ω) of the base spread resistance and reasonably high current density. The degradation of β for the transistor geometry as used in the input stage after different radiation tests is shown in fig. 10. For a nominal collector current in the input transistor of 200 μA the β is expected to be above 60 after irradiation to the maximum doses expected in the ATLAS SCT. Using the above value of current in the input stage the total power dissipation of the front-end circuit, including the output buffer, is below 1.2 mW/channel.

VI. CONCLUSIONS

A 32 channel and a 128 channel version of a radiation hard analogue front end chip intended for the readout of trackers have been succesfully demonstrated to give adequate noise performance with load capacitances expected from strip detectors in the LHC experiments. In particular, full functionality has been shown at 40 MHz both before irradiation and after 10 Mrad dose, keeping power dissipation within acceptable limits and with little degradation of the noise.

REFERENCES

1. P.Jarron, et al., LeCroy conf, 1991 New York and CERN/ECP 91-24.
2. F. Anghinolfi et al. NIM **A326** (1993) pp. 100-111.
3. K. Borer et al. IEEE Trans. Nucl. Sci., **41**, No.4, Aug. 1994.
4. L.L. Jones, M. French and P. Seller, IEEE Trans. Nucl. Sci., **41**, No. 4, Aug. 1994.
5. F. Anghinolfi et al. NIM **A344** (1994) pp. 173-179.
6. R. Brenner et al. NIM **A339** (1994) pp. 477-484
7. M. Dentan et al. IEEE Trans. Nucl. Sci., **40**, No. 6 (1993) pp. 1555-1560.
8. L. Blanquart et al. IEEE Trans Nucl. Sci., **41**, No. 6, Dec. 1994, p.2525 ff.
9. M. Dentan et al. IEEE Trans Nucl. Sci., **43, June 1996**, III, part 2, p.1763 ff.
10. V. Radeka, Ann. Rev. Nucl. Part. Sci. **38** (1988) pp. 217-277

Noise Characterization of Transistors in a 1.2 μm CMOS-SOI Technology up to a Total-Dose of 12 Mrad (Si)

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Abstract

The analog performance of the Thomson HSOI3-HD technology has been measured up to a total dose of 12 Mrad(Si) of ionizing radiation (^{60}Co). The threshold voltage shift is -170 mV for p-channel and -20 mV for n-channel transistors. Transconductance degradation is respectively 4% and 17%. Noise has been measured in the 500 Hz-25 MHz bandwidth. In addition to the 1/f and white noise, a generation-recombination contribution appears in the noise spectrum. This contribution is sensitive to the bias applied to the backgate and body electrodes. The white noise increase after irradiation is 16% for p-channel and 35% for n-channel transistors. p-channel transistors have very low 1/f noise and are less sensitive to irradiation effects.

I. INTRODUCTION

The existing rad-hard technologies have been primarily developed for digital ICs. As a consequence, little attention has been devoted so far to their noise characteristics over a wide bandwidth. In particular, the noise of SOI radiation hardened technologies has never been extensively studied. In this paper, which expands our previous work [1], we present results on the noise performance of the HSOI3-HD rad-hard technology. This process, industrially developed by Thomson–CSF Semiconducteurs Spécifiques (TCS), is a 1.2 μm CMOS-SOI technology using a SIMOX substrate. The aim of our research is to investigate the analog characteristics and the radiation hardness of the technology in view of complex ICs for signal processing in experiments at the LHC (Large Hadron Collider, CERN, Geneva, Switzerland).

Our study covers irradiation and bias dependent annealing effects on n- and p-channel transistors. Noise has been studied in the 500 Hz-25MHz frequency bandwidth. Contributions from 1/f noise and white noise sources have been separately evaluated. In addition, we found that a localized source of free carrier generation can be activated if particular bias conditions are applied to the body and backgate electrodes. Its effect is to introduce a single time constant generation-recombination (G-R) contribution to the noise spectrum.

II. EXPERIMENTAL DETAILS

The HSOI3-HD technology is a polycide gate CMOS-SOI process [2, 3]. The SIMOX substrate is realized by 200 keV O^+ ion implantation at 500-700°C followed by annealing at 1300-1350°C. Isolation between devices is achieved by conventional LOCOS, and a LDD (Lightly Doped Drain) structure is used to lessen impact ionization due to high electric fields. Thickness of the gate oxide, silicon body and buried oxide are respectively 23 nm, 150 nm and 380 nm, and the transistors are partially depleted. The minimum line width in this technology is 1.2 μm (size of contacts, vias and interconnections), but the minimum drawn gate length allowed is 1.4 μm.

For this noise study we used large transistors with high transconductance to have a low equivalent input voltage noise density. The MOS-SOI n- and p-channel transistors we studied were actually five-terminal devices. We define as "backgate" the substrate electrode (common to the whole chip) and as "body" the silicon film under the gate oxide, accessible separately for every transistor via a lateral contact. The width of the measured transistors was W=1000 μm, and two different gate lengths were studied: L=1.4 μm and L=2 μm.

All measurements presented in this paper refer to one processing batch. A total of 10 chips, containing 4 transistors each, were used for the prerad measurements. Two of them were irradiated up to a total dose of 12 Mrad(Si). The noise measurements presented in this study were made after an annealing of three months.

Gamma irradiation took place with a calibrated ^{60}Co source at room temperature. It was performed in four steps with pauses at 1.5, 3.5, 7.5 and 12 Mrad(Si). The dose rates were respectively 18, 31, 54 and 54 rad/sec, and 5 hours interruption between each exposure was kept to perform static measurements. The uncertainty on the dose was 20%. We have not studied dose rate effects in our work.

We have chosen to simulate as much as possible the irradiation effects on the transistors in their operational condition. Therefore both irradiation and annealing occurred

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in air at room temperature with the devices continuously under bias. The transistors were connected in diode configuration ($V_{ds}=V_{gs}=1.1$ V for n-channel and -1.5 V for p-channel) with a source-drain current of 200 µA. For analog applications in front-end electronics (i.e. charge sensitive amplifiers), the input transistor gives the major contribution to the overall noise of the circuit. It normally operates with $V_{bg}=V_{ss}$ and V_{source} close to 0 V. To simulate its operational bias we have chosen $V_{body}=V_{source}=0$ V and a backgate bias $V_{bg}=-3$V.

Most noise measurements were performed with the device kept in saturation, with $V_{ds}=800$ mV, and with a constant source-drain current density of 0.5 µA/µm ($I_{ds}=500$ µA). The noise measurement chain is depicted in fig. 1. The drain current noise was amplified and transformed into voltage noise by a low noise transimpedance amplifier, then further amplified by a voltage gain stage and measured by an HP3588A spectrum analyzer. The reference source of the HP3588A was used to measure the frequency transfer function of the measurement chain, and a PC controlled the whole setup. In this configuration the noise was expressed as equivalent noise voltage referred to the gate by applying the system transfer function to the measured output noise. The potentials of the backgate and of the body could be adjusted externally in order to investigate their effect on the noise. With this setup, we could study the noise in the 500 Hz-25 MHz bandwidth.

Some additional measurements were done in the linear region of operation. In that case, the transistor was biased with a source-drain voltage $V_{ds}=20$ mV, and with a load resistor $R_d=8.3$ kΩ. The noise was amplified by a Brookdeal 5003 Nanovolt Amplifier and measured by the spectrum analyzer.

III. Results and Discussion

A. *Static parameters*

The evolution with dose of the noise performance and the static transistor parameters may be correlated. Therefore, we have measured again carefully these static parameters and found some difference between this processing batch and the previous one [1]. Although our results are based on measurements of about 10 devices in each case, we think that the difference is significant.

In table 1, we summarize the threshold voltage, transconductance and mobility of n- and p-channel transistors before and after 12 Mrad(Si) exposure and subsequent annealing. The mobility is extracted in the linear region ($V_{ds}=20$ mV), while the transconductance refers to saturation, with $I_{ds}=500$ µA and $V_{ds}=800$ mV.

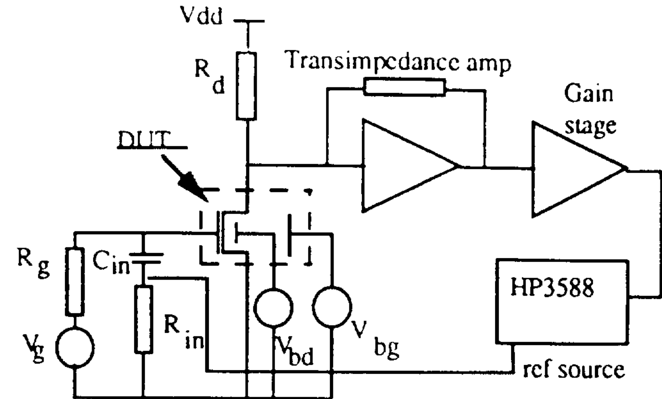

Figure 1: Noise measurement setup for transistors in the saturation region. The whole chain is controlled by a PC. The body (V_{bd}) and backgate (V_{bg}) potentials can be changed externally. $R_g=1$ MΩ, $R_{in}=50$ Ω, $R_d=10$ kΩ.

Both n- and p-channel transistors prove to be radiation hardened as regards static parameters. For the p-channel devices, mobility is less sensitive to irradiation.

The evolution of the threshold voltage shift during irradiation and annealing is shown in fig. 2. By using the subthreshold current stretchout technique [4], we have separated the contributions of the trapped oxide charge (ΔV_{ot}) and of the interface states (ΔV_{it}).

The impact of the annealing at room temperature and under bias on the static parameters of the transistors was almost negligible. On the contrary, we observed significant threshold voltage shift with annealing when all terminals were grounded [1]. Therefore the application of bias even during annealing is important to simulate the realistic behaviour of the transistors.

Table 1: Summary of the static parameters of transistors with W=1000 µm and L=1.4µm before and after irradiation to 12 Mrad and annealing.

	V_{th}[V]	g_m[mS]	µ[cm^2/Vs]
p-channel prerad	-1.31	3.76	200
p-channel 12Mrad	-1.48	3.63	194
p-channel variation	-0.17	-3.4%	-3%
n-channel prerad	0.85	4.12	357
n-channel 12Mrad	0.83	3.41	263
n-channel variation	-0.02	-17%	-26%

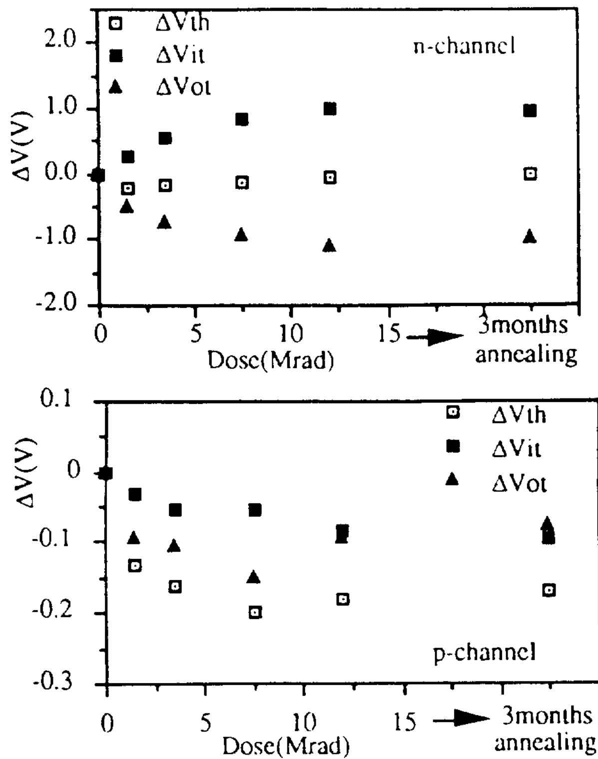

Figure 2: Threshold voltage shift with irradiation and annealing for n- and p-channel transistors with W=1000 μm and L=1.4 μm

B. Noise

The noise of the n- and p-channel transistors can be described by the superposition of three noise contributions which can be studied separately. In addition to the usual 1/f and white noise sources, a localized G-R source is active only under particular bias conditions of the body and backgate. In fig. 3 we show an example in which the different contributions are put in evidence.

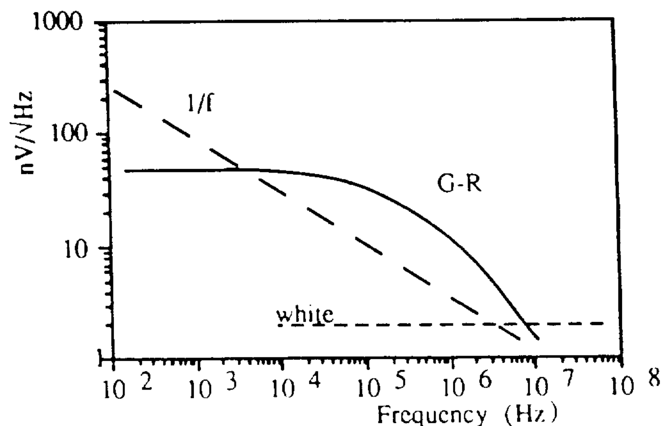

Figure 3: Qualitative noise spectrum of a transistor in saturation showing the superposition of the three different contributions. The G-R term moves depending on the applied body and backgate bias.

The G-R hump changes in frequency and amplitude depending on the backgate and body potentials. We take advantage from this characteristic and move it to lower frequencies when we want to study the white noise, or to higher frequencies when the 1/f region is of major interest.

G-R noise

Generation-recombination noise in MOS transistors is related to the random emission of carriers at defect centers in the depletion region in the semiconductor bulk. The spectrum which describes the G-R contribution, in the case of a single time constant, can be expressed as equivalent noise voltage at the input [5] and depends on the time constant of the emission process τ_t as

$$S_V^2 \propto \frac{\tau_t}{1+\omega^2\tau_t^2} \qquad (1)$$

The time constant τ_t determines the cutoff frequency ($f_{cutoff}=1/2\pi\tau_t$) where the G-R input referred noise is 3dB under the value at the plateau.

This contribution is usually negligible in present bulk technologies, where the defect concentration in the depleted region close to the gate oxide is very low. SOI technologies using SIMOX substrate may nevertheless have relatively high defect concentration in the region of the buried oxide, as shown by a number of studies [6,7,8]. Some of these works have revealed the presence of a monoenergetic defect center. These results are dependent on the particular SIMOX substrate, changing considerably with ion implantation dose temperature, and with annealing temperature.

We have found a G-R noise component in the noise spectra of both p- and n-channel transistors in the HSOI3-HD technology. Its cutoff frequency and amplitude show a strong dependence on the bias condition. In fig. 4 the dependence of the cutoff frequency and amplitude on the backgate potential is depicted for an n-channel transistor. These spectra have been obtained by subtracting the 1/f and white noise contributions from the measured noise curve.

A similar behaviour is found also when changing the body bias. In fig. 5 we show the cutoff frequency and the noise at the plateau of the G-R component as a function of the body potential applied before irradiation. For both n- and p-channel transistors the amplitude of the plateau increases with the absolute value of the body bias while the cutoff frequency in a complementary way decreases. The product of the spectral density at the plateau times the cutoff frequency is fairly constant, which suggests that a constant number of physical defects is involved in the G-R process.

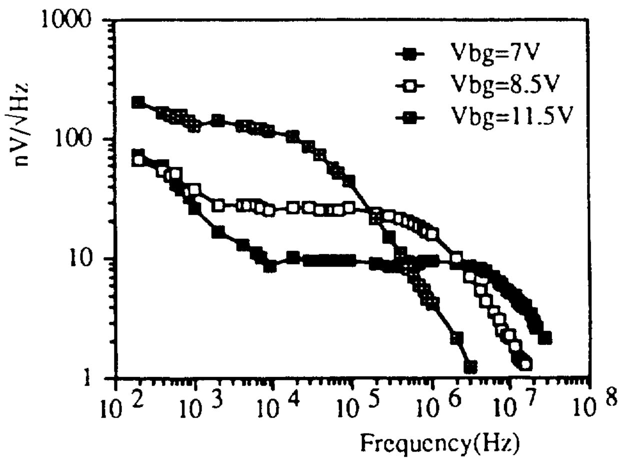

Figure 4: Input referred noise voltage coming from the G-R contribution for different backgate bias. V_{body}=0 V. The cutoff frequency of the G-R hump moves more than two decades with the backgate passing from 7 to 11.5 V. The backgate threshold voltage is 26 V, and the transistor size is W=1000 μm, L=1.4 μm.

Generation-recombination components have been already found in SOS transistors [9], but in that case the variation of the body potential introduced several terms with different time constants. In our measurements we only see one hump, indicating a single time constant phenomenon. A monoenergetic defect in the depleted silicon close to the buried oxide could be at its origin. The time constant of the generation-recombination is inversely proportional to the majority carrier concentration around the defect. By applying a bias to the body or backgate, we modify this concentration at the interface between the buried oxide and the body, therefore the time constant changes.

If the back interface is at the origin of the G-R noise, we have to understand how this noise source is coupled to the source-drain current where we have measured it. In fact, the front channel is the only conductive path between source and drain in our measurements, the back interface being always far from inversion. To investigate the possible mechanism of transmission, we have performed noise measurements in the linear region of operation. In the resulting spectra, the G-R noise was absent for all the backgate or body potentials applied, indicating that the coupling of the noise source to the channel occurs only in presence of the pinchoff.

We have observed that the G-R component is modified by the irradiation. At identical bias conditions, the cutoff frequency is lower after exposure for n-channel transistors and higher for p-channel. At V_{body}=-0.4 V, for the n-channel the cutoff frequency moves from 24 MHz to 4 kHz. For the p-channel at V_{body}=0.7 V, it changes from 5 kHz to 900 kHz. This is a consequence of the backgate threshold voltage shift, which is -6 V for the n-channel and -3.4 V for the p-channel transistors. Owing to this shift, the depletion condition of the back interface is different when the same body and backgate bias are applied. Therefore, the time constant of the generatio-recombination process is modified.

By applying different body bias we can get pre- and post-irradiation spectra with the same cutoff frequency of the G-R noise, and see that the amplitude and shape of the hump is unchanged. This suggests no significant variation in the defect density responsible for this noise.

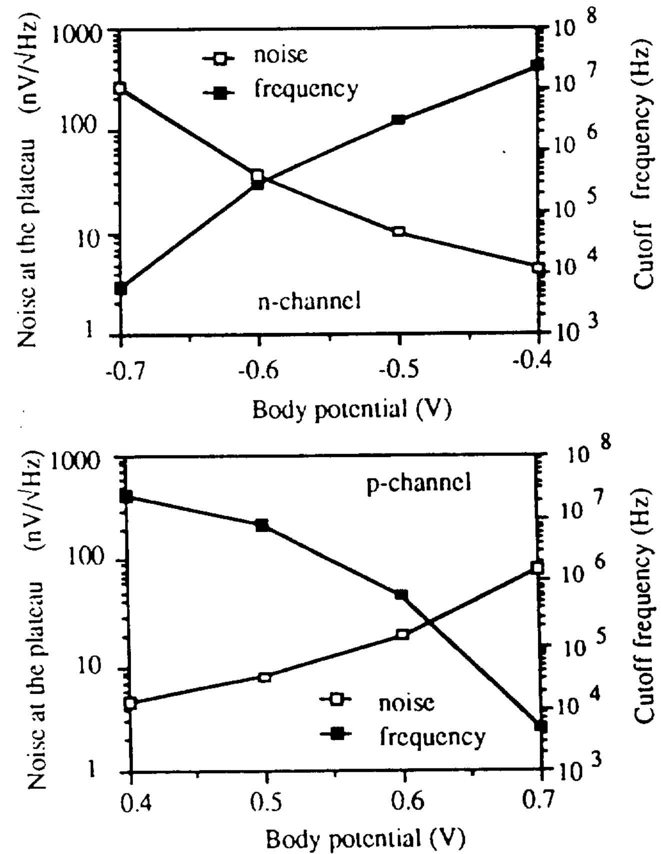

Figure 5: n- and p-channel transistors with W=1000 μm and L=1.4 μm. The noise at the plateau and the cutoff frequency of the G-R component are shown as a function of the body potential applied, with V_{bg}=0 V. The values have been extracted from unirradiated samples.

White noise

The origin of the white noise in MOS transistors can be traced to the random thermal motion of carriers in the channel. In strong inversion and in saturation, the drain current noise can be referred to the input as a noise voltage spectral density with the expression

$$S_V^2 = 4kT\frac{2}{3}\cdot\frac{\Gamma}{g_m} \quad (2)$$

where k is the Boltzmann constant, T the device temperature and g_m the transconductance. The factor Γ is technology and device dependent and has no direct physical meaning, but takes into account several effects. First, it includes the factor 1+δ (where δ depends on the body effect coefficient, the surface potential and the body to source bias) resulting from the different depletion condition close to the source and drain diffusions [10]. Further, it corrects the formula for the reduced mobility at high fields and for the increased carrier temperature. The carriers in the channel being not necessarily in thermal equilibrium with the lattice, T used in (2) could be different from the device temperature. The Γ factor also includes in the simple formulation (2) the white noise contributions coming from the polysilicon gate resistance and the body access resistance. To be more precise, these two additional noise sources should be separately evaluated [11].

In table 2, we report the results of the white noise measurements before and after irradiation. The measured thermal noise is given together with the corresponding g_m and the extracted Γ. The body potential during measurement was -0.7 V for the n-channel and 0.9 V for the p-channel transistors. This bias was applied to move the G-R hump at low frequencies so that the thermal noise was clearly visible in the bandwidth of our measurement setup. The backgate potential was in every case 0 V.

The pre-irradiation Γ is about 10% higher for p-channel transistors. This difference could be due to the contribution of the body access resistance, which we know before irradiation to be higher for the p-channel transistors.

Table 2: White noise, transconductance and Γ factor for n- and p-channel transistors before and after irradiation and annealing. V_{body}=-0.7 V for the n-channel and 0.9 V for the p-channel transistors. V_{bg}=0 V in all cases.

	n-chan. L=1.4µm	n-chan. L=2µm	p-chan. L=1.4µm	p-chan. L=2µm
S_v prerad [nV/√Hz]	1.98	2.02	2.16	2.21
S_v 12Mrad [nV/√Hz]	2.73	2.66	2.50	2.57
ΔS_v	+38%	+32%	+16%	+16%
g_m prerad [mS]	4.58	4.22	4.52	3.90
g_m 12Mrad [mS]	4.00	3.55	4.20	3.60
Δg_m	-13%	-16%	-7%	-8%
Γ prerad	1.63	1.57	1.92	1.72
Γ 12Mrad	2.70	2.27	2.37	2.15
ΔΓ	+66%	+45%	+23%	+25%

After irradiation the situation is reversed. The n-channel transistors reveal a more significant increase in the thermal noise, and they are finally more noisy by 5 to 10% than the p-channel ones. This result is not only justified by a more pronounced reduction of the transconductance, but also by a sharper increase of the Γ factor. This suggests a higher sensitivity to irradiation for one or more of the parameters contained in Γ. It could be the body access resistance or could come from high field effects on the mobility and temperature of the carriers. This last effect is surely important, as shown by the higher increase in Γ for the n-channel transistor with minimum gate length.

1/f noise

According to the McWorther model [12], the 1/f noise in MOS transistors is due to random trapping and detrapping of the mobile carriers in the traps located at the Si-SiO_2 interface and within the gate oxide. It is therefore a direct indication of the quality of the interface, and is very sensitive to trapping states created by irradiation. The noise voltage spectral density referred to the input can be expressed as [13]

$$S_V^2 = \frac{K_f}{C_{ox}^2 WL} \cdot \frac{1}{f^{\alpha}} \tag{3}$$

where C_{ox} is the gate capacitance per unit area, K_f is a technology dependent constant and α is a parameter close to 1.

Using (3) to fit the experimental points, we have extracted the coefficients K_f and α. In table 3 a summary of the results for both channels before and after irradiation and annealing is given.

The coefficient α is less than one for both p- and n-channel transistors, and increases in all cases after irradiation by about 5%. This indicates a creation of slow trapping states as a consequence of the gamma exposure.

The extracted K_f show a big difference between n- and p-channel transistors. The 1/f noise is in fact much lower in p-channel devices. Owing to the doping implant made to adjust the threshold voltage, the p-channel transistor is a buried channel device. It is therefore less sensitive to the Si-SiO_2 interface trap density.

K_f is proportional to the interface trap states density through some coefficient [13, 14]. The increase of K_f can be compared with the static characterization, in particular with the interface states and oxide trapped charge evolution (figure 2). Both the 1/f noise and the static parameter measurements agree that the n-channel transistor interface is more damaged by irradiation. The bias condition during exposure strongly affects this result. The positive voltage

applied to the gate of the n-channel transistor forces the positive species generated by the radiation to move towards the interface. This species is mainly responible for defect formation [15].

Table 3: Extracted 1/f coefficients before and after irradiation and annealing.

	α pre	α 12M	$K_f[fC^2/\mu m^2]$ pre	$K_f[fC^2/\mu m^2]$ 12M
n-chan L=1.4μm	0.88	0.94	$2.53 \cdot 10^{-9}$	$8.33 \cdot 10^{-9}$
n-chan L=2μm	0.88	0.92	$5.38 \cdot 10^{-9}$	$9.13 \cdot 10^{-9}$
p-chan L=1.4μm	0.88	0.92	$4.7 \cdot 10^{-10}$	$1.35 \cdot 10^{-9}$
p-chan L=2μm	0.90	0.96	$7.2 \cdot 10^{-10}$	$2.22 \cdot 10^{-9}$

IV. CONSIDERATIONS FOR ANALOG APPLICATIONS

The static parameter study has revealed that the HSOI3-HD technology is adequate to stand 12 Mrad(Si) ionizing dose with very small changes in its static characteristics. The p-channel transistors have shown to be particulary radiation hardened, having a decrease of mobility and transconductance of about 4% after irradiation and annealing.

For any consideration on the noise behaviour, we should focus our attention on the range of frequencies of interest for our applications. In the LHC experiments, shaping filters will be used to treat the signal coming from the detectors to maximize the signal over noise ratio. These shaping techniques determine the frequencies of interest for the noise.

For ICs to be used in the part of the experiments where radiation hardness is required, a low frequency limit ≥1 MHz is foreseen, sometimes even >5 MHz. At these frequencies, transistor noise should come only from the thermal contribution to get the maximum signal over noise ratio. The corner noise frequency f_{cn}, which is the frequency where the 1/f and white noise contributions are equal, is generally used as the relevant parameter. It is bias dependent, so it is meaningful only when given together with the current level.

1/f noise is of some concern in the studied technology. n-channel transistors of minimum gate length, which have the highest flicker noise after irradiation, present a f_{cn} at about 800 kHz (I_{ds}=500 μA). This means the 1/f contribution is still present, though not dominant, as far as 2 MHz, where it gives 1/3 of the total noise. The p-channel transistors, with f_{cn}≈180 kHz at 500 μA after exposure, could be used even at lower frequencies without being affected by the 1/f component.

The G-R component can considerably increase the noise in the frequency region of interest. Great care should be taken with the body bias of the transistors where low noise is required. The backgate electrode is common to the whole chip, so the body contact is the only means to control the cutoff frequency of the G-R hump. To reduce the high frequency noise, this contribution has to be moved to a low frequency. This can be obtained by applying a body bias. In fig.6 we show the noise spectra for n- and p-channel transistors with an applied body potential of, respectively, -0.9 V and 1.1 V. For the n-channel, the applied bias is sufficient to make the hump disappear at low frequency. For the p-channel, the G-R contribution is moved below 1 MHz, but it is still visible in the depicted spectra, where it completely covers the 1/f noise.

As shown in fig. 6, the noise is determined only by the thermal contribution at frequency >1 MHz for the p-channel transistor and >3MHz for the n-channel when an adequate body bias is applied.

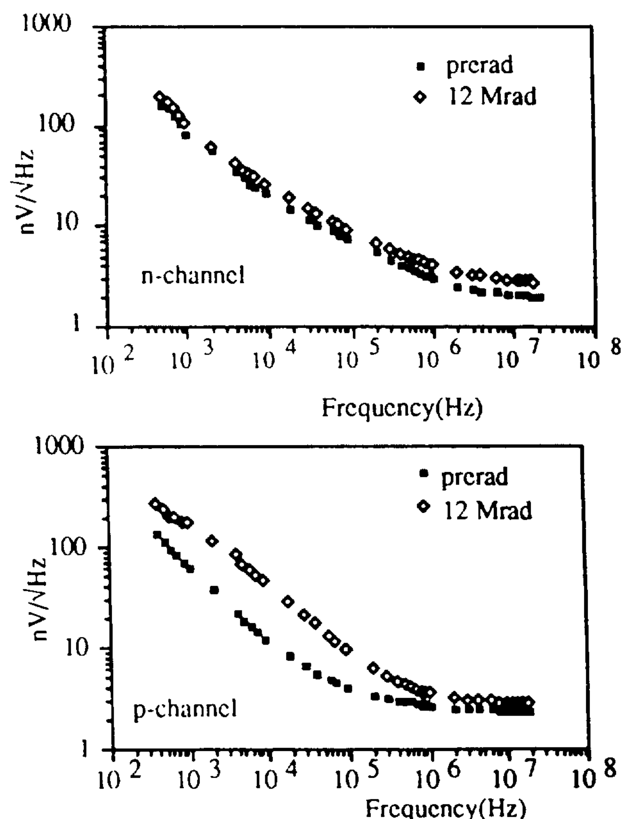

Figure 6: Noise before and after irradiation and annealing for n- and p-channel transistors with W=1000 μm and L=1.4 μm. The body bias applied during measurement was -0.9 V for the n-channel and 1.1 V for the p-channel. V_{bg}=0 V. The 1/f noise of the p-channel is covered by the G-R hump.

V. CONCLUSIONS

Static characteristics of n- and p-channel transistors in the HSOI3-HD technology have been measured before and after irradiation and annealing up to 12 Mrad(Si) from a ^{60}Co source. For n-channel transistors the threshold voltage shift is -20 mV, the transconductance degradation is 17% and the mobility variation is -26%. For the p-channel, we have found ΔV_t=-170 mV and a degradation in both mobility and transconductance of less than 5%.

Noise has been studied in the 500 Hz-25 MHz bandwidth. The spectra reveal the contribution of three noise sources. In addition to the 1/f and thermal noise, which have been fully characterized, a G-R contribution has been found. The noise source responsible for it is located spatially close to the back interface, and can be coupled to the front channel under certain bias conditions. The cutoff frequency of this G-R noise can be changed over a wide range by acting on the body and substrate bias. For the n-channel, a body bias of -0.9 V is sufficient to move the whole G-R contribution below 1 MHz when V_{bg}=0 V, whilst a 1.1 V bias is necessary for the p-channel.

p-channel transistors have lower 1/f noise and are less sensitive to irradiation in the whole explored bandwidth. Their increase in the white noise after 12 Mrad(Si) is about 16% against 35% for the n-channel.

In comparison with bulk radiation hardened technologies in similar studies [16,17], the HSOI3-HD technology performance seems better for both 1/f and thermal noise. In particular, the radiation hardness of the noise characteristics is very good. In addition, SOI technology has low sensitivity to single event phenomena [18]. Therefore, the studied technology is a good candidate for mixed analog-digital applications in harsh environments.

AKNOWLEDGEMENTS

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VI. REFERENCES

[1] F.Faccio et al. "Study of device parameters for analog IC design in a 1.2 μm technology after 10 Mrad", *IEEE Trans. Nucl. Science* NS-39(1992)1739 (Int. Rep.CERN-ECP/92-24)

[2] J.L.Leray et al. "From substrate to VLSI: investigation of hardened SIMOX without epitaxy, for dose, dose rate and SEU phenomena", *IEEE Trans. Nucl. Science* NS-35(1988)1355

[3] J.L.Leray et al., "CMOS/SOI hardening above 100 Mrad (SiO_2)", *IEEE Trans.Nucl.Science* NS-37(1990)2013

[4] P.J.McWorther and P.S.Winokur, "Simple technique for separating the effects of interface traps and trapped-oxide charge in MOS transistors", *Appl.Phys.Lett.* 48(1986)133

[5] L.D.Yau and C.T.Sah, "Theory and experiments of low-frequency generation-recombination noise in MOS transistors", *IEEE Trans.El.Devices* 16(1969)170

[6] W.E.Carlos, "Paramagnetic centers at Si-SiO_2 interfaces in silicon-on-insulator films", *Appl. Phys. Lett.* 50 (1987), 1450

[7] T.J.Ennis et al, "The effect of implantation temperature on defect production in SIMOX structures", *Semicond.Sci.Technol.* 4(1989)626

[8] P.K.McLarty and D.E.Ioannou, "Deep states in silicon-on-insulator substrates prepared by oxygen implantation using current deep level transient spectroscopy", *Appl.Phys.Lett.* 53(1988)871

[9] P.Gentil et al. "Low frequency noise measurements on silicon-on-sapphire (SOS) MOS transistors", *Solid-State Electronics* 20(1977)935

[10] Y.P.Tsividis, *Operation and modeling of the MOS transistor*, New York, McGraw-Hill, 1988

[11] S.Tedja et al, "Noise spectral density measurements of a radiation hardened CMOS process in the weak and moderate inversion", *IEEE Trans.Nucl.Science* NS-39(1992)804

[12] A.L.McWorther, *Semiconductor surface physics*, Philadelphia, Univ. Pennsylvania Press, 1956, pp.207-227

[13] Z.Y.Chang and W.M.C.Sansen, *Low noise wide-band amplifiers in bipolar and CMOS technologies*, Leuven, Kluwer academic publishers, 1991

[14] G.Ghibaudo, "A simple derivation of Reimbold's drain current spectrum formula for flicker noise in MOSFETS", *Solid-State Electr.* 30(1987)1037

[15] G.C.Messenger and M.T.Ash, *The effects of radiation on electronic systems*, New York, Van Nostrand Reinhold publisher 1992

[16] W.Dabrowski et al, "Noise measurements on radiation-hardened CMOS transistors", *IEEE NSS*, Santa Fe, november 5-9 1991, vol.3, pag.1536

[17] S.L.Thomas et al, "Measurements of a radiation hardened process: Harris AVLSIRA", *Nucl.Instr.Meth.* A342(1994)164

[18] O.Musseau et al, "SEU in SOI SRAMS- a static model -", to be published in *IEEE Trans.Nucl.Science* NS-41(1994)

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A Fast, Low Power CMOS Amplifier on SOI for Sensor Applications in a Radiation Environment of up to 20 Mrad(Si).

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Abstract

The design and measurements of a 0.5mW CMOS current mode amplifier in a SOI radiation hard technology are reported for a total dose of 20Mrad(Si). It is designed for the fast readout of particle detectors in high energy physics experiments but could equally be applied to the readout of any capacitive sensor in a radiation environment. A pre-irradiation gain of 43.3mV/4fC, rise time of 17nS and Equivalent Noise Charge (ENC) of 1436e$^-$ + 78e$^-$/pF (1.97nV(Hz)$^{-1/2}$) is achieved. Measurements are reported at 0, 10Mrad(Si) and 20Mrad(Si) with the evolution showing changes in peak voltage, rise time, parallel noise and series noise of -23%, 26%, 23% and 60% respectively after 20Mrad(Si).

I. INTRODUCTION

Low power, high speed analog circuits are becoming desirable for many applications including those that have the added requirement of being resistant to radiation.

This amplifier has been developed in the framework of future high energy particle physics experiments at the Large Hadron Collider (LHC) in CERN. A typical experiment at the LHC will involve millions of detecting elements each with its own VLSI amplification and signal processing electronics. Detector signals will be processed in real time with an event frequency of 40MHz. All the detectors and electronics will be contained within a confined space, hence the power consumption requirements are stringent to minimise cooling.

The expected radiation environment will be 10-20 Mrad(Si) of ionising radiation over a 10 year period and a neutron flux of 2×10^{13} cm^{-2} year^{-1} [1]. The main concern for a CMOS circuit is the effect of ionising particle induced radiation damage [2,3] and hence forms the basis of this study.

In this paper we present the concept of the Cascoded Grounded Gate Amplifier (CGGA) which provides a high gain bandwidth product at a very low power consumption. It is designed to operate in the harsh radiation environment of the LHC and we present the amplifier performance before and after gamma radiation exposure.

The technology used in this design is the HSOI3HD 1.2-µm CMOS SOI process from Thomson TCS. The analog performance of this technology has been extensively studied. Threshold voltage (V_t) shifts of -170mV and -20mV, and g_m degradation of 4% and 17% for p and n channel transistors respectively have been reported for 12Mrad(Si) of ionising radiation [4].

II. THE CGGA AMPLIFIER DESIGN

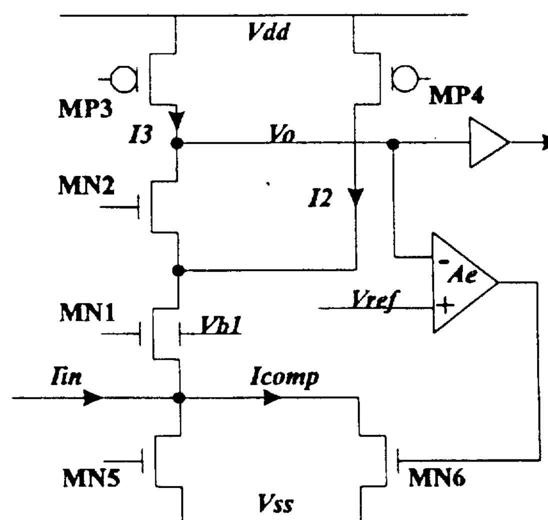

Fig. 1 The Cascoded Grounded Gate Amplifier (CGGA)

The proposed CGGA amplifier is shown in Figure 1. It consists of the grounded gate input MOSFET MN1, the cascode stage MN2 and the current sources MP3, MP4 and MN5 . The output node V_o acts as an integrating node of capacitance C_o. The slow speed error amplifier (Ae) ensures a stable DC potential of the output node and defines a discharge time constant of C_o through the controlled current source MN6. The technique also provides self adjustment for the effect of the sensor dark current, which becomes significant as the total dose accumulates. Detector leakage

currents of up to 20μA can be compensated for, enabling a DC connection to the sensor. This, in turn reduces the processing cost of the detector.

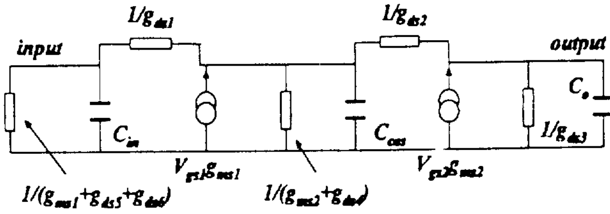

Fig.2 The small signal model for the CGGA.

The small signal model for the CGGA is given in figure 2 where g_{ms} is source transconductance, g_{ds} is drain-source conductance and V_{gs} the gate-source voltage of the respective transistors. The capacitances are defined as follows:

$$C_{in} = C_{sen} + C_{gs1} + C_{gd5} + C_{gd6} \quad (1)$$

$$C_{cas} = C_{gd1} + C_{gs2} + C_{gd4} \quad (2)$$

$$C_o = C_{gd2} + C_{gd3} + C_l \quad (3)$$

where C_{gs} and C_{gd} are the gate-source and gate-drain capacitances, C_{sen} is the capacitive load of the sensing element on the input and C_l the total load capacitance of the analog output buffer and error amplifier.

The current sources are designed to give a very small drain source conductance whilst keeping their drain capacitance to a minimum. In this way their effect becomes negligable for the first two time constants. The three time constants now reduce to :

$$\tau_{in} = (C_{gs}+C_{sen})/g_{ms1} \quad (4)$$

$$\tau_{cas} = (C_{gd1}+C_{gs2})/g_{ms2} \quad (5)$$

$$\tau_o = C_o/g_{ds3} \quad (6)$$

The charge gain of the amplifier $1/C_o$ is defined as the ratio of the output pulse amplitude divided by the input charge. The gain-bandwidth product (GBW) of the CGGA amplifier is determined by the source transconductance (g_{ms1}) of MN1 and the capacitance of the output node C_o. To obtain a high GBW at low power consumption, g_{ms1} must be large and C_o small.

The grounded gate device MN1 has W_1/L_1= 1500μm/1.4μm in order to operate in weak inversion with drain currents that satisfy (7).

$$I_d < 2n\mu C_{ox}(W/L)\, U_T^2 \quad (7)$$

Where U_T is the thermal voltage given by kT/q and n is a process dependant factor that relates to the weak inversion slope [6]. With a drain current of 80μA MN1 is deeply in weak inversion at room temperature. In this region of operation $g_{ms1} = I_d/U_T$ which maximises the ratio g_{ms}/I_d and hence achieves optimum power consumption. The input impedance is $1/g_{ms1}$ and in turn gives the fastest possible input time constant for a given detector capacitance.

The current source MP4 reduces the bias current in the output load MP3 by a factor five. This allows the output node capacitance C_o to be kept small by minimising the drain area of MN2 and MP3. Thus, C_o as low as 30fF can be obtained in a CMOS 1.2μm SOI process.

The chip consists of 12 channels each with vertical pitch of 100μm and length 800μm. Including the pads the total surface area is 7.9mm². Figure 3 is a photograph of the chip.

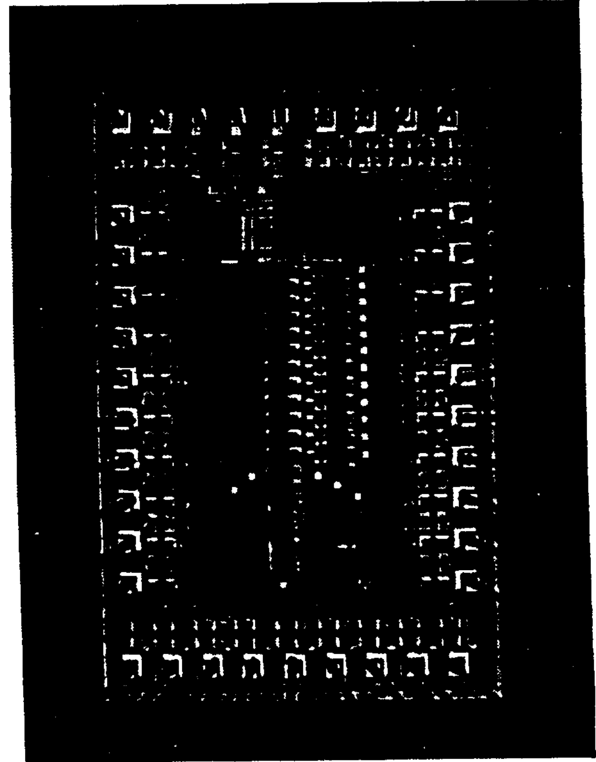

Fig.3 A photograph of the 12 channel CGGA chip.

III. NOISE ANALYSIS

The noise in an SOI device of the studied technology consists of three main components, namely white noise, 1/f noise and Generation Recombination (G-R) noise.

The white noise (or channel thermal noise) is due to the random thermal motion of the free carriers in the channel of a MOSFET. The channel can be approximated to a simple resistor [7] and its thermal noise behaviour can be expressed either as a series voltage source given by (8), or a parallel current source (9) where the equivalent noise resistance is given in (10). The white noise is therefore increased after irradiation due to both a reduction in g_m and to the increase of the Γ coefficient. The values for the various coefficients before and after irradiation can be found in [4].

$$e_n^2 = 4kTR_n \qquad (8)$$

$$i_n^2 = 4kT/R_n \qquad (9)$$

$$R_n = (2/3)\Gamma/g_m \qquad (10)$$

The 1/f noise has a noise spectral density as given in (11) where K_f is the flicker noise coefficient and α, a parameter close to 1.

$$e^2_{1/f} = K_f/(C_{ox}{}^2 WLf^{\alpha}) \qquad (11)$$

Both K_f and α are increased after irradiation with α becoming even closer to the unity value.

The G-R noise appears as a hump in the transistor noise spectrum [4]. The significance of the G-R noise source depends upon the frequency of operation and the bias applied to the transistor body. Careful adjustment of the body potential can move this hump out of the required bandwidth. The input transistor MN1 is therefore designed with an external body connection to allow for a compensating variable potential.

The Equivalent Noise Charge *(ENC)* of the system is expressed in terms of the equivalent parallel ($i_{n\,p}^2$) and series ($e_{n\,s}^2$) noise sources that would be required at the input in order to produce the observed noise at the output as shown in figure 4 [10].

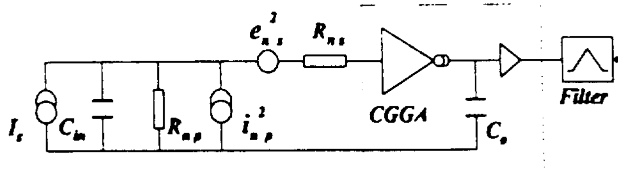

Fig. 4 : The Noise model of the CGGA and filter .

The series component of the *ENC* is almost entirely due to the effect of the input transistor MN1 and is given in (12).

$$ENC^2_s = (e_{n\,s}^2 C_{in}^2)/t_m \qquad (12)$$

Where the thermal noise contribution ($e_{n\,s}^2$) can be found from (8) and (10) using g_{ms1}. C_{in} is the total capacitance seen at the input and t_m is the rise time after the filter.

The parallel component of the ENC (13) is mainly due to the channel thermal noise of the current sources MP3, MP4, MN5 and MN6.

$$ENC^2_p = (1/3)(i_n^2\, t_m) \qquad (13)$$

i_n^2 can be found using equations (9) and (10) where R_n in (9) is the sum of the 4 noise resistances in parallel .

The 1/f contribution ($ENC^2 f$) can be found from (14) assuming α to be close to 1 [8,9]

$$ENC^2 f = (K_f C^2 / C^2_{ox} W_l L_l\, 2\, n)(n!^2 e^{2n} / n^{2n}) \qquad (14)$$

where n is the order of the filter. The significant parameter affected by irradiation for the 1/f noise of the circuit is therefore K_f. Even allowing for the increase in K_f after irradiation the calculation reveals a contribution to the *ENC* of less than 1% compared to the white noise and hence can be neglected.

Using the parameters given in [4] the above analysis results in an expected pre-irradiation parallel noise of 985e and a series noise of 95e/pF which corresponds to 2.4 nV(Hz)$^{-1/2}$. After 12Mrad(Si) the theoretical prediction is 794e + 131.5e/pF or 3.3 nV(Hz)$^{-1/2}$.

IV. EXPERIMENTAL CONDITIONS

A total of ten chips were irradiated, five at 10Mrad(Si) and five at 20 Mrad(Si) using a ^{60}Co source. The exposure was over a 76 hour period giving dose rates of 133Krad(Si)/hour and 266Krad(Si)/hour.

The results reported here represent the mean values taken from complete measurements of all ten chips. The measurements were taken 2 days after the irradiation and both the irradiation and the measurements were carried out at room temperature. The transistor characteristics are dependant upon the bias applied during exposure and also during any annealing period. For this reason all the chips were biased in an operational mode during and after the irradiation process.

The bias currents were kept constant for all measurements. In an operational environment one could perhaps consider increasing bias currents slightly in order to compensate for transconductance degradation.

The noise measurements were taken after a 25ns shaping through a CR/RC^2 filter. This is then equivalent to sampling the signal at the LHC clock frequency. The parasitic loading

capacitance of the package and measurement board on the input of the amplifier was measured to be a minimum of 7pF. The parallel noise contribution was taken using a linear fit to the measured data considering both the contribution of the board and package plus 1.1pF as calculated for the inherent source capacitance of MN1.

V. MEASUREMENTS BEFORE AND AFTER IRRADIATION.

A 300μm thick silicon detector releases approximately 25000 electrons (4fC) when traversed by a minimum ionising particle (mip). The CGGA signal response for an equivalent input signal of 1 mip is shown in figure 5. It shows a peak voltage of 43.3mV/mip with 80% of the signal response given in 17ns. The peak is maintained at more than 96% of the signal response during a 25ns window and hence becomes very robust with respect to uncertainties related to the sampling time. The spread of the samples taken show a standard deviation of 1.8% providing confidence in the matching of process parameters across the wafer.

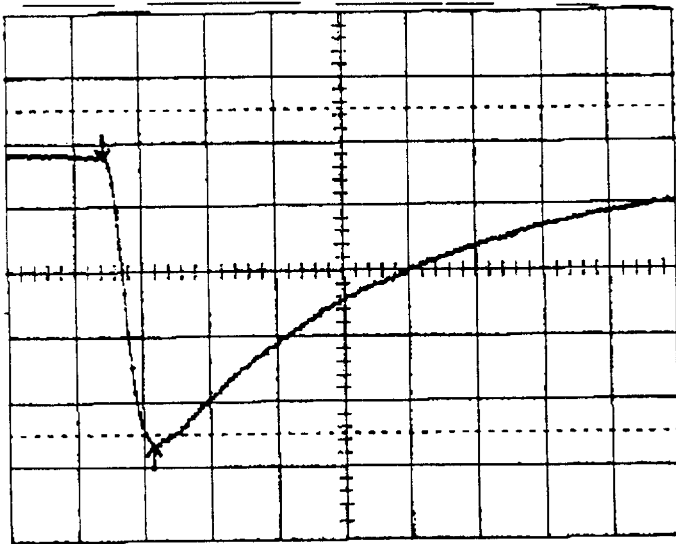

Fig. 5 : Signal response from the CGGA to a 4fC input signal. The scale is 50ns/div. and 10mV/div. on the horizontal and vertical axis respectively. The peak voltage is 43.3mV with a rise time of 17ns.

The decay of the response is determined by the impedance of the integrating node V_0. Here the decay is designed to reduce to a minimum the error introduced by timing uncertainties whilst avoiding potential problems due to pile up. Figure 6 shows the signal response for positive and negative input signals of 4fC. The decay can be seen to be complete after 750ns.

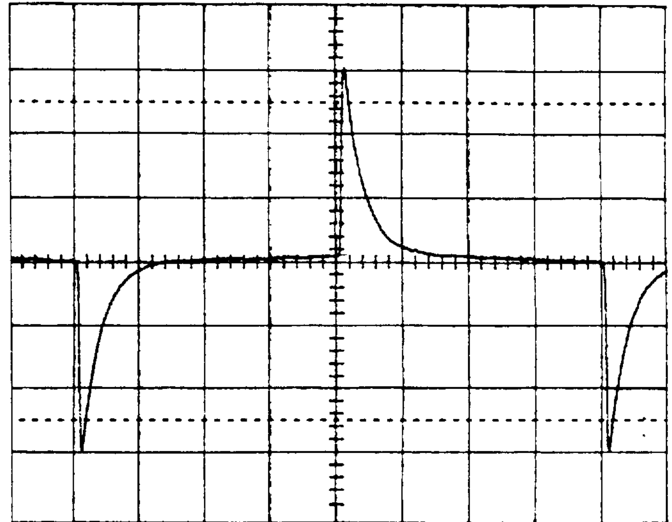

Fig. 6: Signal response for positive and negative input signals of 4fC. The scale is 500ns/division and 14mV/division on the horizontal and vertical axis respectively. The decay is complete after 750ns.

After exposure the signal shape from the CGGA is very well preserved. The peak voltage is degraded initially by 23% and then remains stable. The rise time, measured as the time taken to achieve 80% (10% - 90%) of the peak value, increases from 16.7ns to 21.5ns after 20Mrad(Si). Figure 7 shows the effect of the irradiation on the peak value and rise time.

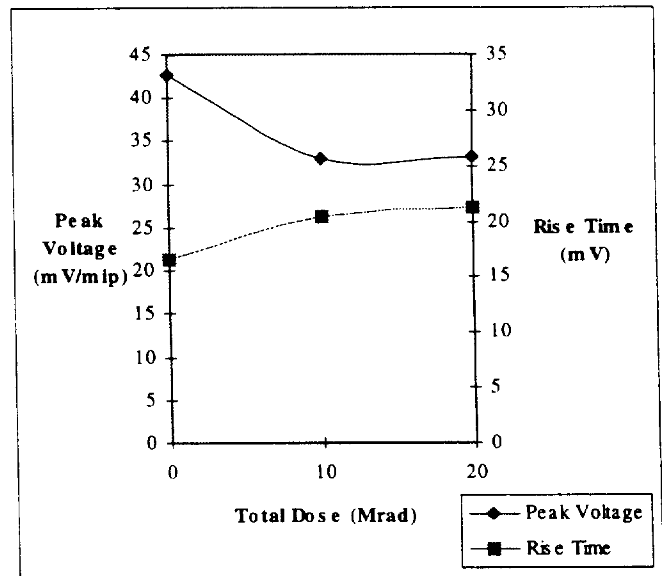

Fig. 7: Evolution of the peak voltage and rise time for an input signal of 4fC with irradiation.

Figure 8 shows the noise slope before and after irradiation. The pre-irradiation result is an Equivalent Noise Charge (ENC) of 1436 e^- + 78e^- /pF (rms) which corresponds to approximately 2nVHz$^{-1/2}$. After 10Mrad(Si) there is an increase in the parallel noise of approximately 23% whilst the series noise increases by nearly 60%. The degradation thereafter is small and only apparent in the parallel noise, increasing by a further 9%.

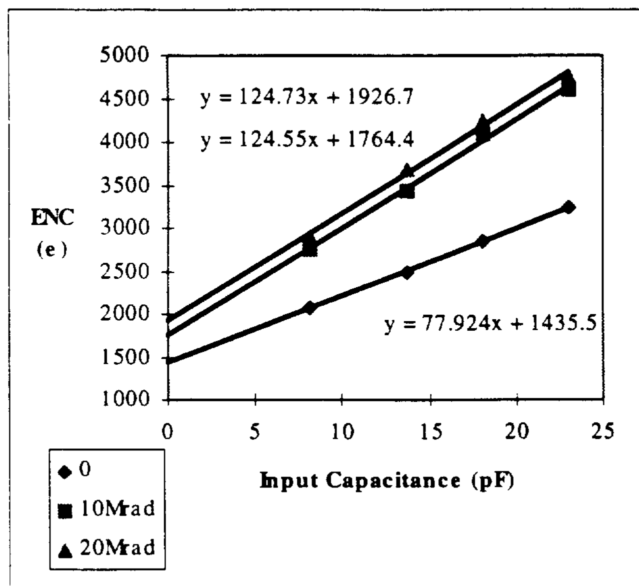

Fig. 8: The noise performance after 0, 10Mrad(Si) and 20 Mrad(Si).

The measured result compares well to the theoretical prediction with respect to the series noise but the parallel component is significantly higher both before and after irradiation. The result for the series noise would suggest that the parameters used for the prediction of effects under irradiation are good. A larger than expected value for C_{in} could account for the discrepancy in the parallel noise.

VI. CONCLUSION

The design and fabrication of an amplifier for particle detector readout at the LHC has been achieved. Results have been shown for a total dose of a 0, 10Mrad(Si) and 20Mrad(Si) of gamma radiation using a ^{60}Co source and are summarised in Table 1.

The majority of the radiation effect is apparent within the first 10Mrad(Si) with only a small change thereafter. Satisfactory operation at higher levels of total dose would therefore seem probable but further study would be needed to confirm this.

	0	***10Mrad(Si)***	***20Mrad(Si)***
Peak Voltage /4fC	43mV	33mV	33mV
Rise Time	17nS	20.5nS	21.5nS
Parallel Noise (ENC)	1436 e^- rms	1764 e^- rms	1926 e^- rms
Series Noise (ENC)	78 e^- / pF rms	124.6 e^- / pF rms	124.7 e^- / pF rms

Table 1: Measured performance of the CGGA 0, 10Mrad(Si) and 20Mrad(Si) of ionising radiation.

For LHC, the signal response remains fast enough and with sufficient gain to operate continuously at 40MHz throughout its proposed 10 year life cycle. The noise, whilst satisfactory for low capacitive sensors could be reduced further in order to cope with larger detectors.

VII. ACKNOWLEDGEMENTS

We would like to thank M. Campbell and F. Anghinolfi for much useful discussion on the noise behaviour.

VIII. REFERENCES

[1] G.R. Stevenson, A. Fasso, *The Radiation Field in and around Hadron Collider Detectors*, IEEE Trans. NS-39 (1992) 1712

[2] G.C.Messenger,M.S.Ash, *The Effects of Radiation on Electronic Systems*, New York,Van Nostrand Reinhold, 1992

[3] Jean-Pierre Colinge, *Silicon-on-insulator Technology, Materials to VLSI*, Kluwer Academic Publishers.

[4] F. Faccio, M.Bianchi, M.Fornasari, E.H.M.Heijne, P.Jarron, J. Redolfi, G.Rossi, G.Borel: *Noise characterization of transistors in a 1.2μm CMOS-SOI technology up to a total dose of 12 Mrad(Si)*. IEEE trans. NS41 (1994) 2310

[5] Y.P. Tsividis, *Operation and modelling of The Mos Transistor*, Mc Graw Hill, 1988

[6] E. Vittoz, *CMOS VLSI Design course notes* ,EPFL Lausanne 1989.

[7] Grey, Meyer, *Analysis and design of analog integrated circuits*.Wiley, p639, 1977

[8] Chang/Sansen, *Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies*, Kluwer, 1991

[9] Chang/Sansen, *Effect of 1/f noise on the resolution of CMOS analog readout systems for microstrip and pixel detectors*. Nucl. Inst. & Methods A 305 1991

[10] Radeka, *Signal, noise and resolution in position-sensitive detectors*, IEEE trans. on Nuclear Science Vol. 21 1974

Analog Performance of SOI MOSFETs up to 25 Mrad (Si)

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Abstract

We have studied the analog performance of the HSOI3-HD technology (industrialized by Thomson TCS, St.Egrève, France) up to a total dose of 25 Mrad of ionising radiation. Static parameters and their evolution have been extracted, and particular attention has been devoted to the noise. We found that most of the damage occurs in the first 12 Mrad, so the technology can find applications where tens of Mrad total doses are foreseen. p-channel transistors should be chosen as key elements in low noise ICs, with a maximum degradation of 18% in transconductance and better 1/f noise performance. A Generation–Recombination component in the noise spectra can be controlled through the body bias. We have studied the energy level of the trapping centers responsible for it and found that it is not modified by the irradiation.

I. Introduction

Complex ICs for analog and digital signal processing in experiments at the Large Hadron Collider (LHC) will require radiation hardness up to a level of 10 to 100 Mrad. In view of this application, we have studied in previous work [1, 2] the noise and static parameter evolution of the HSOI3-HD CMOS-SOI technology after 12 Mrad. The results showed that, with careful bias of the key transistors for noise considerations, the technology can be used to implement analog functions still correctly working after that total dose.

It has been found (e.g. [3]) that there is a saturation effect of the radiation damage after a total dose varying with the technology. In this work, we have studied the analog behaviour of the HSOI3-HD up to 25 Mrad to see if there is any saturation effect, in order to understand whether the technology is suitable for application in the inner parts of the LHC experiments, where doses higher than 10 Mrad are expected.

We previously reported the presence of a Generation–Recombination component in the noise spectra. With the noise versus temperature technique we have now determined the energy level of the trapping centers responsible for it. A more detailed study of its evolution with the total dose is also presented, showing that it is not modified by the irradiation.

II. Experimental Details

The HSOI3-HD technology is a 1.2 µm polycide gate CMOS-SOI process manufactured by Thomson TCS on SIMOX substrate, and it has been described in our previous works and in [4]. Thickness of the gate oxide, silicon body and buried oxide are respectively 23 nm, 150 nm and 380 nm. The transistors can be fully depleted under particular bias conditions (medium thickness devices following the classification in [5]).

Wide transistors (W=1000 µm) have been used to maximise the drain noise, reduce the thermal equivalent input voltage noise density and study the 1/f contribution with better precision. The minimum gate length has been chosen in the study (L=1.4 µm) in view of noise optimisation in analog applications. The MOS-SOI transistors we studied were actually five-terminal devices. We define as "backgate" the substrate electrode (common to the whole chip) and as "body" the silicon film under the gate oxide, accessible separately for every transistor via a lateral contact.

Gamma irradiation took place with a calibrated ^{60}Co source at room temperature at a dose rate of 91 rad/sec. The transistors were kept under bias (diode configuration with Ids=200 µA, chosen as most realistic for analog applications) both during the 76–hours irradiation and the subsequent room temperature annealing.

Extraction of the static parameters was performed with an HP4145B* semiconductor parameter analyser. The noise measurements were made with the device in saturation (V_{ds}=800 mV, V_{gs}-V_t=300 mV)) and a constant source-drain current density of 0.5 µA/µm. The drain current noise was amplified by a transimpedance amplifier and a voltage gain stage, then measured by an HP3588A spectrum analyser. In this configuration the noise was expressed as equivalent noise voltage referred to the gate, and could be measured over the 500 Hz–25 MHz bandwidth.

III. Results and Discussion

A. *Static parameters*

The threshold voltage shift as a function of total dose is depicted in figs.1 and 2 for n- and p-channel transistors. The

contributions of interface states and oxide trapped charge are shown separately. The prerad threshold voltage for p-channel transistors is about -1.3 V, whilst it is 900 mV for the n-channel. These values were extracted with the back interface in accumulation. Room temperature annealing under bias does not change the threshold more than about 50 mV. The shift in threshold of the p-channel transistors after a 25 Mrad irradiation, though limited to -360 mV, leads to a relatively high threshold voltage. This imposes a power supply of at least 3.5 V.

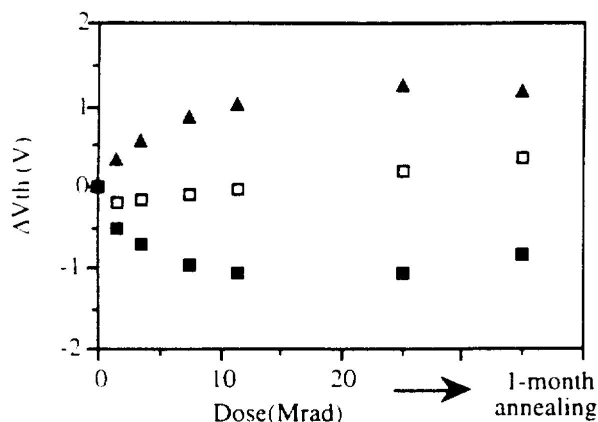

Figure 1: Threshold voltage shift for n-channel transistors. Empty squares represent the overall shift, which is due to the contributions of trapped oxide charge (black squares) and interface states (black triangles).

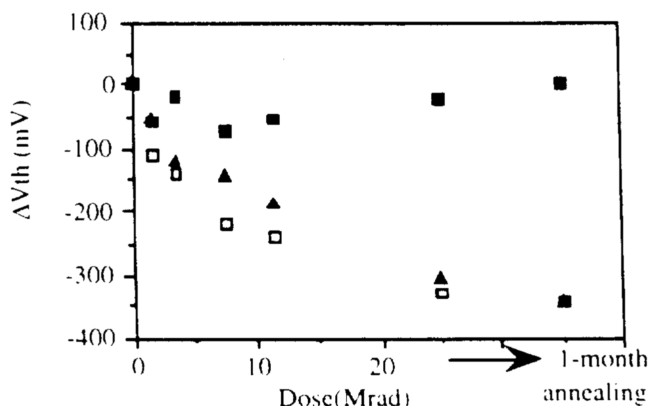

Figure 2: Threshold voltage shift for p-channel transistors. Empty squares represent the overall shift, which is due to the contributions of trapped oxide charge (black squares) and interface states (black triangles).

For analog applications, a useful expression of the technology performance is the plot of the scaled transconductance (g_m/I_{ds}) as a function of the drain current density. It shows clearly the transconductance degradation in weak, moderate and strong inversion. Figs. 3 and 4 show the result for a 25 Mrad irradiation relative to the particular processing batch under study.

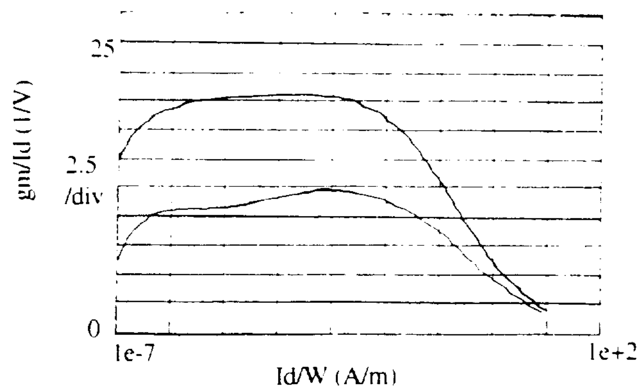

Figure 3: n-channel scaled transconductance decreases after the 25 Mrad irradiation by about 44% in weak, moderate and strong inversion.

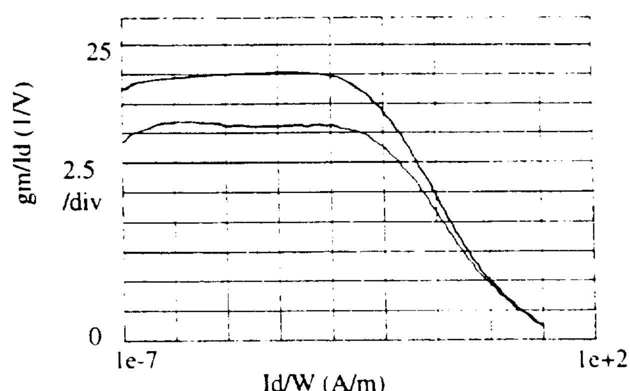

Figure 4: p-channel scaled transconductance decreases by 18% in weak inversion after 25 Mrad. In moderate and strong inversion the degradation is even lower.

The maximum degradation in transconductance for p-channel transistors occurs in weak inversion, with a variation of –18%. For the n-channel transistors the degradation is about –44% in both weak and strong inversion. This difference in the radiation hardness is mainly due to two reasons. First, the positive bias applied to the n-channel transistor during irradiation and annealing worsens the effect of the charge migration in the gate oxide. Secondly, the p-channel transistor in the studied technology is a buried channel device. Therefore it is less sensitive to interface damage effects. This is confirmed by the results on the 1/f noise, as shown further on.

In all measurements the leakage current was limited to some tens of pA, showing no formation of lateral leakage paths between source and drain. This is important for analog applications involving switched capacitor circuits (ADCs, analog memories, feedback capacitor reset switches), and it is a major failure mechanism for standard commercial technologies exposed to ionising radiation.

B. Noise

The analog frontend electronics of high energy physics experiments widely uses amplifiers and shapers, and noise is referred to the input as Equivalent Noise Charge (ENC) [6]. The noise characteristic of a technology ultimately determines the sensitivity of these analog circuits at a given power consumption, therefore it is essential that the designer has good measurements of the noise.

The relative impact of white and 1/f noise on the noise performance of amplifier circuits can be influenced via the shaping time chosen. Generally speaking, the white noise component dominates for short shaping times, like those foreseen in LHC experiments (25 ns). This might not be true for radiation-hard technologies, which may have 1/f component dominant up to 1 MHz or more, especially after irradiation. Therefore the evolution of the noise in the whole frequency spectrum must be studied in detail.

Three different contributions build up the noise spectrum of transistors in the technology studied: white noise, 1/f noise and G-R noise. In the following sections, we will treat each of them separately.

Typical noise for n- and p-channel transistors is shown in figs. 5 and 6.

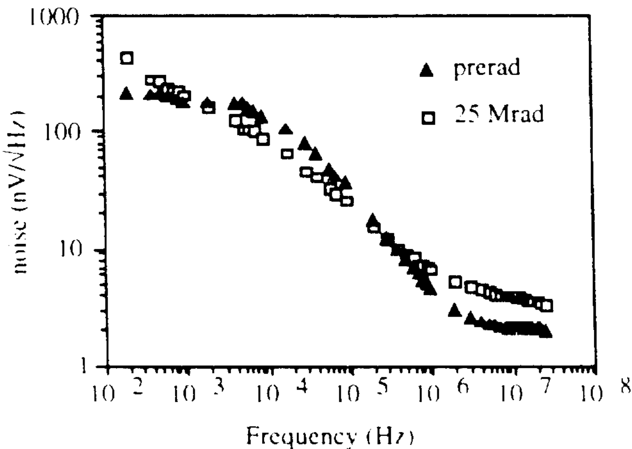

Figure 5: Noise spectra of an n-channel transistor before and after 25 Mrad and annealing for V_{body}=-0.9 V. In both the G-R hump shows up in the tens of kHz region, therefore the 1/f noise is not clearly visible, or even completely hidden in the prerad case. The white noise after irradiation is not well distinguishable either.

The G-R hump can be moved widely in frequency by applying a body potential, but the layout of the studied structures did not allow us to use body biases higher than ±0.9 V. A higher bias would make the hump disappear under the dominant 1/f noise, which is not the case in figs. 5 and 6. After irradiation the white noise is not really distinguishable in the spectra, and we have not yet found an explanation for this phenomenon which occurred in transistors of this particular processing batch. Nevertheless we have reported in the next section white noise figures even after irradiation. Those values were extracted at a frequency of about 20 MHz in order to give a reference number.

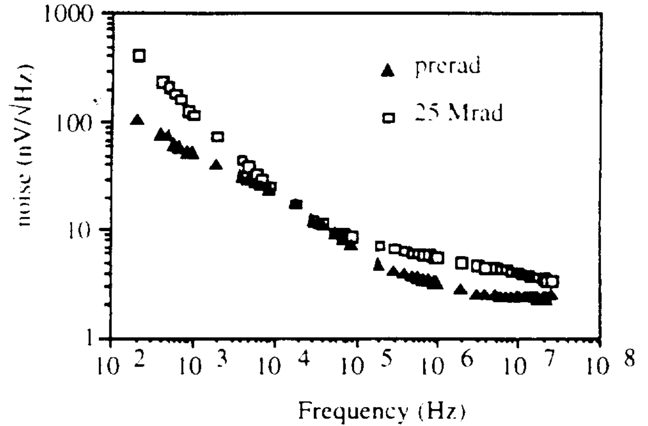

Figure 6: Noise spectra of a p-channel transistor before and after 25 Mrad irradiation and annealing for V_{body}=0.9 V. In the prerad curve, the G-R hump is visible around 20 kHz and partially covers the 1/f noise. The level of white noise is well defined only before irradiation.

White noise

In strong inversion and in saturation, the noise from the drain current can be referred to the input as a noise voltage spectral density with the expression

$$S_V^2 = 4kT\frac{2}{3}\cdot\frac{\Gamma}{g_m} \qquad (1)$$

where k is the Boltzmann constant, T the device temperature and g_m the transconductance. The factor Γ is called excess noise factor, is dependent on technology and device and has no direct physical meaning. In table I the values of the thermal noise, transconductance and the extracted Γ are given for n- and p-channel transistors before irradiation, after 12 Mrad and annealing and after 25 Mrad and annealing.

The transconductance refers to the transistor in the same condition as in the noise measurement. Γ increases more in the p-channel devices, but the lower decrease in transconductance makes the equivalent input noise almost equal after irradiation for n- and p-channel transistors. Therefore p-channel transistors are still preferable as they perform at higher speed at the same current and noise.

Table I: white noise, transconductance and excess noise factor before irradiation and after 12 and 25 Mrad.

	n-channel	p-channel
S_v pre [nV/√Hz]	1.96	2.25
S_v 12M [nV/√Hz]	3.10	3.14
S_v 25M [nV/√Hz]	3.19	3.29
g_m pre [mS]	4.28	4.22
g_m 12M [mS]	2.98	4.19
g_m 25M [mS]	2.67	3.82
Γ pre	1.48	1.92
Γ 12M	2.58	3.72
Γ 25M	2.45	3.73

1/f noise

The 1/f noise voltage spectral density referred to the input can be expressed as [7]

$$S_V^2 = \frac{K_f}{C_{ox}^2 WL} \cdot \frac{1}{f^\alpha} \qquad (2)$$

where C_{ox} is the gate capacitance per unit area, K_f is a technology dependent constant and α is a parameter close to 1.

K_f is an important technology dependent parameter. It must be as low as possible because it determines the minimum noise of the circuit when the shaping time is such that 1/f component has a significant contribution. This parameter should be extracted from the measured points. In table II we have reported the extracted K_f and α parameters for n- and p-channel transistors. The 1/f noise is much lower for the p-channel transistors, as expected.

Table II: Extracted 1/f coefficients before and after irradiation at 12 and 25 Mrad.

	n-channel	p-channel
α pre	0.88	1.02
α 12Mrad	0.92	1.04
α 25Mrad	0.94	1.00
K_f pre [$fC^2/\mu m^2$]	$2.83 \cdot 10^{-9}$	$1.37 \cdot 10^{-9}$
K_f 12M [$fC^2/\mu m^2$]	$16.82 \cdot 10^{-9}$	$5.61 \cdot 10^{-9}$
K_f 25M [$fC^2/\mu m^2$]	$20.79 \cdot 10^{-9}$	$6.90 \cdot 10^{-9}$

G-R noise

Generation-recombination (G–R) noise in MOS transistors is due to random emission of electrons and holes at defect centers in the depletion region of the semiconductor. An extensive theoretical and experimental work on the subject has been done by Yau and Sah [8], who gave an analytical expression to calculate the noise in bulk transistors in saturation. The G–R power spectrum has a plateau and a steep $1/f^2$ region, and is characterised by a cutoff frequency (that is the frequency where the G–R input referred noise is 3dB under the value at the plateau).

We have found a G–R component in the noise of the HSOI3–HD transistors. It is visible in the noise spectra as a hump superposed on the 1/f and white noise, and moving in frequency and amplitude when the bias of the body or backgate is modified and when the temperature is changed. We believe the origin of this component is the trapping–detrapping of carriers in a localized defect center in the bulk of the semiconductor film, probably close to the buried oxide.

In the Yau and Sah formulation, the time constant of the G–R process and the fraction of occupied or inoccupied traps have a strong dependence on temperature and on the energy level of the traps in the gap compared to the intrinsic Fermi level. In the SOI transistor, a change of body or backgate potential changes the relative position of the energy levels in the depletion region, thus modifying the G–R spectrum. The temperature as well influences the noise value at the plateau and the cutoff frequency.

To determine the energy level of the G–R defect centers, we have used the noise versus temperature (NVT) technique. This technique has already been used, in particular with low frequency noise measurements, to study shallow defects in MOSFETs and it has been compared to DLTS with success. For a description of the technique, see [9] and [10].

We have applied the NVT technique to study the noise of n-channel transistors, which show a greater influence of the G–R component. Temperature varied between -7°C and +50°C. We have obtained a series of peaks at different temperatures plotting the noise referred to the input as a function of temperature for different spot frequencies. The temperature and frequency of each peak can be used to draw an Arrhenius plot, and the points can be fitted linearly to get the energy level and the capture cross section of the traps. Unfortunately, noise measurement does not discriminate between electron and hole traps. In figure 7 the Arrhenius plot for unirradiated n-channel transistors is depicted. We calculated an energy level Ec-Et (or Et-Ev) of 0.43 eV, with a cross section of $1.46 \cdot 10^{-13}$ cm^2 if hole traps or $2.44 \cdot 10^{-13}$ cm^2 if electron traps.

To study the impact of irradiation on the G–R noise component, we have plotted the noise plateau value as a function of the cutoff frequency before irradiation and then after 12 and 25 Mrad followed by annealing. This plot is shown in fig. 8. The points fall on the same line, therefore we conclude that the gamma irradiation does not modify the energy, cross section or concentration of the defects. This confirms the bulk nature of the traps, maybe introduced by the

single implant SIMOX technique. In our future work, we will investigate other substrates which are known to give better or different film and interface qualities, such as triple implant SIMOX or BESOI. This could possibly improve the noise performance of the technology.

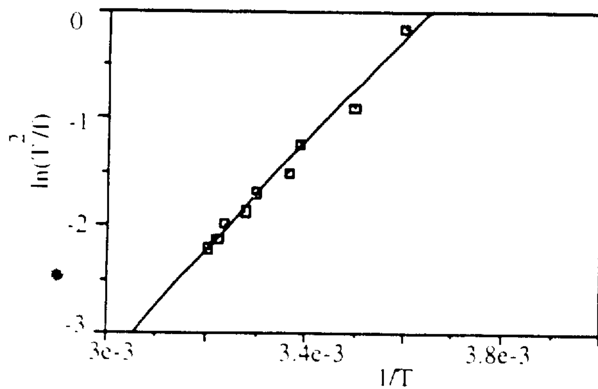

Figure 7: Arrhenius plot for the n-channel transistor G–R noise. From the slope of the linear fit it is possible to extract the energy level of the traps responsible for the noise. From the intercept, the capture cross section is obtained.

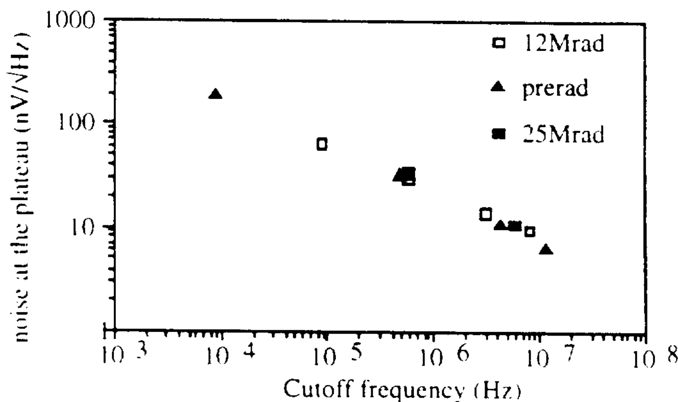

Figure 8: The noise value at the plateau of the GR noise is plotted against the cutoff frequency to show that the irradiation does not affect the generation-recombination process.

IV. CONCLUSIONS

We have studied the analog performance of basic transistors in the HSOI3-HD technology up to 25 Mrad. The n-channel transistors show a significant decrease in transconductance (44%) and an increase in 1/f noise (K_f increases by a factor 7) and are thus not adequate to be used where high gain and low noise are required. On the other hand, the p-channel transistors have a transconductance degradation of less than 18% and a lower Kf (1/3 of the n-channel after irradiation). Therefore, they should be preferred as frontend transistor in an analog circuit.

In measurements of static parameters and noise we found a saturation of the degradation after the first few Mrad. Therefore, we believe that the technology could stand a total dose even higher than 25 Mrad.

The G–R contribution found in the noise spectrum can be widely moved in frequency by changing the bias of the body or backgate terminals. Therefore, by choosing an appropriate body bias it is possible to make the white noise dominant at high frequency. This should be done carefully, because an excessive potential applied to the body could deteriorate significantly the output conductance. The presence of this undesirable G–R noise probably arises from defects in the substrate. We have measured the energy level of these defects with the noise versus temperature technique, obtaining Ec-Et (or Et-Ev) equal to 0.43 eV. The energy, cross section and concentration of these defects are not modified by ^{60}Co irradiation.

V. REFERENCES

[1] F.Faccio, E.H.M.Heijne, P.Jarron, M.Glaser, G.Rossi, S.Avrillon and G.Borel, "Study of device parameters for analog IC design in a 1.2 µm technology after 10 Mrad", *IEEE Trans. Nucl. Science*, Vol. 39, pp. 1739–1746, 1992.

[2] F.Faccio, M.Bianchi, M.Fornasari, E.H.M.Heijne, P.Jarron, G.Rossi, G.Borel and J.Redolfi, "Noise Characterization of Transistors in a 1.2 µm CMOS-SOI Technology up to a Total-Dose of 12 Mrad(Si)", *IEEE Trans. Nucl. Science*, Vol. 41, pp. 2310–2316, 1994.

[3] H.E.Boesch, Jr., F.B.McLean, J.M.Benedetto and J.M.McGarrity, "Saturation of threshold voltage shift in MOSFET's at high total dose", *IEEE Trans.Nucl.Science*, Vol. 35, pp. 1191–1197, 1986.

[4] J.L.Leray et al. "From substrate to VLSI: investigation of hardened SIMOX without epitaxy, for dose, dose rate and SEU phenomena", *IEEE Trans. Nucl. Science*, Vol. 35, No. 6, pp. 1355–1360, 1988.

[5] J.P.Coinge, *Silicon-on-insulator technology: materials to VLSI*, Kluwer academic publishers, 1991, p. 109

[6] V.Radeka, "State of the Art of Low Noise Amplifiers for Semiconductor Radiation Detectors", *Proceeding of the International Symposium on Nuclear Electronics*, Versailles september 1968, n. 46, pp. 1–26.

[7] Z.Y.Chang and W.M.C.Sansen, *Low noise wide-band amplifiers in bipolar and CMOS technologies*, Leuven, Kluwer academic publishers, 1991

[8] L.D.Yau and C.T.Sah, "Theory and experiments of low-frequency generation-recombination noise in MOS transistors", *IEEE Trans.El.Devices*, Vol. 16, pp. 170–177, 1969.

[9] F.Scholz, J.M.Hwang and D.K.Schroder, "Low frequency noise and DLTS as semiconductor device characterization tools", *Solid-State Electronics*, Vol. 31, No. 2, pp. 205–217, 1988.

[10] D.C.Murray, A.G.R.Evans and J.C.Carter, "Shallow Defects Responsible for GR Noise in MOSFET's", *IEEE Trans. Electron Devices*, Vol. 38, No. 2, pp. 407–416, 1991.