CERN/LHCC 95-40
5 July 1995

MEMORANDUM

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To: Members of LHCC, LCRB and LDRB

LERB Members

From: F.Bourgeois / ECP

Subject: Front-ends for calorimetry at LHC

The discussion on pipelined digitizing schemes for calorimetry at LHC during the May meeting of the LHCC could have used some clarification in the subjects of generic R&D activities and the requirements of ATLAS and CMS. On behalf of the LERB, I would like to summarize the situation in a few lines.

Readout for calorimetry at LHC must implement 3 main functions in a radiation tolerant technology in order to satisfy the goals stated in the technical proposals:

1) Provide energy sums (1 to 60 channels) to the trigger level 1 electronics;

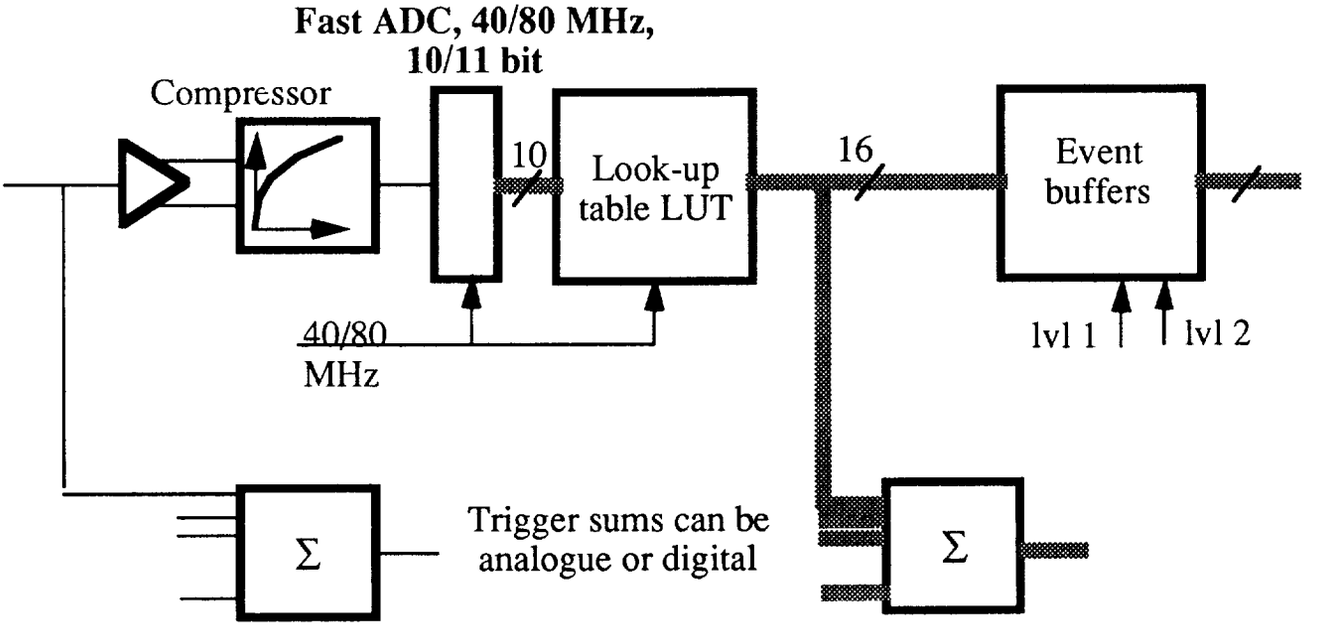
2) Store the analogue or digital samples in a circular buffer with simultaneous read and write capabilities for 2-3 microseconds at a minimum sampling rate of 40 MHz (80 MHz requested by CMS); this buffer must have a minimum depth of 128 cells;

3) Readout the data with a 16-17 bit dynamic range and a precision of 9-10 bits. The dynamic range is achieved with a piecewise linear response of the analogue part of the front-end by means either of a dynamic compressor (e.g. RD16) or, at least, two gain ranges.

Two architectures may be used to fulfil the requirements 2) and 3). They are:

A) The digital one in which a fast ADC is followed by a circular buffer (a fast digital memory). The use of this architecture is widespread since the advent of Flash ADCs (UA1, LEP, HERA experiments etc ...); two examples targeting at LHC application are given below.

A-1) FERMI/RD16 collaboration : see LHCC meeting of 17 May 1995.
Test results :
In the beam: tested end 1994 (a few channels only); 100 channels to be tested this September



Note : extra trigger level 1 latency for digital sums

Figure 1 : Digital architecture

A-2) Charge Integrator and Encoder QIE
Designer : R.J. Yarema (FNAL)
Physicist : G.W. Foster (FNAL)
Chip characteristics

Logarithmic, pipelined QIE chip to give a 4 bit exponent and an analogue, gain switched output. This analogue signal is fed into a conventional 8 bit Flash ADC (which gives the mantissa).

Nr of channels : 1 (PMT application)

Sampling rate : 53 Msps

Test results :

to be used by the KTEV experiment at FNAL

B) The SCA architecture in which an analogue circular buffer (a switched capacitor array SCA) is followed by an ADC. This ADC digitizes the samples associated with a trigger level 1 selected event (100 KHz).

Analogue pipelines (SCAs) were first used in 1983/84 (SLAC Analogue Memory Unit). Several other designs were since experienced and used in experiments (FNAL, HERA, LAA, LBL/Alberta, Nevis Lab, Orsay/Saclay, RD2, RD20). To reach 11 or more bits of resolution, each cell must be assigned a pedestal. According to the proponents of the latest designs, linearity is not a problem. Simultaneous read and write features have been tested in the lab. The list below gives the basic characteristics of the SCA designs with simultaneous read-write capabilities that will be tested for application in LHC experiments.

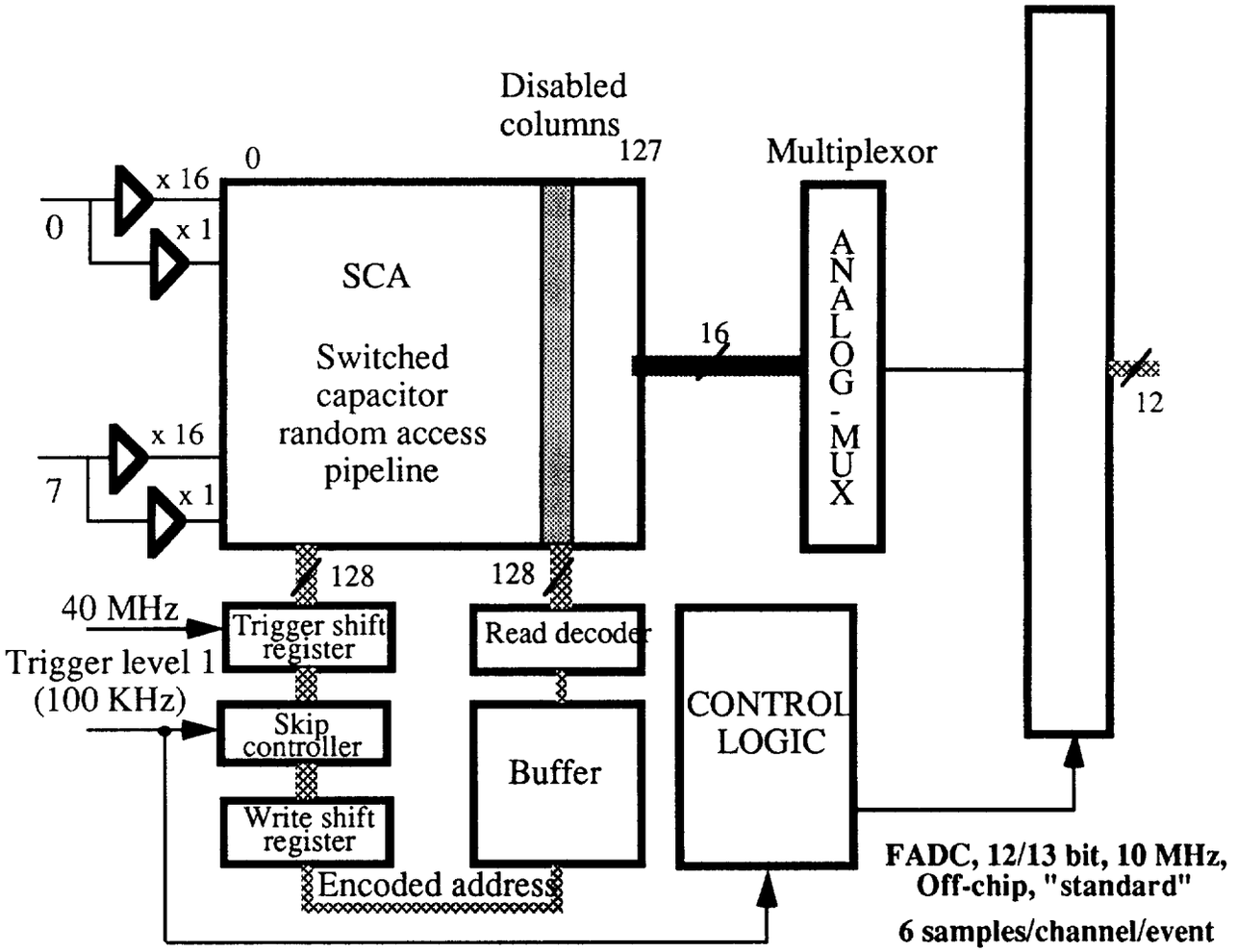


Figure 2 : Analogue architecture

B-1) Effort in Alberta (Canada)
Designer : S.A. Kleinfelder (LBL)
Physicists : J. Pinfold, D.M. Gingrich (Alberta)
Chip characteristics
Nr of channels : 16
Sampling rate : 40 Msps
Depth : 256 cells
Test results :
In the laboratory
Dynamic range : 11.5 bits with one pedestal per cell (to be confirmed)
Noise : 1.2 lsb incoherent, 0.4 lsb coherent
In the beam: tested in 1993 with the RD3 LAr calorimeter, improved version to be tested this September

B-2) Effort in Nevis Lab (USA)
Designer : W. Sippach
Physicists : J. Parsons, Al Gara (Alberta)
Chip characteristics
Nr of channels : 6
Sampling rate : 40 Msps
Depth : 128 cells
Test results :
In the laboratory (preliminary information)
Dynamic range : 13 bits (3.5 Volts full scale) with one pedestal per cell (700 μ V spread).
Noise : 350 μV
In the beam: tested in 1994 with the GEM calorimeter; 100 channels tested in June '95.

B-3) Effort in Orsay/Saclay
Designer : D.Breton (LAL), E.Delagne (Saclay)
Physicists : E.Augé
Chip characteristics
Nr of channels : 16
Sampling rate : 40 Msps
Depth : 128 cells
Pedestal equalization scheme (PSALM)
Test results :
In the laboratory :
Not yet available
In the beam : to be tested this September.

Beam tests for systems in the two architectures are taking place for ATLAS. ATLAS and CMS were asked by the LERB chairman to give dates for the following milestones :

1 - selection of an architecture (e.g. a la FERMI or analogue pipeline)

2 - Test of a prototype system of, say > 1K channels

3 - Beginning of the production of the total quantity