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Presented at the First Workshop on Electronics for LHC Detectors, Lisbon, Portugal, September 11–15, 1995, and to be published in the Proceedings

The STAR TPC Front End Electronics

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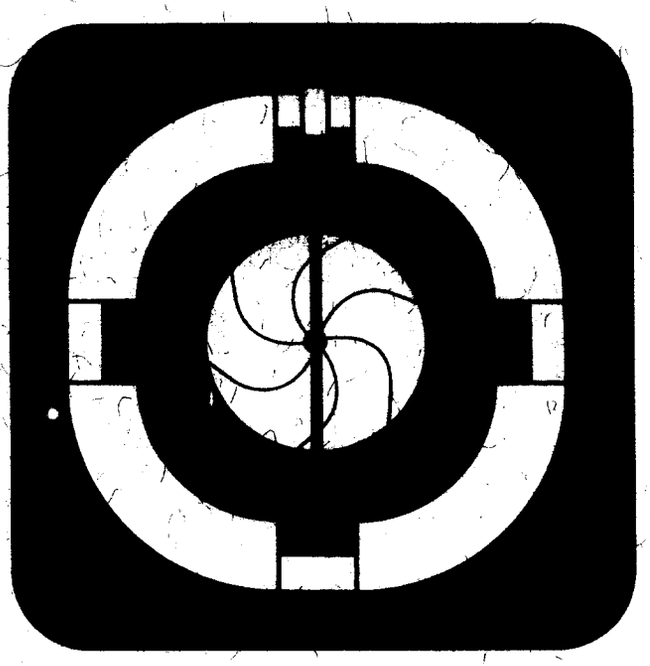
October 1995



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Abstract

The Solenoidal Tracker at RHIC (STAR) uses a large time projection chamber. Each of the 136,600 pads is instrumented with a waveform digitizer, implemented in custom low noise preamplifier/shaper and switched capacitor array/ADCs ICs. The system is highly integrated with all analog functions mounted on small cards that plug into the TPC. Detector mounted readout boards multiplex data from 1152 channels onto a 1.5 Gbit/sec fiber optic link to the data acquisition system.

I. INTRODUCTION

STAR [1] is a large solid angle detector now being built to study high energy heavy ion collisions at the Relativistic Heavy Ion Collider (RHIC). RHIC will collide heavy ions up to gold at center of mass energies up to 200 GeV/nucleon. Scheduled for initial operation in 1999, STAR, shown in Figure 1, will be composed of a silicon vertex tracker, large TPC to track charged particles with $|\eta|<2$, time of flight system, electromagnetic calorimeter, and forward tracking TPC, all in a 5 kG solenoidal magnetic field.

The STAR TPC is 4 meters long, and extends radially from 50 cm radius out to 2 meters. A charged membrane is placed in the center, and electrons drift to the two endcaps, where the signal is multiplied by anode wires. The image charge is detected on 136,600 pads arranged in 45 rows on the two endcaps. Each endcap is divided azimuthally into 12 supersectors. The electronics for each supersector is mounted on 181 32-channel FEE cards, which are read out by 6 readout boards.

To track 4000 or more charged tracks with $|\eta|<2$ per collision, three dimensional space point readout is required. Each TPC pad is read out by a 512 sample waveform digitizer, dividing the TPC into 70 million space points. To provide an acceptable rate into the level 3 trigger, this data must be digitized and read out at up to 200 Hz.

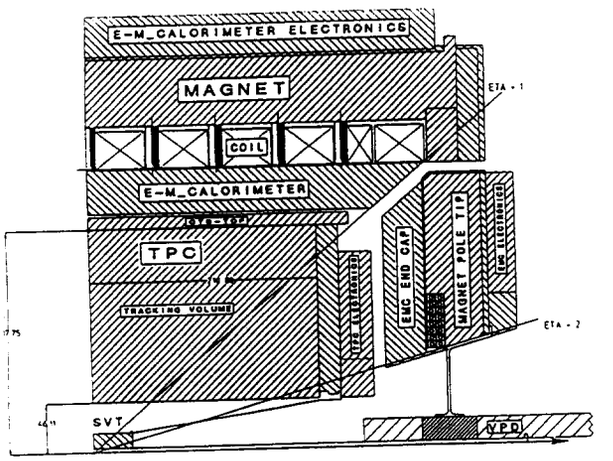

Figure 1. A quarter section view of the STAR detector.

The STAR electronics benefits from previous experience with the NA-49 [2] and EOS [3] TPC electronics. STAR follows the pattern set by these detectors with a preamplifier/shaper, switched capacitor array waveform digitizer, with the electronics mounted on the detector.

II. ELECTRONICS REQUIREMENTS

The TPC gas will be either P-10, which will have a 50 μsec drift time, or helium-ethane, with an 80 μsec drift time. The pads on the inner 13 rows measure 2.85 mm by 11.5 mm, while those on the outer 32 rows are 6.2 by 19.5 mm. The pad capacitances range from about 8 pF to over 30 pF (15 pF average), depending on the length of the trace to the FEE card connector.

Each of the 512 time samples corresponds to a 4 mm drift distance. Diffusion and electron statistics limit the resolution in the drift direction to about 700μ, or about 1/5 of a time sample. In the azimuthal

direction, the limit is 280/410 μ (inner/outer padrows). The azimuthal resolution is determined by charge sharing among neighboring pads. Monte Carlo studies indicate that to reach this limit, a 20:1 signal to noise ratio is required. The dynamic range is set by the requirement that the electronics accommodate a 200 MeV/c proton, which has about 10 times a minimum ionizing signal. To allow for Landau fluctuations, the electronics must not saturate for signals up to 40 times minimum ionizing.

III. ANALOG ELECTRONICS

The overall signal flow is shown in figure 2. The analog circuitry is implemented in two custom integrated circuits, the SAS (STAR preAmplifier /Shaper) and the SCA/ADC (Switched Capacitor Array/ADC). Both chips are 16 channels wide, and implemented in 1.2 μ CMOS.

The SAS chip [4] incorporates an integrating preamplifier with switched reset, a two pole shaper, and an output buffer. The overall chip gain is 16 mV/fC, giving a 50 mV output for a 19,000 electron minimum ionizing particle, and a 2 volt (saturated) output for a 760,000 electron 'maximum ionizing' input.

The integrator has a folded cascode input, with a 1.6 pF feedback capacitor. The capacitor is discharged by a CMOS switch; the measured charge injection is small, and totally masked by noise from the gated grid on the TPC. The integrator maximum charge is more than 1.1 pC, or over 300 minimum ionizing particles. The input capacitance is about 10 pF.

The total noise includes contributions from the SAS, SCA and TPC pad. The SAS noise is about 600 electrons plus 13 electrons/pF. The SCA noise is about 1 mV, or about 390 electrons referred to the SAS input. The TPC pads introduce noise because the G-10 insulator is a poor dielectric. The noise is that of a resistor with a R= $\tan(\delta)/\omega C$ where $\tan(\delta)$ is the dielectric loss angle, the fractional energy dissipation per cycle. For our G-10 $\tan(\delta)$~0.014, so the noise is about 300 electrons. Combining these contributions in quadrature gives a total noise of 940 electrons for 15 pF pad capacitance, 5% of a minimum ionizing signal. It should be noted that the TPC anode wire gain can be increased if the 20:1 signal to noise ratio proves inadequate.

The chip incorporates two input protection diodes. While previous TPC electronics [2,3] has included external protection diodes, our tests indicate that the internal diodes are adequate. Since external diode leakage can contribute to charge buildup on the integrator, we do not plan to use them.

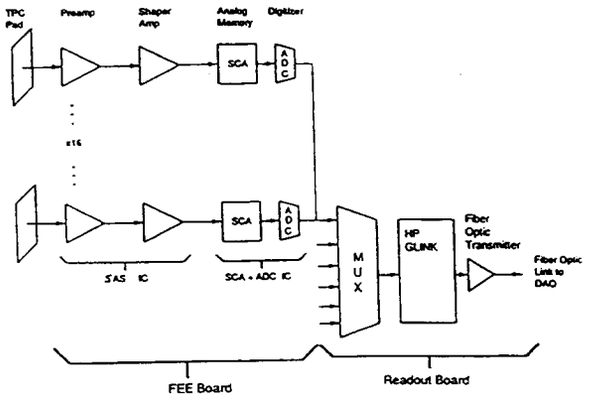

Figure 2. The FEE signal processing chain.

The two pole shaper has a 180 nsec FWHM, chosen to match the diffusion time spreading. The FWHM can be varied by about 40% via an external voltage. The shaper includes an adjustable 1/t tail correction circuit, to match the measured TPC signal shape for the two gases. The SAS can drive a 50 pF load (2 SCA/ADC chips). The chip also includes internal calibration circuitry. Other specifications include linearity better than 5%, crosstalk less than 0.3%, power consumption of 60 mW/channel, DC output voltage matched within 200 mV for all chips.

The SCA/ADC [5] is identical to that used in NA-49. The 512 sample switched capacitor array can sample up to 40 MHz, with a static and dynamic linearity better than 2% over a 2 volt range, with about 1 mV of noise. Because of leakage and charge injection variations, separate pedestals are required for each time bin. Because the pedestals will include contributions from the TPC gated grid switching, the SCA clock is generated by the clock/trigger system, and synchronized to the trigger.

The ADC is a 12 bit Wilkinson converter; STAR plans to only use 10 bits of conversion. The converter counts on both edges of a 60 MHz clock. Each channel has its own ADC, so 512 time buckets can be digitized in about 5 msec; because the ADC is double buffered, readout occurs in parallel with the conversion, minimizing deadtime.

This electronics is mounted on small (2.9" by 7") 32 channel FEE boards, which plug directly into the TPC pad plane, eliminating most cabling. The electronics density is too high to mount the electronics

directly on the TPC pad plane; in addition this would make maintenance and cooling very difficult. Pairs of FEE boards are connected to the readout board by a 50 conductor flat ribbon cable.

IV. DIGITAL CIRCUITRY

Up to 36 FEE boards (1152 TPC pads) can be controlled by a single readout board. The readout board multiplexes the data from the FEE boards over a 1.5 Gbit/sec fiber optic link to the data acquisition system. The readout board also provides trigger, control monitoring and diagnostic functions.

The optical transmitter is a Methode MTM-8510, driven by a HP Gigalink (HDMP-1012) serializer chip. It accepts 20 bits of data at a 60 MHz clock rate - two 10 bit SCA data words in parallel. Transmission is simultaneous with the SCA digitization, so event readout takes a little under 5 msec. The readout control orders the data to optimize the data acquisition system processing speed.

Figure 3 shows the 40 bit wide, 30 MHz bus that supplies data to the serializer. The wide bus necessitates some additional multiplexing, but is necessary because of the speed limits imposed by physical separation between components. This bus is fed by 9 multiplexer FPGAs, each of which controls two FEE cables, a total of four FEE boards.

The bus also connects to a memory which can store a complete event. The memory can be written to and read from by a slow control link, or by the FEE data stream. This memory and alternate readout path are used for diagnostic purposes and during electronics

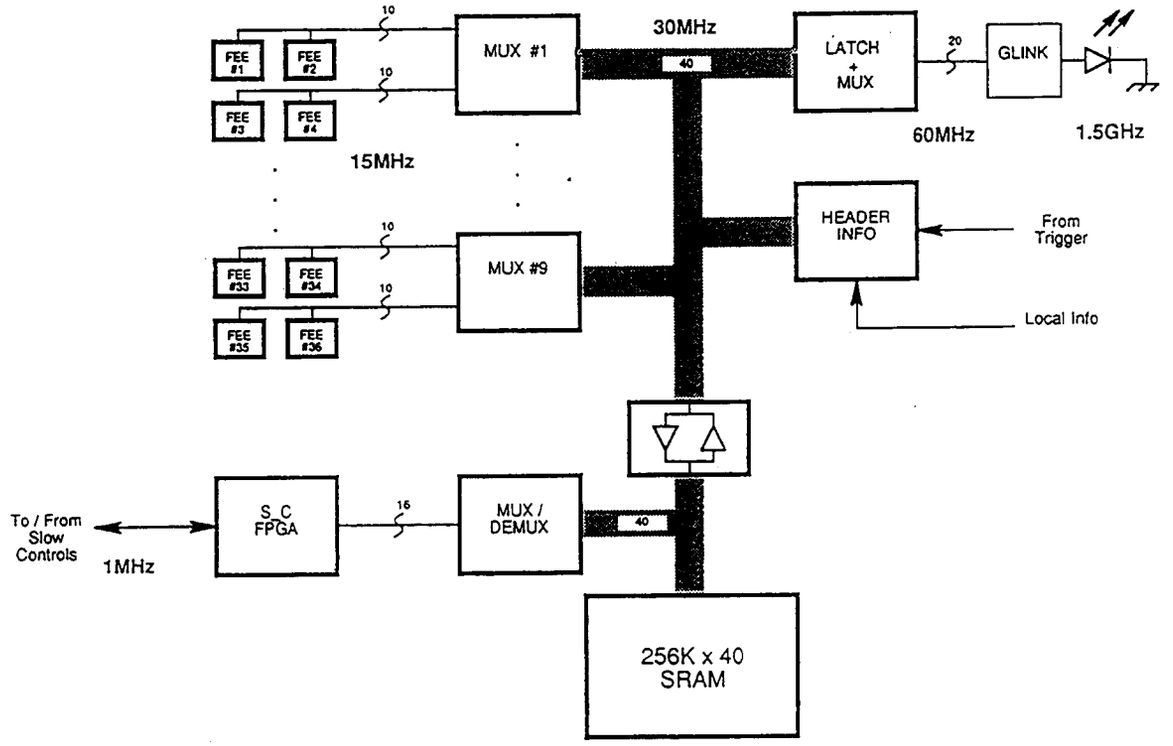

Figure 3. The readout board bus scheme.

installation.

In addition to diagnostic event readout, the controls link can monitor and adjust voltages on the card, turn groups of FEE cards on and off and monitor temperatures. It is based on native HDLC, running at 1 Mbit/sec. HDLC was chosen because other protocols were too inefficient for large packets (Bitbus and LONworks) or would not easily work in a magnetic field (Ethernet). A VME master communicates with the six readout boards of a single supersector over a multi-drop RS-485 link. The readout board end of the link uses a 68302 processor serial port. The 68302 and memory are mounted on a small plug in board. This board has been adopted by other STAR subsystems.

Clock and trigger information is transmitted to the readout boards over a clock and trigger bus. The bus

transmits 8 signals: the 9.3 MHz RHIC beam crossing frequency, a 4 bit data bus and a data clock (five times the crossing frequency), the SCA sampling clock, and a spare. The spare may be used for a second SCA clock, to allow for a nonuniform SCA sampling on the inner TPC sectors. The data bus transmits 20 bits per RHIC crossing, a 4 bit trigger command, a 4 bit DAQ command and a 12 bit trigger token. Trigger commands include triggers, trigger aborts, several calibrations, and a geographical address readout. The DAQ command allows the DAQ and level 3 trigger to respond differently to different types of level 0 triggers, such as low multiplicity (two photon) events. The trigger token is a 12 bit tag that ensures that data from different events does not get mixed during event building. The trigger bus uses AT&T series 41 differential pECL drivers and receivers, chosen for their high speed and good common mode rejection.

To detect cabling errors, each of the FEE boards and readout boards is tagged with a geographical address. The FEE board addresses are etched into the TPC pad planes; the readout board addresses are encoded in connectors attached to the board mounting. These addresses can be read out as a special trigger and passed through the entire DAQ event building and tape writing process, to test that no data is swapped or otherwise confused.

Each readout board receives power over 25 meter long cables from a plus and minus 8 volts at 20 amperes supply located on the detector platforms. Because of the long cables, we incorporated regulators on the readout boards. The supplies themselves are ferroresonant, chosen for their simplicity, reliability and inherent voltage regulation and overcurrent protection.

V. TESTING AND MONITORING

For a system of this size, testing is a major issue. We have built custom chip testers for both of the custom IC's. Each tester is composed of a PC, hardware and software (LabWindows) interface, and custom analog circuitry. The SAS tester measures power consumption, gain, noise, crosstalk and signal FWHM in 1 minute per good IC. The SCA tester checks power consumption, gain, noise, in 3 minutes per good IC. When a test is failed, the testing stops, so bad IC's are detected quickly. We expect yields of about 70% for the SAS and 30% for the SCA, so we will have to test about 45,000 chips in total. To keep track of the chips individually, each chip is labeled with a bar code; a bar code reader attached to each tester allows quick and accurate entry of the chip number.

We are also designing a FEE board tester. It is a combination of the SAS and SCA tester circuitry

During operation, the system is monitored by several calibration systems. These include a UV laser which creates ionization tracks, a pulser that pulses the TPC ground plane wires, and the previously described SAS internal calibration circuitry.

VI. SYSTEM ISSUES

Because of the size and complexity of STAR, considerable effort has gone into system level issues. One area of concern was cabling and ground loops; most of the STAR TPC electronics is mounted directly on the detector. All long distance transmission uses optical links or differentially driven cables. The detector mounting itself imposed stringent requirements on reliability and maintainability.

In the FEE, the TPC wheels (support structure) are a single point ground. The power supplies are completely isolated (except for 750 pF/supply capacitative coupling) from ground. The data fibers are, of course, isolated. The clock and trigger fanouts and the slow controls link are all differentially driven to minimize their contribution to ground loops. Because the AT&T chip inputs only have a 7kΩ impedance to ground, we have tried to limit the number of differential pairs going to the detector.

Because the STAR TPC will be used for dE/dx as well as tracking, the TPC pad plane temperature must be controlled with 0.7° C, so an efficient cooling system is needed for the FEE cards. This is done with an aluminum backer that covers the back of FEE cards where the SAS and SCA chips are located. The backer is bolted to an aluminum water cooling channel. Similar channels are bolted to the readout boards.

VII. STATUS

As of this writing, the FEE card design is complete, and card have been tested on a TPC sector, read out with a FEE board tester. The readout board design is essentially complete, with all of the fast logic prototyped on a VME board.

Chip procurement for the initial 8% of the electronics is well underway, and we expect to have the initial 8% build complete early next year, in time for a summer cosmic ray test.

VIII. LOOKING AHEAD

Since this is a workshop on LHC electronics, it is appropriate to say a few words about what might be done differently if we were designing STAR for 2004.

One fundamental change might be to better match the SAS and SCA to the TPC signals. The TPC signals change shape as the signals drift, depending on the diffusion and dip angle. It might be desirable to electrically adjust the SAS shaping time and SCA sampling rate in the course of a single event, to maintain optimal resolution over the entire drift distance.

Other changes are more evolutionary. We would have developed more highly integrated electronics, with a single chip containing preamplifier through ADC. This chip might accommodate 24 or 32 channels, depending on the TPC pad size, and might also incorporate a more sophisticated (faster) ADC and readout scheme. It could be implemented in a finer line technology, 0.6 or 0.8 μ CMOS. Because any increased separation between the TPC pads and the preamplifier means increased capacitance, and hence noise, there is limited gain by putting too many more channels on a single chip. While it might be possible to mount electronics directly on the TPC pad plane, the problems of testing bare IC dies, and being able to easily replace broken electronics would argue strongly against this.

The power consumption could be reduced, simplifying the cooling problem. A combined SAS/SCA would be a first step. To go further in CMOS technology (necessary for the SCA) would require reducing the preamplifier current, at some cost in noise (noise ~ current$^{1/4}$). To maintain the signal to noise ratio, we would have made two changes. First, a four pole shaper would have a more Gaussian pulse shape, and hence lower noise for a given pulse width. Second a higher anode wire gain, and lower preamplifier gain would accommodate more SAS noise, and hence a lower preamplifier current.

The digital electronics would be similar to but more highly integrated the existing design. However, physical separation between the pads determines the optimal integration; as more channels are multiplexed onto a single optical link, the signals come from a larger and larger area., It might become cheaper to have many smaller readout boards. The fiber optic data link and partitioning of control signals between a fast trigger bus and a slow addressable controls system seems sound, and would probably remain unchanged, although a more sophisticated controls network might be appropriate.

IX. CONCLUSIONS

We have designed and are building a 136,600 channel waveform digitizer system for the STAR TPC. The system has high performance, storing 512 samples/channel at up to 20 MHz, with 10 bits of accuracy. The system is highly integrated, with all of the electronics mounted on the detector. All of the analog electronics is mounted in two custom integrated circuits. This integration provides a compact system at an affordable cost.

Because of the system size, we have put considerable effort into providing diagnostic and error checking capability. The major diagnostic features include a separate slow controls path for data readout, a complete geographic id capability, and dual paths for resetting the electronics.

We have also worked to maximize the maintainability of the system. We use ferroresonant power supplies instead of switching supplies which are less reliable. Each readout board has a bank of 9 individually switchable regulators, so that, for many failures, only a small number of channels will be lost.

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