



ATLAS Note

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WinCC OA project limit studies

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In preparation of Phase-2 upgrade of ATLAS experiment, for the high luminosity era, the subsystems are required to develop the Detector Control System (DCS) based on their unique needs. A key consideration for this upgrade is the size of WinCC OA projects in terms of various parameters. Understanding how large a WinCC OA project can be, without compromising performance is critical for ensuring the stability and efficiency of the DCS.

The current internal note presents studies conducted on WinCC OA projects in order to assess the limits of the servers that are being used by ATLAS experiment. The results provide practical guidance for detector groups, helping them determine how to structure their control systems, in terms of datapoint elements and eventually how many WinCC OA projects will be needed based on their detectors' needs.

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32 1 Introduction

33 1.1 ATLAS DCS architecture

34 The DCS ensures the reliable and safe operation of ATLAS by providing a unified interface for all
35 sub-detectors and the experiment's technical infrastructure [1]. Its architecture is divided into two main
36 categories: the Front-End (FE), which consists of commercial or custom-made hardware devices, and the
37 Back-End, where an industrial Supervisory Control and Data Acquisition (SCADA) software package
38 is used to implement the control system. The communication is realised through various technologies
39 and protocols, with the most commonly used in ATLAS being OPC Unified Architecture (OPC UA), a
40 cross-platform, open-source standard for data exchange in a server-client model.

41 1.2 WinCC OA

42 WinCC OA is a software package designed for use in automation technology [2]. It provides a comprehensive
43 set of tools and features for real-time monitoring, control, and visualization of industrial processes. Its
44 operation is based on gathering information from FE equipment and offers supervisory control functions
45 such as data processing, execution of control procedures, alert handling, trending, archiving, and a web
46 interface.

47 The WinCC OA architecture is divided into layers, with each layer consisting of specific units that utilize
48 the necessary functionalities depending on their assigned tasks. These units, that are called *managers*,
49 communicate using a special WinCC OA protocol over TCP/IP.

50 The central processing unit of a WinCC OA project is called the Event Manager (EM) and is responsible
51 for maintaining an up-to-date image out of all process variables in memory. Other managers, query data
52 from EM's process image rather than communicating directly with the control units, making the EM the
53 central data distributor of a project.

54 This communication is being performed in the form of messages. To ensure smooth project operation, two
55 message queue containers are defined with specific limits on the number of messages that can be sent to
56 and received from the EM. If this limit is exceeded, the EM becomes saturated. In such case, EM will
57 automatically disconnect from the manager responsible for exceeding the container limit, and that manager
58 will be stopped. The upper limit of message queue container, in the receiving direction of EM, is defined
59 by the config file entry `maxInputMsgCount` with a default value of 100,000 messages. The upper limit of
60 Buffer Control Manager (BCM) output queue in the sending direction (to all other managers) is defined by
61 the config file entry, `maxBcmBufferSize` with a default value of 10,000 kB [3, 4].

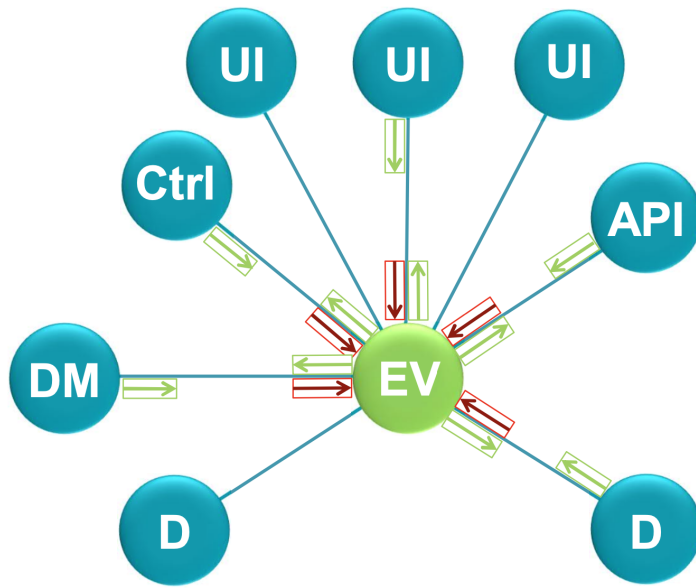


Figure 1.1: The flow of messages to and from the EM.

62 **1.3 DCS usage**

63 In the simplest approach, a typical project in the DCS context is responsible for monitoring and controlling
 64 hardware (such as a high-voltage mainframe or gas system). An OPC UA server acquires raw data from
 65 the hardware and passes it to a client within a WinCC OA project, where it potentially undergoes further
 66 processing.

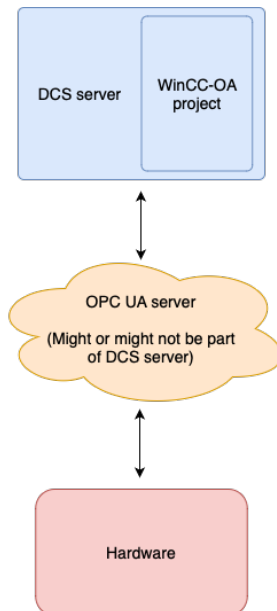


Figure 1.2: Simplified use case of a DCS server, OPC UA server and hardware interconnection.

67 1.4 Typical ATLAS DCS server

68 As of October 2024, the ATLAS DCS production environment utilizes Dell PowerEdge R440 servers, each
69 running one or more WinCC OA 3.19 projects, depending on the project size, and one or more OPC UA
70 servers, depending on the project's requirements. These OPC UA servers may operate locally or remotely
71 (on a separate server from the DCS) and communicate with the WinCC OA project over TCP/IP.

Table 1.1: Dell PowerEdge R440 technical specifications [5].

Number of DPs	Number of DPEs
Processor	Intel Xeon Silver 4210 CPU
Cores per socket	10
Threads per core	2
Processor base frequency	2.20GHz
Memory	32GB

72 2 Study foundations

73 2.1 The average project

74 To establish a consistent foundation for the study, it was considered imperative to set four primary
75 assumptions in order to define the phase space of exploration. Each of these assumptions is treated as a
76 variable under investigation.

- 77 • Assumption 1: The structure of datapoint type (DPT).
- 78 • Assumption 2: The number of datapoints (DPs) typically present in an average project
- 79 • Assumption 3: The number of control managers employed (for setting new values)
- 80 • Assumption 4: The model of server used.

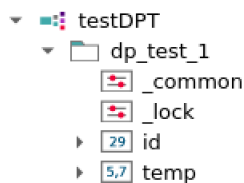


Figure 2.1: DPT structure.

81 In order to facilitate a quantitative analysis of the aforementioned variables, it was deemed necessary to
82 define an "average" project as, a data point type (DPT) comprising two data point elements (DPEs): one of
83 the integer type and one of the floating-point type (figure 2.1). A dataset composed of 5,000 DPs, *two*
84 control managers and a *R440* Dell server.

85 2.2 Test procedure

86 The systematic examination of the variable outlined above, necessitated the desing of a structured test
87 procedure, which was developed with the objective of simulating the behavior of an approximation of a real
88 project in the most accurate manner. Conducted within a WinCC OA 3.19 environment, the test procedure
89 began with the creation of a test project, including the generation of the DPT and the corresponding
90 DPs. A script utilizing the `dpSet()` function was developed to assign values to both DPEs, mimicking
91 hardware-induced value changes. Additionally, a script using the `dpConnect()` function was created in
92 order to respond to these changes. These two scripts were mapped into three control managers¹, with one
93 control manager handling the `dpConnect()` script and two handling the `dpSet()` script instances.

¹ Each manager corresponds to a single process

94 The objective of this study was to determine the *rate* of DPEs that can be written, without exceeding the
95 default message queue limit of EM (config file entry `maxInputMsgCount`), in receiving direction.

96 In order to obtain concrete, reproducible results, the script responsible for setting new values in DPEs
97 was executed in a loop of 100,000 iterations, a value mirroring the default value of `maxInputMsgCount`.
98 Looping over the buffer size was chosen to ensure that each iteration generates more messages than can be
99 processed. This approach serves as a definitive indicator of the rate's sustainability. Within each iteration of
100 this loop, a nested loop executed for a specific number of DPs defined by the individual test case. The goal
101 of the study -to determine the sustainable rate of written DPEs per second- was achieved by introducing a
102 delay between the two loops.

3 Results

3.1 DPT structure

Throughout the study, the DPT structure (Assumption 1) remained unchanged, as the two DPE types, integer and float, are representative of the most common data types returned by hardware devices. Moreover tests have shown that variable type does not play a vital role in performance; however, additional types, may be considered in future studies.

3.2 Using different number of DPs

The exploration of the aforementioned phase space, began focusing on the total number of data points in a project (Assumption 2).

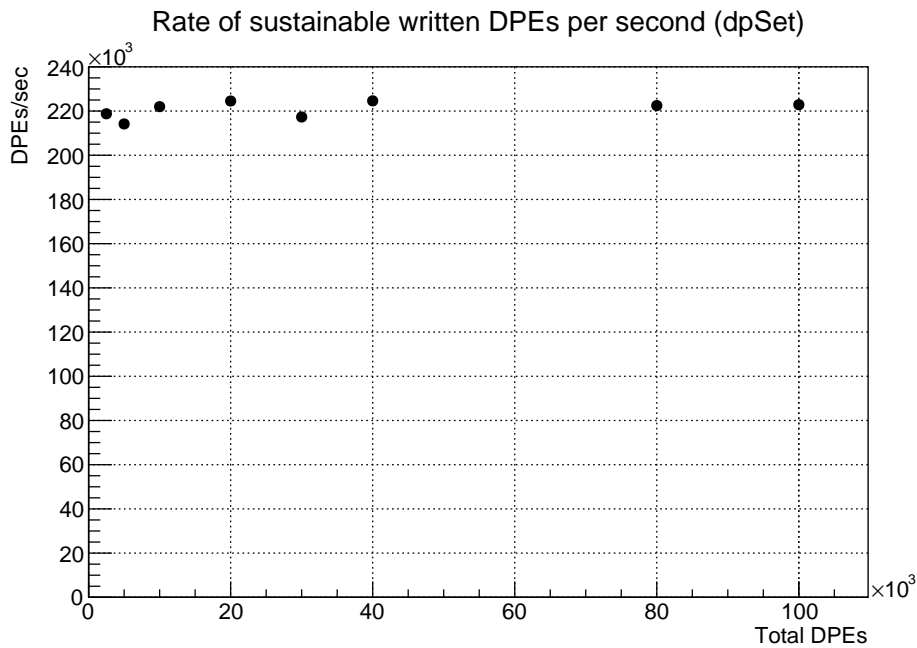


Figure 3.1: The graphs depicts the maximum sustainable rate of datapoint elements that can be written against the number of total datapoints that the project has.

In the plot shown in figure 3.1, is displayed the maximum sustainable rate of DPEs that can be written, without causing saturation of the Event Manager (EM), relative to the number of total DPEs available in the

114 project. The graph demonstrates a constant behaviour with values fluctuating around 220,000 *DPEs/sec*,
 115 indicating that increasing the number of DPs does not impact project's efficiency.

116 A closer examination of the plot, indicates that the number of DPEs tested reached up to 100,000. During
 117 the course of the studies it was attempted to exceed this number, but the tests were unsuccessful as they
 118 immediatelly triggered EM message queue limit. It should be noted however, that if needed, it is possible
 119 to increase the number of DPEs by modifying the `maxInputMsgCount` entry, in project's configuration
 120 file.

121 The following table 3.1, presents the precise numerical values used in plot, 3.1, for reference.

Table 3.1: The rate of written datapoint elements.

Number of DPs	Number of DPEs	DPEs/sec
1250	2500	218765.294
2500	5000	214170.920
5000 (average project)	10000	221993.818
10000	20000	224539.751
15000	30000	217319.066
20000	40000	224615.902
40000	80000	222466.334
50000	100000	222869.270

122 3.3 Using different number of control managers

123 Based on the assumptions of the average project that were defined in section 2, the next variable under
 124 invastigation, is the number of control managers that utilise the `dpSet` script (Assumption 3). In the table,
 125 3.2, can be found the maximum sustainable rate of DPEs that can be set by one, two and four control
 126 managers, when the total number of DPs in the project is 5000.

Table 3.2: The rate of written datapoint elements for different number of control managers.

Number of control managers	DPEs/sec
1	228685.046
2 (average project)	221993.818
4	219679.497

127 A comparison of the measured rates, utilizing different number of control managers reveals an increase
 128 of approximately 2.96% when only one control manager is used instead of two. The decrease is smaller,
 129 approximately 1.05%, when four control managers are used instead of two.

130 3.4 Tests on Dell R610 server

131 The final assumption pertains to the server on which the tests were conducted. In order to complete the
 132 studies, it was considered valuable to obtain the maximum sustainable rate of DPEs that can be written to a

133 Dell R610 server (former production servers) for an average project.

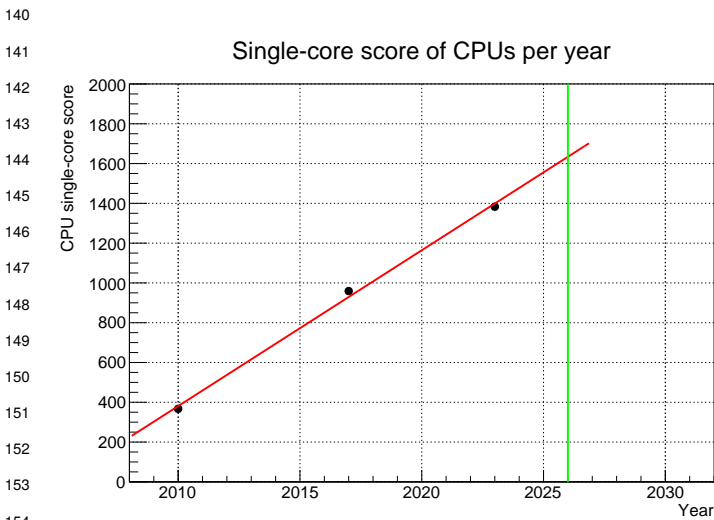
Table 3.3: Dell PowerEdge R610 technical specifications [6].

Number of DPs	Number of DPEs
Processor	Intel Xeon CPU E5620
Cores per socket	4
Threads per core	2
Processor base frequency	2.40GHz
Memory	16GB

134 Comparing the measured rates achieved on the two different server models (table 3.4) reveals a significant
 135 difference in performance. The data rate on the Dell R440 server is approximately three times greater than
 136 that of the Dell R610, reflecting the superior processing power and architectural advancements of the former.
 137 This difference aligns with the single-core performance scores (source, <https://www.geekbench.com>), where
 138 the Intel Xeon Silver 4210 CPU (of R440 server) scores 959 compared to the Intel Xeon CPU E5620 (of
 139 R610 server) score of 367 [7].

Table 3.4: Comparison of Server Models

Server model	Processor	Single-core score	Processor year	DPEs/sec
R610	Intel Xeon E5620	367	2010	73173.397
R440 (average project)	Intel Xeon Silver 4210	959	2017	221993.818
-	Intel Xeon Gold 6430	1383	2023	-
Future model	Future processor	1650 (EV)	2026	-



155 Figure 3.2: The graphs displays the CPU single-core score of Intel Xeon E5620, Intel Xeon Silver 4210 and Intel Xeon Gold 6430. Based on a linear fit in the previous values, the single-core score of a 2026 CPU is extrapolated.

The upcoming high-luminosity upgrade is scheduled to take place between 2026 and 2029 [8]. Therefore, it was considered valuable to extrapolate the single-core score of a CPU projected to be built in 2026. In order to achieve this, we included the single-core score of a 2023 CPU (Intel Xeon Gold 6430) that could be part of a server built in the same year. This extrapolation yielded an estimated single-core score of approximately 1650 for a 2026 CPU, suggesting that the maximum sustainable rate of written DPEs per second a server can handle, will increase, supporting higher data processing demands.

156 **4 Conclusion**

157 This note presented the findings from the studies conducted on WinCC OA projects for the ATLAS DCS,
158 offering essential insights into the scalability and performance limits of the projects. Through systematic
159 tests involving varying numbers of DPs, control managers, and server models, it was observed that the
160 maximum sustainable rate of DPEs remains stable with increased DPs, although performance is moderately
161 impacted by the usage of additional control managers. These findings provide practical guidelines for
162 configuring WinCC OA projects in order to maintain efficiency and prevent reaching system's limits,
163 ensuring reliable performance during High-Luminosity LHC phase.

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