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R&D Proposal

DEVELOPMENT OF HIGH RESOLUTION Si STRIP DETECTORS FOR EXPERIMENTS AT HIGH LUMINOSITY AT THE LHC

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Abstract

Recent studies indicate that good tracking near the interaction region in LHC experiments will be crucial to fully exploit the physics potential of this machine up to the highest luminosities. It is believed that Si strip detectors are among the best candidates to survive in the experimental environment imposed by the high energy, high luminosity and the severe radiation levels expected.

It is therefore proposed to perform a systematic study of the feasibility of using Si strip detectors and suitably designed front-end electronics for tracking in LHC experiments.

Issues discussed here are possible physics applications, requirements and design characteristics for Si strip detectors and front-end electronics and cooling. An R&D programme for the coming two years is described.

Everything should be made as simple as possible,
but no simpler.

Albert Einstein, 1879 - 1955

Table of Contents

1. INTRODUCTION

1.1 Tracking at LHC

The construction of high-luminosity, high-energy hadron colliders within the next decade is by now recognized to be the top priority in high energy physics. It is realistic to assume that a machine like the LHC can perform at luminosities of above $10^{33} cm^{-2} sec^{-1}$ and may reach extreme luminosities of above $10^{34} cm^{-2} sec^{-1}$ in order to shed light on new phenomena in physics. Possible physics scenarios attainable with such accelerators have been widely discussed [1.1, 1.2]. In the boson sector, the discovery of the standard model neutral Higgs or of charged Higgs doublets would be of prime importance. In the fermion world, the top quark awaits discovery, which may happen before at the Tevatron collider (present limits on the top mass from CDF, UA1, UA2 and LEP seem to push it out of the range of $200 GeV$ LEP). In this case, however, a detailed study of the properties of the t quark [1.3] will be a realistic physics goal for an LHC. Other scenarios predict the appearance of supersymmetric particles, technicolour particles, composite W and Z bosons, . . . at LHC energies.

Whereas it seems feasible how to build high luminosity machines, there is much more uncertainty at present how to build detectors which are capable of measuring the outcome of interactions at these extreme energies and luminosities. This proposal addresses the question if Si strip detectors are suitable for tracking in an LHC environment. It is assumed that tracking is necessary - at least in some detectors - up to the highest possible luminosities in order to fully exploit the physics potential of the LHC. Many arguments in favour of the necessity of good tracking have been made recently [1.3,1.4,1.5,1.6]. These will not be repeated here. However, in order to explain the scope of this proposal, a few physics cases are mentioned here, which have been considered for guidance to develop ideas for a R&D programme on Si strip detectors to be used for tracking at LHC.

Tracking will be essential for processes with interesting fermions, which have relatively high cross-section, but are nevertheless buried in very high backgrounds. E.g., it is argued that for top quark masses up to 300 or $400 GeV$ LHC is a top factory able to produce up to 10^6 (m_t = $350 GeV$) or 10^7 (m_t = $200 GeV$) events per year at $\mathcal{L} = 10^{33} cm^{-2} sec^{-1}$. In studying these t particles, b meson tagging with a very precise vertex detector will be important to enhance signals above background. B particles are copiously produced at LHC. High statistics clean event samples can be obtained using a very high performance vertex detector tagging these events by the B decay vertex. Enough statistics may be available even after a very rigorous selection using vertex criteria to allow a study of possible CP violation effects in the B-sector. This requires a reasonable statistics sample of fully reconstructed decays in a defined CP eigenstate. For processes with interesting bosons, e.g. the standard neutral Higgs decaying into 4 leptons via Z^0Z^0 or $H \rightarrow \gamma\gamma$ decay, highest luminosities will be needed to have a few detectable events. For this case, it is extremely difficult to predict if global tracking can still be done ($\mathcal{L} \geq 10^{34} cm^{-2} sec^{-1}$), but it nevertheless seems essential to have some tracking information to allow association of tracks which are identified in calorimeters or filters as leptons or associate leptons or γs with the correct primary vertex. A further point under consideration is that at very high luminosities multiple interactions in one bunch crossing need tracking information near the vertex to separate the primary vertex of the interesting events from several other minimum bias event vertices.

A non-exhaustive list of topics where high precision tracking near the vertex will be required is listed here :

- Primary vertex identification.
- Impact parameter measurement at the primary vertex with high precision for leptons and hadrons from heavy flavour decays.
- Full reconstruction of secondary vertices from inclusive and exclusive decays of heavy flavours.
- Separation of several primary vertices within one bunch crossing.
- Momentum measurement of charged particles.
- Lepton identification in conjunction with a calorimeters and μ filters.
- γ conversion rejection together with e calorimetry.
- Association of identified leptons with proper primary vertex.
- Identification of topologies, e.g. very high p_T jets, charged particle multiplicity, . .
- Measurement of jet thrust axis.
- Use of track information in second level trigger.
- . . . .

1.2 Scope of Proposal

Si detectors are considered to be good candidates of tracking detectors which can operate in an LHC environment. The speed of charge collection in Si, typically about $30nsec$ for $300\mu m$ thick detectors, the radiation hardness and the possibility to have fine granularity almost at will predestines Si strip detectors (and clearly also Si pixel detectors) to fulfil the requirements for their use at high luminosity and very high track densities expected for LHC experimentation. Existing experience with the Si vertex detectors of ALEPH and DELPHI experiments at LEP is very encouraging concerning their capability of high precision tracking. It is however clear that none of the existing devices could be used straightforwardly in an LHC environment.

For both detectors and front-end electronics, the requirements, in particular radiation hardness and speed, are so much more demanding at LHC that an intensive R&D programme is necessary to prove that these devices can indeed be used in LHC experiments. Similarly, one has to extrapolate from existing trackers by at least a factor of 10 to 20 in size, so that totally new systems aspects, e.g. mechanical stability, radiation hardness of support materials, alignment, quality control, etc. have to be considered.

The purpose of this proposal is to show areas where R&D work has to be done on specific components of a Si tracking device and propose specific projects to solve open questions. It is not intended to propose at this time to build a prototype of a Si tracker for an LHC experiment, but to study the performance of all the necessary components under conditions as expected around the beam pipe of an LHC interaction region.

Included in this study are applications for experiments both with protons and with heavy ions, including SPS heavy ion experiments. In order to evaluate the requirements on the detector components, a model of a possible Si tracker for each application is defined to serve as a test ground and to understand which system aspects have to be worked on. It is intended to arrive at the end of an about 2 year long R&D programme, which is the subject of this proposal, at a precise specification of a Si tracker for the different applications. It is expected that the construction of a full prototype system will be proposed as an outcome of this work.

References

[1.1] Proc. of ECFA Study Week on Instrumentation Technology for High Luminosity Hadron Colliders, Vol. 2, CERN 89-10 ECFA 89-124, Nov. 1989.

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[1.4] G. Tonelli et al., *Silicon Tracking at High Luminosity*. ECFA Aachen, Vol. III, p.285.

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[1.6] J. Hylen et al., *Silicon Tracker Conceptual Design Report*. SCIPP 90/24, JHV-HEP-90-0831, CALTEC 68-1673, Sept. 90.

2. POSSIBLE APPLICATIONS

2.1 Tracker and Vertex Detector for Luminosities of $10^{34}cm^{-2}sec^{-1}$

2.1.1 Design Concept

Physics requirements ask for a first coordinate determination with the highest possible accuracy as close as possible to the interaction point. This requirement has however to be confronted with the limited radiation hardness of detectors and front-end electronics and technical limits to the finest achievable granularity of strips which determine the quality of two-track separation. The approach in this study aims at full functioning of the detector at the highest luminosities (of and above $10^{34}cm^{-2}sec^{-}$) but also takes into consideration that a large amount of very important physics (in the fermion sector) can already be done at a luminosity of $10^{33}cm^{-2}sec^{-1}$. Since, to present knowledge Si strip detectors can survive about 3 years of continuous opera-tion at $\mathcal{L} = 10^{34}cm^{-2}sec^{-1}$ with still reasonable performance (see Chapters 3 and 4 of this pro-posal), it is assumed that a first layer of detectors can be placed approximately at $r = 10cm$. It may have to be foreseen that the one or two innermost layers of a realistic detector are con-structed in a modular way, so that they can be exchanged every 2 or 3 years, or whenever their performance has degraded below a certain required level.

An optimal design for a tracker/vertex detector will only be possible after considerably more knowledge has been gained concerning the performance of the different detector components in an LHC environment. To develop ideas for relevant R&D studies one needs however to have a concept of a detector. A central detector, covering a range of η from -1.8 to +1.8 (range of polar angle from 20 to 160 degrees) is proposed. The covered range is approximately the same as proposed for the Silicon Tracker Preshower, which is regarded for this exercise as a complementary detector. Two ideas are described here, which can be further studied, modified and evaluated.

The first of the proposed designs is in Fig. 2.1a. The detector consists of 3 double layers. These layers are built of double-sided microstrip detectors with strip pitch of $50\mu m$ on both sides. The radii of these layers are 10, 20 and $30cm$. The total area of silicon is $10.6m^2$; the total number of readout channels is 8.5 million.

Another design is drawn in Fig. 2.1b. There are also three double layers built of the same detectors as mentioned before. In the central part, where layers have cylindrical shape radii are also 10, 20 and $30cm$. The range of polar angle covered is also the same. Tracks with θ lower then 30 degrees cross only one layer however. For $30 < \theta < 45$ two layers, and for $\theta > 45$ all three layers are crossed. This design will also probably make system aspects (mechanics, cooling, powering and readout) more difficult. But the total area of silicon is only $3.5m^2$ and the total number of readout channels is 2.8 million, both three times less than for the first design. Another important advantage is that the tracks do not cross detector planes at angles lower than 45 degrees. In the first design it is only 20 degrees near the cylinders ends.

For small angles the signal is divided between many strips on one of the sides and much harder to detect because of that.

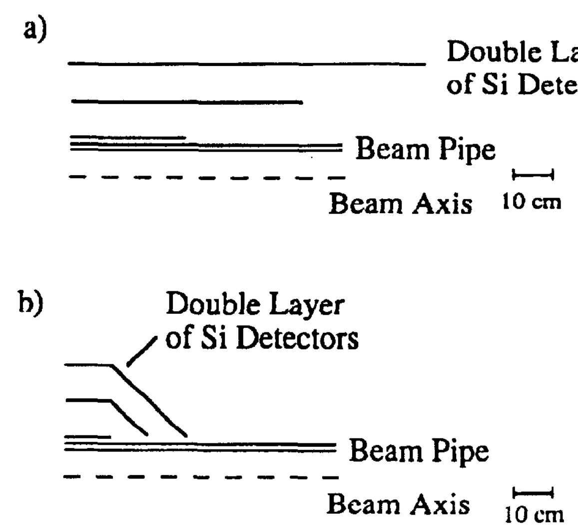


Fig. 2.1
Two preliminary layout concepts for a tracker design.
The figures show one quarter of the cross-section along the beam axis.

It is expected that the future design of the tracker will be a modified version of one of the two presented here. The design decisions depend on further studies on :

- physics performance - simulation using SLUG (Simulation for LHC Using Geant), in cooperation with groups working on other proposed detectors
- double-sided detectors and readout electronics
- system aspects: cooling, mechanical stability and precision, powering and readout connections
- radiation hardness of the detectors and electronics.

It should be emphasized that some of the most complex problems will be posed by the requirements on the cooling.

2.1.2 Performance Considerations

First studies concerning double-track resolution have already been performed with the use of the PYTHIA event generator. The highest demands for this resolution are inside high energy jets, typical for interesting high transverse momentum events. Figure 2.2 shows the average fraction of tracks that are not overlapped by others as a function of radius and for different double-track resolutions (50, 100, 200 and 500μm) inside a $1 TeV$ jet. Assumed is a double-sided strip detector, that has the same resolution in two dimensions and of the order of at least 200μm is necessary to resolve tracks in the conditions expected.

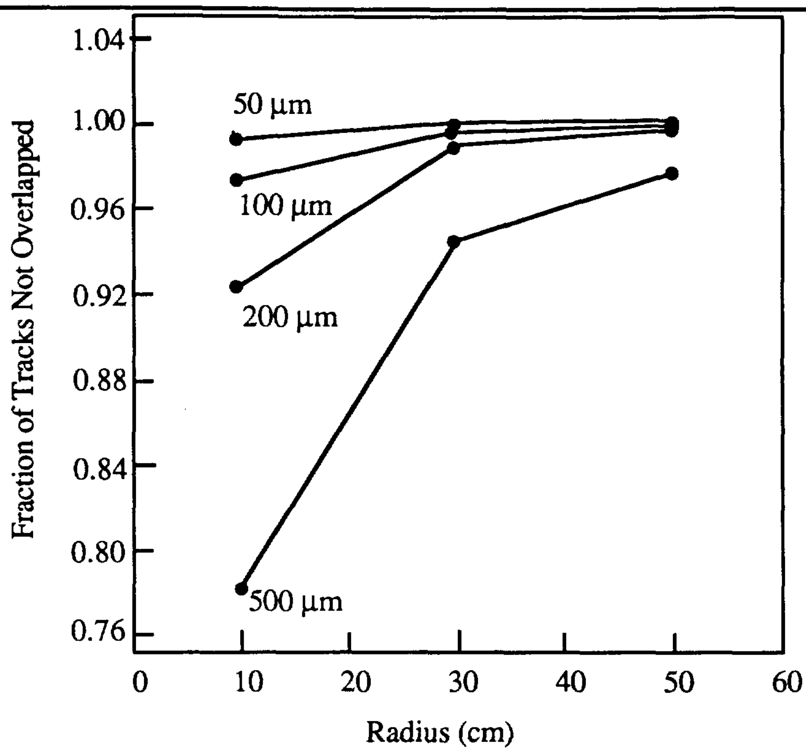


Fig. 2.2 Fraction of tracks that were not overlapped by others at least in one projection inside a 1TeV jet as a function of radius and for different double-track resolutions (50, 100, 200 and 500μm. Assumed is the same resolution in two perpendicular directions on the detector plane.

Extensive simulation studies including tracker combined with other detectors have to be performed to test the physical performance of the considered designs. Some results can be obtained before that however.

Stand-alone momentum resolution of a Si tracker is given by the formula:

$$\frac{dp}{P} = \frac{P}{0.3\,B}\sqrt{\frac{720}{N+5}}\,\frac{e}{\ell^2}$$

p : momentum (or P_t in principle) in GeV

B : Magnetic field in Tesla (I assume a 2T field)

N : Number of points (equidistant). According to the PDB the formula is ok for $N > 10$, but I checked that it is still good for N=3

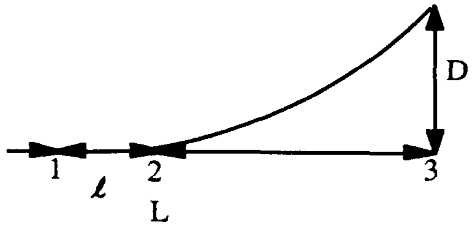
e : resolution of the tracker (I assume $e = 15\ \mu m$)

ℓ : projected length of the track (= lever arm of the device)

If we assume 3 double layers at 10, 20 , 30cm we get: $N = 3$, e = 10μm (each double layer provides one point with e/$\sqrt{2}$ precision) and $\ell = 20cm$:

$$dp/p = 0.41\% \times p \quad (33\% \text{ at } 80\text{ GeV})$$

This is not very exciting and there is need of an external measurement.



Assumed is a third measured point at $L = 1$m, with a resolution of $200\mu m$. The momentum measurement is simple : a straight line is extrapolated from the tracker at 1, 2 to 3 and the distance D to the track impact is measured. We ignore problems of pattern recognition at that point. Then :

$$\frac{dp}{P} = \frac{6.7\,p}{B}\sqrt{s^2 + 2\left(\frac{L}{\ell}\right)^2 e^2}\ \frac{1}{L^2}$$

with s : resolution at 3. (This formula is approximate, it requires $L/\ell >> 1$ (5 is ok), and in principle only 2 points measured in the tracker (3 improves a bit). With $\ell = 20$cm, $L = 1$m, $e = 15\mu m$ and $s = 200\mu m$, $B = 2$T one achieves:

$$dp/p = 0.07\% \times p,\ (33\% \text{ at } 500 \text{ GeV}),$$

which is sufficiently good.

Under these assumptions, the resolution is dominated by the intrinsic resolution of the external tracker (s) and its lever arm (L). It is an interesting exercise to find the minimal requirements for the tracker, before it starts to have the main contribution to the resolution:

$$s > \sqrt{2}\,\frac{L}{\ell}\,e$$

as $e = 15\mu m$ is more or less granted, (let's have some safety margin!) we find that $L/\ell > 10$, or the device should be longer than $10cm$

It could be concluded that a 3 (double) layer tracker at 10-30cm, together with a measurement at large radius (with moderate resolution) provides a momentum resolution which is sufficient for most LHC physics. In stand-alone mode the resolution is very moderate, but might still be of help for pattern recognition and track extrapolation to outer devices.

With r : inner radius and ℓ: lever arm, the impact parameter resolution is

$$d(i) = e\sqrt{1 + 2\frac{r}{\ell} + 2\left(\frac{r}{\ell}\right)^2}$$

With $r = 10cm$, $\ell = 20cm$, $e = 15$:

$d(i) = 23\mu m$ (16 with double layers)

$r = 20cm$, $\ell = 10cm$, $e = 15$:

$d(i) = 54\mu m$

The average impact parameter of a B-track is about $240\mu m$: A simple example: assuming i is exponentially distributed for b events and we make a cut a 3σ resolution to reject non-B background one would be 75% efficient with $d(i) = 23\mu m$, with $54\mu m$ the efficiency would drop to 50%

Concerning impact parameter resolution it is necessary to go as close to the interaction point as possible. 10*cm* seems to be sufficient, 20*cm* is probably too far away.

2.2 Tracking for Heavy Ion Experiments at SPS and LHC

An area of physics for which the proposed R&D programme would be of the highest interest are the Heavy-Ion experiments foreseen at CERN in the years 1994-1995 at the SPS (fixed target) and in the first years of operation at the LHC, used in collider mode with nuclear beams up to Pb.

The aspects of relevance are different in the two cases, and will be treated separately in the following, although the researchers concerned are the same and the physics programme are ideally one the continuation of the other. It should be apparent that these timescales make some of the developments on the critical path for the experiments, and would thus have a high priority for the physicists involved.

2.2.1 Physics with Heavy Ions at LHC

The injection of heavy ions in LHC is currently foreseen since the beginning of its operation [2.1]. The centre-of-mass energy per nucleon would be lower than in the proton-proton mode, still giving a 1262*TeV* total c.m. energy for Pb-Pb collisions. The design luminosity would be $2 \cdot 10^{27} cm^{-2}\, s^{-1}$, several orders of magnitude below the maximum luminosity in the p-p mode.

A proto-collaboration for an experiment addressing both heavy ion physics and p-p minimum bias physics was set up in December 1990, at which point several working groups on specific items were formed, namely : 1) Global event characteristics and event generators; 2) Hadron spectra; 3) Dileptons and direct photons; 4) Hard processes (jets); 5) pp minimum bias. So far no detailed detector specification has been given, and only general concepts have been presented (see Figs. 2.3 and 2.4).

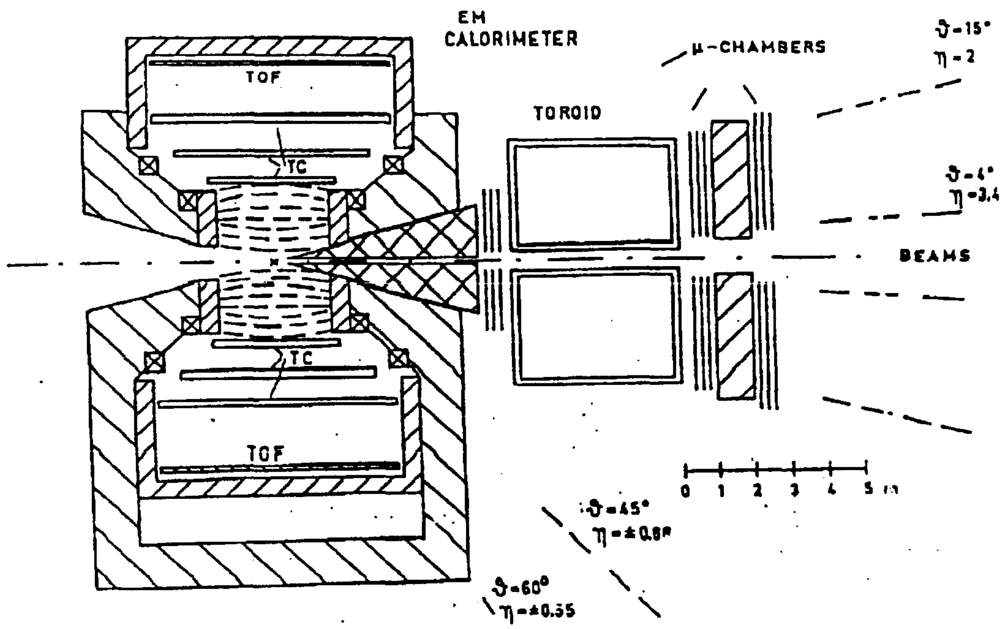


Fig. 2.3
General concept of a detector for heavy ions and pp minimum bias experiments at LHC.

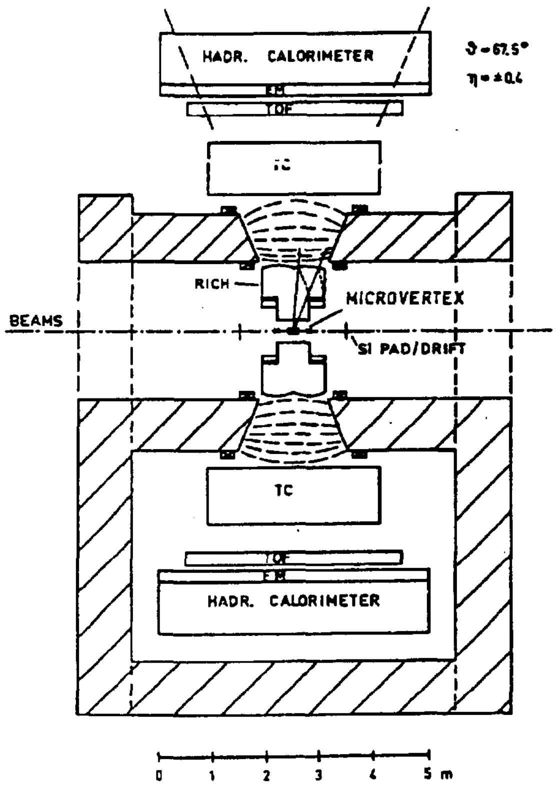


Fig. 2.4
General concept of a detector for heavy ions and pp minimum bias experiments at LHC.

The expected charged particle densities are considerably higher than in p-p collisions : for central *Pb-Pb* collisions, event generators like VENUS [2.2] indicate dN (charged)/dy of the order of 2000 and dN (charged)/d (Omega) around $300 sr^{-1}$.

The detector components where high resolution silicon detectors would be highly desirable are :

a) Microvertex for hyperon decay detection and determination of Cerenkov rings' centres;

b) Multiplicity detector to tag central collisions.

Both applications demand rather high granularity, due to the high multiplicity : for example, a microvertex layer at $R = 5cm$ with a track density of 13 tracks/cm^2 would require $200{\times}200 \mu m^2$ elements to ensure 0.5% cell occupancy. On the other hand, at larger distances, double-sided strip detectors represent the most attractive option.

For this application, rate and radiation hardness requirements are substantially less demanding than for LHC p-p at full luminosity, while most of the system aspects would be the same.

2.2.2 Fixed Target Experiments with Pb Beams at SPS

The operation of SPS with heavy ion beams is foreseen to start in 1994 (the concept of the accelerating facility is described in the report CERN 90-01). Proposals for experiments are currently in preparation : among them, four groups are considering using high resolution silicon detectors (NA35, NA38, WA80, WA85).

Due to the high luminosity (up to $4 \cdot 10^8$ ions / 15 seconds, and with targets of up to 20% of an interaction length) and to the Lorentz boost, experimental conditions are actually more challenging than at LHC/ions and even LHC/pp.

In particular, at R = $5cm$, track densities at forward angles would be up to $30/mm^2$ for central interactions, and integrated fluxes for a 50 days run (at 10^8 ions/burst on a 20% target) would be up to $7.5 \cdot 10^{13}$ neutrons/cm^2 and $4 \cdot 10^{15}$ charged particles/cm^2.

A specific application which is being studied with extensive Monte Carlo simulations is the measurement of charged multiplicity in NA38 (a high-rate dimuon experiment) in the laboratory pseudorapidity range 1.6 to 4.0.

A distance of a few cm from the interaction point is required to limit the number of background muons coming from pion and kaon decays. Good resolution on N(charged) for central events (about 1400 tracks in the quoted angular range) requires a granularity of the order of 10^4 elements.

A schematic view of a possible detector arrangement is shown in Fig. 2.5, with two identical detectors subdivided into 24 sectors each; every sector would be further segmented into a few hundred strips. Overlaid is an event as expected from heavy ion interactions. Detailed specifications are expected in a few months from now.

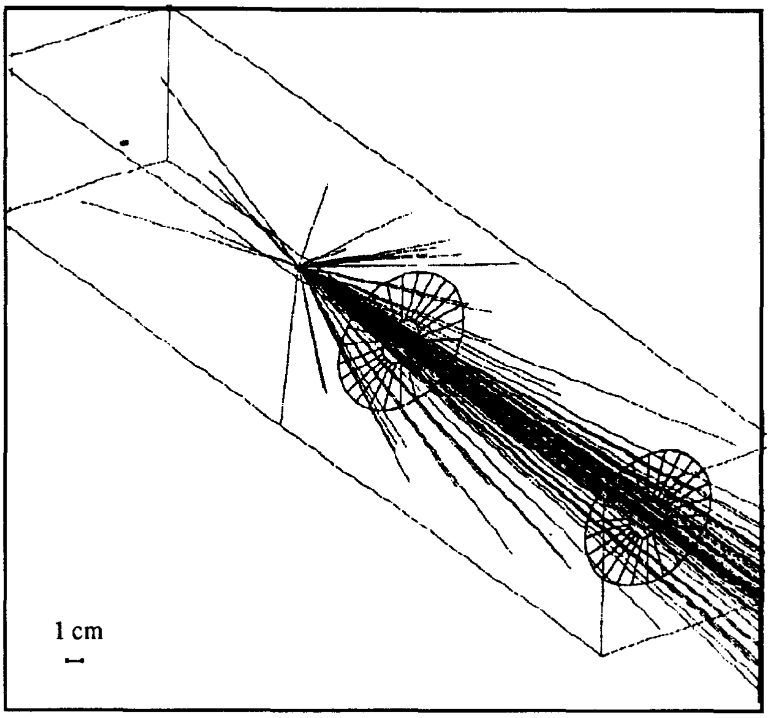


Fig. 2.5
Schematic view of a possible arrangement of a silicon detector for a fixed target experiment.

2.3 A Dedicated Beauty Experiment at the LHC

During last autumn, a test to use a high resolution Si tracker with forward geometry has been successfully performed in the UA1 interaction region of the Sp$\bar{p}$S collider (P238 test). This vertex detector consisting of 48 Si strip detectors was running at a distance of ± $3mm$ from the interacting beams at high luminosities with negligible background and good track efficiency.

This result encourages the planning of a dedicated beauty experiment for the LHC using a Si forward tracker and dedicated trigger processors. This development will be the subject of a separate proposal for R&D to the DRDC. The specifications for Si detectors and associated front-end electronics for such an experiment will be similar to those required by the applications mentioned in Chapters 2.2 and 2.2. Some of the specific design requirements for silicon detectors and front-end electronics for this application are described in Appendix A. It is intended to do some R&D work specific for this application within the framework of this study.

References

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3. Si STRIP DETECTORS

Requirements for LHC

We make the assumption that double sided silicon microstrips are the most likely detectors to be used on a wide scale for tracking close to the beam at LHC as a consequence of probable availability and expertise in their use. Naturally, this does not exclude more complex detectors like pixels to be employed when available where they offer advantages. Neither does it exclude the use of simpler detectors such as single sided microstrips, although complex events in a low mass detector will require maximum information from minimum material.

3.1 Performance specifications

It is important to note that detailed specifications can only be arrived at in combination with simulation studies which identify the physics requirements. Conversely, realistic simulations can only be carried out with a knowledge of the practical possibilities for the detectors. There will be important limitations imposed by occupancy in terms of size of element and allowable space point ambiguities from multiple hits. The requirements on momentum resolution are not well known and will influence the layout of the strips. Radiation damage effects are easier to estimate, as far as signal to noise performance is required, but there are many unknowns to be evaluated. Power consumption and cooling, as well as mechanical support will be ingredients in the final specification.

With these qualifications in mind we propose some outline specifications as a guide to future design, Table 3.1, which can be refined as further information becomes available. They are based on what we believe to be achievable in the near future using present technology.

No assumption has yet been made about the relative orientation of the strips since this can be chosen as required once the technology is fully demonstrated. We expect to commence with orthogonal strips but orientations of less than 90° may be advantageous to reduce spatial ambiguities if the required spatial resolution in both coordinates can be achieved.

The three main requirements emphasised by Table 3.1 are segmentation, speed and radiation damage. We comment briefly on each of these.

Table 3.1 Possible starting specifications for LHC microstrip detectors - based on double-sided, a.c coupled technology

Parameter	Value	Comment
Wafer thickness	~300μm	on 4inch wafer
Strip dimensions	60mm × ~10μm	fit 4inch wafer & minimise strip capacitance
Strip pitch	50μm	
Number of strips	9 x 128	
Strip leakage current	<10μA	after several years
Total leakage current	30mA	guard currents should not be excessive after irradiation
Bias resistor	100$k\Omega$	
p-side strip capacitance	<5pF	if possible, adjust strip widths
n-side strip capacitance	<5pF	to achieve
Decoupling capacitance	100pF	
Depletion voltage	<50V	during operation
Operating voltage	100V	
Breakdown voltage	>150V	
Interstrip resistance	>100$k\Omega$	

Segmentation

This parameter depends on the position resolution, signal sharing between strips and radiation damage induced leakage currents. Strips must be read individually, for reasons of speed and immunity to radiation damage, and it will be challenging to bond at higher density than 50μm.

Speed

A good signal to noise ratio cannot be achieved unless the charge collection time is short compared to the amplifier time constant. It has already been emphasised [3.1] that detectors must be well over-depleted to ensure sufficiently rapid charge collection but, to make matters worse, charge collection times are expected to change during the lifetime of the detector as a consequence of bulk radiation damage [3.2]. This particularly affects the hole component of the signal which is expected to be slowed significantly. Recent measurements indicate that charge collection can be maintained at least up to neutron fluences of ~10^{14} $n.cm^{-2}$ if detectors are operated at 100V [3.3].

Radiation damage

In the central cavity the charged particle dose will depend (as $1/r^2$) on radial distance from the beam while the neutron fluence will be practically isotropic. Annual neutron fluences of ~$10^{13} cm^{-2}$ will be typical while a charged particle dose of ~$2 \cdot 10^4$ Gray at $10cm$ radius may be expected [3.5].

From data on bulk damage to silicon by neutrons and charged particles estimates can be made of the increase in leakage current, probably with sufficient accuracy [3.2], since there are strong dependences (factors of ~3) on design of the overall system, in particular the calorimeter composition and location. There are also possibilities to reduce the flux of neutrons by inserting moderator materials.

To demonstrate the conditions under which a tracking detector must operate estimates are made of expected changes in bulk leakage currents at LHC and consequences for a "minimal" detector (Table 3.1). Damage constants based on available data have been used - $6.9 \cdot 10^{-17}$ A.cm^{-1} for neutrons and $2.9 \cdot 10^{-17}$ A.cm^{-1} for charged particles. (For details of the assumptions see [3.2,3.5]). Annealing effects, which are not yet fully understood, may result in a reduction in leakage currents in actual operation (by factor ~ 2).

Table 3.2 Annual rate of leakage current increase for $\mathcal{L} = 10^{34} cm^{-2} s^{-1}$ and $10^7 sec$/year operation

Layer	R (cm)	L(cm)	ΔI(μAcm^{-2})	ΔI_{layer}(A)	ΔP(kW) (at 100V)
1	10	50	131	0.4	0.04
2	30	130	33	0.8	0.08
3	50	200	25	1.6	0.16

Electronic noise depends on detector segmentation; examples are calculated assuming microstrips 50μm × 6cm in each layer. After five years of operation the strip currents and shot noise, assuming CR-RC shaping, are given in Table 3.3.

Table 3.3 Microstrip leakage currents and shot noise contribution after 5 years operation

Layer	ΔI_{strip} (μA)	ENC_{shot} (e) 15ns CR-RC	ENC_{shot} (e) 45 ns CR-RC
1	20	1890	3270
2	5.0	950	1650
3	3.8	825	1430

Although present indications are [3.3] that the detectors would function adequately after several years the shot noise will become high enough that cooling of the detector below ambient temperature may well be advisable. In addition to current increases in the strips themselves it may be necessary to pay special attention to guard currents at the periphery of the detectors to ensure that power consumption does not become unacceptably high.

The consequences of radiation damage are not confined to leakage current increase [3.2] and most of these effects are only beginning to be studied significantly. Many of the questions can only be answered by designing and fabricating new detectors and evaluating them for hardness. It is unlikely that any detectors presently in use will be adequate without further development.

3.2 Choice of technology

Double sided microstrips must be a.c coupled to the electronics. In principle this need only be the case for one surface if the second surface strips are read out through low input resistance, d.c. coupled preamplifiers but experience to date suggests that interstrip currents will necessitate capacitors on both surfaces.

The capacitors should be integrated on the detector for reasons of space, which is not difficult. There are two biasing techniques in use - punch-through and accumulation layer resistors (*Aleph* [3.6,3.7]) and polysilicon resistors (*Delphi* [3.8]). There are two isolation techniques - field stops (*Aleph*) and field plates (*Delphi*). None of the alternatives can yet be excluded on the basis of experimental results, although accumulation layer resistors on the n-side are hard to manufacture with great uniformity [3.9]. The polysilicon resistors are now known to be very hard with respect to neutron irradiation [3.4] so appear to be particularly promising.

Detector thickness

We expect signal to noise to be a challenge. Therefore, despite the wish to minimise material, we assume that ~300μm is required which can be achieved with 4 inch wafers. Most probable signals of ~25,000 electrons are expected. For several reasons this is not likely to be the typical signal observed on a single microstrip. Landau fluctuations tend to give rise to average pulses larger than the most probable value. Particles will not usually be incident on the silicon normally, again increasing the total pulse size.

Charge sharing between strips will be common on at least one surface, which will reduce the typical signal on a strip. The combination of magnetic field and electric field in the silicon will give rise to non-normal drift paths for electrons and holes. The effect is most serious for the electrons where angles of up to ~18° for a 2T field ($\tan(\mu_H H)$~0.3) may be expected. This can significantly distort the position measurement in a digital readout system

[3.10] and reduce the signal on each strip. If the strips are orthogonal on the two surfaces, the effect could be minimised by ensuring that the p-type strips, collecting holes, are placed parallel to the magnetic field - which is easy to arrange in the barrel of a solenoidal detector.

Microstrip capacitance and decoupling capacitors

Noise, speed and power consumption are vital determinants of a silicon tracking detector system. They depend explicitly on the detector capacitance at the amplifier input [3.11] and it is advantageous to reduce the microstrip capacitance if possible. It is well known that this is determined mainly by interstrip capacitance, and thus can be reduced to some extent, but there is concern that on the ohmic side of the detector this is higher than on the junction side. Some calculations [3.12] have suggested that this can be reduced significantly. If true, this will be an important specification to be achieved.

The values of decoupling capacitors are chosen to ensure the maximum signal transfer into the amplifier; some, usually small, loss is inevitable. The conditions usually applying to a charge-sensitive amplifier are that $C_d << C_c << C_a$ referring to, respectively, detector, coupling and effective amplifier input capacitances. This seems to be quite easy to attain in most circumstances, eg a 5cm x 10μm strip using 0.2μm oxide gives C_c=90pF. For a current sensitive amplifier, much the same condition holds except that now $C_d << C_c << 1/\omega R_a$ with R_a the input resistance. Since typical values of R_a are likely to be ~100Ω, and must be kept small to minimise the pulse rise time, this condition should still be satisfied.

Bias resistors and interstrip resistances

Given the expected increase in leakage current, there is no purpose in making bias resistors of the values currently in use. From a noise point of view, a 100kΩ resistor in parallel with the amplifier input is equivalent to a leakage current of 0.5μA and would be adequate at LHC. If every strip is read out relatively low interstrip resistances can also be tolerated; the requirement is that they should be large compared to the amplifier input impedance which is likely to be ~100Ω.

3.3 Specific R&D projects

Some systematic studies of radiation hardness of detectors (for example using neutrons) are already under way and some double sided detectors exist, or are in an advanced stage of production, which will be available for irradiation. We see a need to supplement the information which is now, or shortly will be, available by further systematic radiation studies using several different particle types and specifically designed components, as well as detectors themselves, to understand fully the tolerance of detectors to the LHC environment.

We propose therefore to design test structures (which will include detectors of several sizes) which will be fabricated and tested under irradiation. The test devices will include microstrips, diodes, resistors, capacitors and gated diodes which will allow the evaluation of key elements of full size detectors but they will be fabricated on only one side of the silicon wafer, allowing the independent testing of the two surfaces. Particular properties which require examination are the behaviour of different types of bias resistors, maintenance of interstrip isolation, charge collection speed and annealing behaviour, as well as technology specific features possibly unique to individual manufacturers.

The irradiations will be carried out at RAL (using neutrons), Strasbourg (low energy electrons), CERN (particle beams) and elsewhere, as available. These will provide complementary information on both bulk and surface components of the damage. We hope to identify not only weak points in the designs, but also to shed some further light on the basic origins of the radiation damage so that further hardening can be achieved.

Since bulk damage is of such importance to the leakage currents and thus the noise behaviour of the system there is interest in demonstrating more clearly whether or not any improvement in bulk tolerance can be expected. In addition, serious attention must be paid to the n-side of the detectors, about which little is yet known regarding their post-irradiation behaviour, and interstrip capacitance, which has an important influence on power consumption of the front end amplifier.

The production of test structures and much of their evaluation should take place in the first year of the programme with continuation expected at a lower level in the second year. Our main interest in the second year, having identified the elements of a successful radiation tolerant design, will be to fabricate detectors of close to full size using a limited number of directly comparable designs in the technologies available to us.

We have identified three main manufacturers - SI (Norway), IHP (Germany) and VTT (Finland) - with whom we have developed working relationships in the last few years and who have expressed interest in participating in this programme. We expect to continue to work closely with them on the detector design and fabrication technology to achieve our goals. However there is no intention to exclude from consideration detectors produced by other manufacturers who may be willing to collaborate with us.

References

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4. FRONT-END ELECTRONICS

The requirements for a front-end electronic system which can operate around an LHC interaction region at a luminosity of around $10^{34} cm^{-2} s^{-1}$ and a possible solution are discussed. This paragraph outlines the general principles. Details are discussed in Appendix B.

4.1 Constraints

In the absence of definitive timing constraints, which will be determined by the detailed functioning of the different subsystems of a big LHC detector, a list of parameters is given below which serve as a guide-line for speed requirements on the front-end electronics. Similar numbers are used in first studies of other detector components [4.1,4.2]:

- Interval between each beam crossings : $15ns$
- Time delay, first level trigger : $\approx 1\mu s$
- Average time between each first level trigger : $\approx 10\mu s$
- Time delay, second level trigger : $20\text{-}100\mu s$
- Average time between each second level trigger : $\approx 1ms$

Another global constraint to be mentioned is power consumption. Specific numbers on this cannot be given at this stage since the question of cooling and detector layout has not yet been clarified. However, it is clearly of great importance to keep the power consumption at the lowest level possible.

4.2 Aims of the Readout Electronics

The main goals of the front-end readout electronics is to provide:

- Very low noise, including minimal distortion of valid information at any stage of the processing.
- Very precise time-tagging to correlate all the signals of interest to the correct BCO.
- Maximum background-free information.
- Minimum pile-up problems.
- No dead-time.
- Selective (sparsified) readout of analog pulseheight values.

In addition, the system must be robust, reliable and easy to calibrate and to verify for functionality.

4.3 Proposed Methods to be Used

We propose to achieve these aims through the following key items:

- Charge sensitive preamplifier.
- Shaper with a peaking-time optimized w.r.t noise, but not constrained to the BCO frequency.
- Time-slicing and preliminary on-chip storage of all useful information.
- Waveform analysis for precise time-tagging of every interesting signal, for handling eventual pile-up effects, and for suppressing background, noise and out-of-time signals.
- Sparsified hierarchical readout scheme.
- Built-in test and verification functions.

4.4 Suggested Implementation

An outline of the proposed front-end readout chip is shown in Fig 4.1. It consists basically of the following main parts:

1. Control block.
2. Preamplifier with shaper.
3. A primary analog storage (pipe-line).
4. An Analog Pulse Shape Processor(APSP).
5. A secondary analog/digital storage.
6. A readout block.

Except for the control and readout block, there will be one each of the other modules for every channel on the chip.

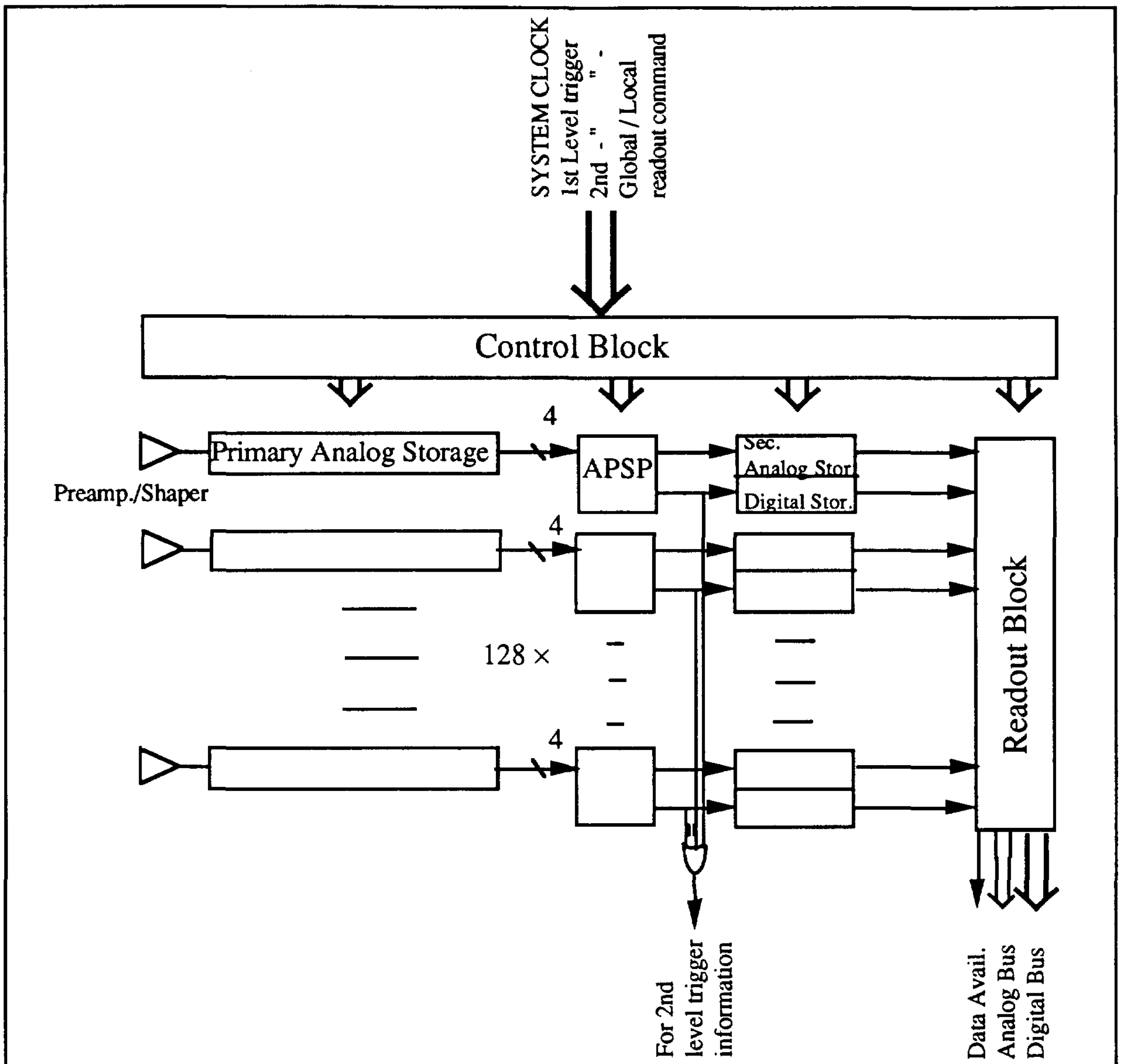

Fig. 4.1
An outline of the proposed front-end readout chip.

The analog time-continuous output from the preamplifier/shaper is being periodically sampled (for every BCO) which transforms the signal into a still analog but now time-discrete form. All of the sampled values will be stored temporarily in the primary analog storage [4.4,4.5].

On a positive 1st level trigger, relevant information i.e. some predetermined samples corresponding to the BCO for which the trigger was for, will be transferred to the APSP. This unit is the *"brain"* of the system having the task of analyzing the analog pulse shape and to make a decision on whether or not the signal fulfils predetermined requirements for being defined as a real hit.

The output of the ASPS, which operates on the speed of the average time between each 1st level trigger, is the analog value of the peak of the shaped output in addition to a digital 'yes/no' signal telling if the event in the channel was accepted or not. Both the values are put on the secondary analog and digital storage respectively. In addition, the 'yes/no' answers from all the channels in the chip, will be OR'ed together and made available on a separate output pin for eventual use in the 2nd level trigger decision.

Upon a positive 2nd level decision (or possibly earlier) the corresponding data will upon request of a global readout command be transferred to the readout block which will take care of performing a hierarchical sparsified readout.

The control block will take care of correct timing including the flow of data in and out of the different modules. In addition it has the important task of buffering information in the storages in the case of consecutive triggers on both levels.

4.5 Choice of Technology

In order to build prototypes of the different subcircuits as the first approach, and later on a prototype of the final front-end chip, a traditional CMOS bulk process will be used. This is convenient for prototype circuits and has the advantage of being cheap in addition to provide easy access and frequent Multi Project Chip runs.

However for the final circuits, it is necessary to choose a technology which is radiation resistant enough to survive the radiation environment at the LHC. For the moment a CMOS/SOI process [6] seems very promising and will probably be commercially available from several foundries in the near future. Yet, from what we know, processes of this type have not been evaluated sufficiently for analog purposes. However, it is likely that a redesign from the CMOS/bulk system into such a process should not cause any particular problems.

4.6 Specifications

Below are listed specifications of the front-end readout electronic which will be aimed for :

- No. of channels per front-end chip : 128
- Power consumption per channel : < 3mW
- Type of amplifier : Charge sensitive
- Type of shaper (filtering) : *CR-RC*
- Shaper peaking-time : $45ns$
- Total gain preamplifier/shaper : $20\text{-}30mV / MIP$
- Detector capacitance (C_d): $\sim 10pF$
- Noise for $C_d = 10pF$ (excl. noise from leakage current) : ≈ 700 $r.m.s.$ e^-

- Type of information provided : Analog pulseheight and digital address
- Readout procedure : Sparsified, parallel and hierarchical
- Discrimination method : Threshold on timing,shape and peak value
- Readout after 1st level trigger : OR'ed digital information (possibilities of full readout)
- Readout after 2nd level trigger : Full readout (if not already done)
- Operating speed zero level : $15ns$
- Available processing time 1st level : ~ $10\mu s$
- Available processing time 2nd level : ~ $1ms$
- Sampling method : Voltage
- Average pitch : $50\mu m$
- Process : Radiation resistant CMOS

4.7 Discussion on the Choices of Methods

A front-end electronic readout system has been proposed which is believed to be a good solution for the application described in this proposal. Below are listed arguments for some of the methods/solutions which have been chosen and which are of a fundamental character:

Charge sensitive preamplifier : It has very good noise performance [4.3] and a wide range of experience is available for this type in these applications.

Analog system : In general, information about the waveform is advantageous to provide:

- **on-chip**, a precise time-tagging and pile-up handling, in addition to excellent rejection of background, noise and out-of-time signals
- **off-chip, off-line**, possibilities of centre of gravity calculations, Landau-correlations and determination of number of charged particles by pulseheight measurements (in particular in the case of γ-conversions).

Time-slicing : It gives the freedom to choose peaking-times of the amplifier with respect to optimal noise performance without being constrained to the time between each BCO. This implies of course that a precise time-tagging is performed at some stage.

Time-tagging : Of course this has to be performed if a peaking-time longer than the time between each bunch crossing is used. However, it should be noticed that even for systems where the peaking-time is constrained to the BCO frequency, situations are likely to occur where out-of-time signals will be erroneously interpreted as real signals which were in reality the tail of a signal from the previous bunch crossing. This is an additional good reason for addressing the problem from the very beginning.

Peaking-time : 45*ns* is proposed because it makes a good amplifier design easy to achieve for reasonable values of power consumption. It also provides excellent noise performance even for quite high values of leakage current. It is also short enough for the time-tagging to be precise.

4.8 Specific R&D Projects

Listed below are the proposed specific R&D projects for the coming two years.

- Evaluation of the performance of the preamplifier/shaper which is already under design.
- Adaption of the already existing analog storage element to this particular application. This includes also working on the interface with the control block.
- Design of the control block.
- Exploration of the properties of waveform analysis (APSP). This includes simulation studies and in particular analysis of experimental data from a real test set-up.
- Design of the APSP.
- Design of the readout block.
- Definition of the digital I/O i.e. signal type and levels. Designing I/O units that corresponds to the definition.
- Definition of a global test and verification procedure for the system including work on how to implement it on each level.
- Assembly of a test system using many submodules, later assembly of a part of the system using complete modules.
- A close interaction with the on-going efforts by other groups, in particular for the evaluation of the CMOS/SOI radiation hard processes.

References

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5. PRECISION MOUNTING, MECHANICS AND COOLING.

Mechanical Structure and Cooling of an LHC Silicon Tracking Detector

One of the most crucial issues which will face the designers of any silicon microstrip tracker for application at the LHC will be the maintenance of the mechanical stability of the detector. Since the goal will be to achieve spatial measurements of a few microns precision, the position of elements of the detector must be maintained to a similar level. This is an especially difficult problem because of the need for a low mass structure and the high heat output, mainly from the local electronics but also from the detectors themselves, which will necessitate cooling on a much larger scale than in previous experiments.

The power dissipation in the electronics is expected to be a few mW per channel and the total heat load is estimated to be several kW. Temperature uniformity of the system is an important consideration, to maintain the structure to ~5μm tolerances, and it may be necessary to maintain the temperature significantly below ambient, to give a margin of safety in noise as a result of leakage current increase.

Some attention has been given to similar problems in the context of a tracking detector for SSC [5.1]. It will be important to consider whethere there are alternatives to the solutions developed there since they involve novel and, for cooling, hazardous materials.

5.1 Cooling

It is obvious that a high precision structure must be carefully cooled to keep it stable to the precision required. This means that, ideally, the temperature should be uniform throughout the tracker and, secondly, that it should be maintained close to a chosen operating point. What is more difficult, without a thorough engineering study, is to say what the tolerances should be. There is a disadvantage in allowing the temperature to rise since leakage currents increase rapidly. Any system will also need to be carefully controlled during shutdowns so that temperature changes occur sufficiently slowly not to distort the structure.

The large heat load rules out many solutions because of insufficient cooling power but it is possible that helium cooling, which is simple in concept, may be viable[Appendix ..] . Detailed engineering studies are required to demonstrate that the cooling can be uniform enough to avoid excessive thermal gradients and, thus, physical distortions.

The proposed SSC solution [5.1] is evaporative liquid cooling whereby a phase change in a working fluid removes thermal energy by its latent heat of vaporisation. An advantage of this approach is that the process can be controlled quite precisely because there is a well defined relationship at equilibrium between temperature and fluid pressure. However although many refrigerant fluids have been considered, all of them - fluorocarbons, amines, hydrocarbons - present serious safety hazards. They require a complex distribution system and, for safety, double enclosure in a nitrogen environment.

The problems of mechanical construction and, particularly, cooling a detector are so great that consideration must be given to them at an early stage. We require dedicated mechanical engineering support with access to computer design tools to evaluate a serious design of a support structure.

5.1.1. Specific R&D Projects

In the context of an investigation of a helium gas cooling system the tasks and time scale planned are:

- estimation of the mechanical stresses and possible deformation of wafers caused by thermal and gas flow loads (Finite Element Analysis) - summer of 1991,
- study of a way of supporting of the wafers against vibration forced by the gas stream - end of 1991,
- experimental confirmation of the results obtained from the thermal and mechanical analysis - spring of 1992,
- consideration of possible detector arrangements inside the tracker and computer modeling of the gas flow through the tracker to improve the uniformity of the gas velocity distribution - summer of 1992,
- construction of a maquette of a quarter of the tracker and measure the gas velocity in all places of interest using the thermo-anemometry technique - end of 1992.

5.2 Microbump Bonding

The number of bond wires needed for a LHC silicon detector can exceed a few million. It is questionable if the wire bonding techniques used to date offer sufficiently high yield and reliability for future application on such a large scale. One possible alternative is to consider the use of bump bonding which could allow the placement of electronic chips directly on the silicon and the construction of convenient modules for assembly and, relatively easy, replacement. There are several possible approaches to the problem:

5.2.1 Solder-Bump Bonding

Imperial College and Rutherford Appleton Laboratory have, in a general context, been evaluating the use of flip-chip bump bonding of microelectronics to silicon detectors. In collaboration with GEC-Plessey Ltd, a first iteration has been completed and further iterations are being planned.

The technique employed [5.2,5.3] is the use of lead-tin solder bumps, where a precise volume of solder is confined between wettable metal pads of known area on each side of the bond, these pads being surrounded by regions into which the solder will not flow. When the temperature is raised to the melting point of the solder (~180°C), surface tension forces tend to bring the structures into alignment. Thus accurate alignment of large number of connections can be made using standard techniques of metal deposition and photolithography.

Precision at the few micron level can be achieved with bond densities of 10,000 in a small area [5.3]. Our efforts, so far, have concentrated on the bumping of RAL MX chips (128 elements at 50μm pitch) to existing silicon detectors. New detectors have been fabricated to take this a stage further by mounting several MX chips on a detector and to examine small arrays of pixels. The results appear to be very promising. Examination of the bonds at several stages of the process has shown highly regular, precisely positioned and shaped metal areas as required. In January this year the first complete units were received from GEC-Plessey and tests are under way to evaluate them. Further devices, of new design, will be bonded later this year.

5.2.2 Resin Technology

Microbump bonding is done by using bump crowns on bond pads and simply gluing another chip onto the detector with corresponding pad layout and bumps aligned back to back. A special insulating resin is needed. The bumps are pressed against each other by the shrinkage stress force of the resin when the resin is set using UV-light.

An automatic bonder of this type has already been used to make an A4 size LED array module [5.4]. To use the microbump technique, the chips have to be aligned with respect to each other, which has to be done anyway, then a chip with corresponding pad layout is pressed on and aligned. This method would speed up the production of detector modules. The joint would be as solid as the detector, and no special caution is needed compared to the bond wires which can not stand mechanical stress. The joint can be opened using a solvent and jointed again up to 30 times [5.4].

The possibility to exploit this technology is under study in Finland.

5.2.3 Conducting Glue Drops

As mentioned above, industrial techniques exist for bump-bonding, but the manufacturers are few (Plessey, Thomson/LETI, IBM, Philips), and iteration costs range from 50 to 250 KSF. Also delivery delays can be quite important. The Centre de Physique des Particules de Marseille (CPPM) has started some R&D work on developing a laboratory-scale bump-bonding method, for quick hybridization of chips with reasonable size (100 connections).

A gluing device has been designed, using micropositioning tables, and drops of conductive glue are deposited onto the silicon chip, by stamping. The drops are spherically shaped, and diameters of 40-50μm are obtained on a regular basis, when producing arrays of few hundreds of connections. Various glues have been tried, in particular b-stageable epoxies, which have two phase-transition temperatures, one that corresponds to drying, the other to polymerisation. A lot of work is devoted to finding, in cooperation with manufacturers, the right glue that would have the correct properties of viscosity, conductivity, stamping ability, room temperature operation,...

In parallel, we have designed a positioning tool to align the two chips, and press them together for bonding. We hope to develop an optical system, based on split-prisms, that would help to align the chips while viewing them from in-between.

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6. MANPOWER, INFRASTRUCTURE AND FUNDING

At this time, ten institutes and two industrial-oriented institutes (IHP Frankfurt and S.I. Oslo) are participating in this study. The manpower allocated to this effort will evolve with time. A number of people signing this proposal have, in addition to the contribution foreseen for this study, responsibilities in on-going projects. There are discussions with further European institutes with expertise in this field, who may decide to join this effort at a later date. In particular, the CPPM (Marseille, France) which is already participating in the R&D proposal for pixel detectors, is planning to join efforts on microbump bonding, irradiations and tests of detectors and electronics chips.

The Santa Cruz Institute for Particle Physics (SCIPP) at the University of California at Santa Cruz will participate in this R&D effort through existing collaborations with participating institutions, which are part of this proposal. These are on-going efforts :

a) Development of radiation-hard silicon strips detectors with Imperial College and University of Turin, geared towards production at S.I.
b) Cooling, alignment and mechanical structures with Cracow University.
c) Data acquisition with Cracow University and Rutherford-Appleton Laboratory.
d) Front-end development with Rutherford-Appleton Laboratory, University of Turin and Cracow University. The emphasis here is on fast shaping and a purely digital readout. Moreover, the superior noise performance and radiation hardness of bipolar technologies are exploited. There exists familiarity with radiation-hard technologies in the U.S.

The fact that this R&D effort at SCIPP is parallel to their HERA/SSC R&D will provide a potential for exploring a variety of technical solutions. Participating SCIPP personnel will be: Hartmut Sadrozinski, Nicolo Cartiglia, Katherine O'Shaughnessy, Daniel Pitzl, Ned Spencer, David Dorfan and Joel DeWitt.

A first preliminary division of tasks, best suited to available or to be created infrastructures in the different laboratories is summarized in Table 1.

Table 2 summarizes a budget request for the first two years of activity. Projects concerning detectors assume that developments will be made in parallel with several different firms. This is essential since it is expected that different technologies have to be investigated to find an optimal solution. The figures indicated in Table 2 are mostly the processing costs of devices in specialized foundries. Point 1 under electronics includes one prototype run each year to develop bipolar front-ends for the Pb-Pb SPS experiment, which will be undertaken by the Turin group. Some special equipment will have to be bought and circuit design and fabrication of PCBs and ceramic hybrids is foreseen. Points 6 and 7 under the heading of electronics cover special equipment not available in participating laboratories. A small amount of travel money is included for allowing people who have limited support from their home institutes to come to meetings and visit firms and pay subsistence for short-term stays at CERN.

Table 1

ACTIVITY INSTITUTE =	1	2	3	4	5	6	7	8	9	10	11	12	13
SIMULATIONS													
(i) Physics performance of tracker		✗			✗		✗						
(ii) Mechanical structures		✗					✗						
(iii) Electronics using CAE tools	✗												
(iv) Detectors	✗	✗											
DETECTORS / TEST STRUCTURES													
(i) Design			✗	✗	✗			✗	✗	✗			
(ii) Evaluation (C-V,I-V)	✗	✗	✗	✗	✗		✗	✗	✗	✗	✗	✗	
(iii) Assembly / bonding	✗								✗				
(iv) Detectors + chip test	✗	✗		✗	✗	✗			✗	✗	✗	✗	
(v) Test beam	✗	✗		✗	✗	✗	✗		✗	✗	✗	✗	
(vi) Bump bond development				✗	✗	✗			✗				
(vii) Mechanical precision mounting	✗								✗	✗			
(viii) Processing			✗					✗					
FRONT-END ELECTRONICS													
(i) Design	✗					✗		✗	✗				
(ii) Prototype device testing	✗	✗		✗		✗			✗				
(iii) Chip testing	✗			✗		✗			✗				
(iv) Systems tests	✗			✗									
(v) Hybrids, special technologies	✗												
(vi) PCB, auxiliary electronics		✗		✗			✗		✗				
(vii) Pure digital design		✗							✗		✗		✗
IRRADIATIONS (e,γ,n,p)	✗				✗	✗			✗	✗			✗
MECHANICS													
(i) Cooling		✗			✗								✗
(ii) Prototypes		✗					✗		✗				✗
ALIGNMENT	✗	✗											✗
DAQ		✗											✗
BEAM TESTS													
(i) Running	✗	✗		✗	✗	✗	✗		✗	✗	✗	✗	
(ii) Analysis		✗		✗	✗				✗	✗			

1 CERN
2 Inst. of Nucl. Physics, Cracow
3 IHP, Frankfurt/Oder
4 University of Helsinki
5 Imperial College London
6 CPPM, Marseille
7 University of Oslo
8 SI, Oslo
9 Rutherford-Appleton Laboratory
10 LEPSI, Strasbourg
11 INFN, Torino
12 Yale University
13 SCIPP, Santa Cruz

Table 2

Estimated Budget for Development of Si Strip detectors,
Front-End Electronics and Mechanical Structures and Cooling for an LHC Si Tracker

	DETECTORS	YEAR 1	YEAR 2
1.	Test structures for radiation hard detectors. Technology variations	75 K	25 K
2.	Strip detector prototypes a. Mask design b. Mask production c. Detector prototype Processing	 60 K 45 K 	 90 K
3.	Design and fabrication of mechanical supports, mounting jigs, Alignment Instrumentation	25 K	20 K
4.	Special instrumentation for Si detector tests (probe station, micro-manipulator, picoampmeters, . . .)	50 K	50 K
		255 K	**185 K**
	ELECTRONICS		
1.	Prototypes of components (Full custom design) Processing	60 K	60 K
2.	Full system single channel Prototype processing		20 K
3.	Full size chip processing		40 K
4.	a. Evaluation of SOI technology available at IHP Frankfurt Radiation test of devices b. Design and process on circuit in IHP 501	50 K 	 70 K
5.	External VLSI design	35 K	50 K
6.	Auxiliary electronics	15 K	15 K
7.	DAQ equipment	30 K	30 K
		190 K	**285 K**
	MECHANICS		
1.	Prototype work	10 K	10 K
2.	Special Instrumentation	40 K	
3.	Microbump bonding	100 K	100 K
		150 K	**110K**
	TRAVEL	**40 K**	**40 K**
	TOTAL	**625 K**	**620 K**

7. REQUESTS TO CERN

Knowledge on both Si strip detectors with capacitively-coupled diodes and integrated polysilicon resistors and on design and test of front-ends of the kind proposed exist in the CERN group. It is therefore considered to be most efficient for this group to take on the responsibility for the design and test of the proposed analog/digital front-end system and for design and test of radiation-hard test structures and detectors, including SOI technology evaluation, in collaboration with IHP Frankfurt. The funds which will be requested from CERN for this part of the programme amount to approximately 260 KSF per year, including travel and subsistence.

Other support which will be requested from CERN is (i) use of a high-energy test beam for about 14 days main user time in 1992 and 1993 each, and (ii) computing support, in particular for physics and detector simulation and for engineering projects (CAE).

APPENDIX A.

DESIGN REQUIREMENTS FOR SILICON DETECTORS AND READOUT CHIPS FOR THE LHC BEAUTY EXPERIMENT

The silicon detectors for the LHC Beauty experiment [A.1] will be arrayed in about twenty planes perpendicular to the beam axis, distributed throughout the interaction region. Each plane will contain four detectors, approximately *5cm* on a side, with diode strips on both faces to measure vertical and horizontal coordinates. The inter-plane spacing will be approximately *4cm*. A small gap (a few millimeters) will be left between upper and lower halves to allow passage of the circulating beams. The detectors themselves should be no thicker than $200\mu m$ and should have a readout pitch between $25\mu m$ and $50\mu m$. Each detector will have about 2000 x and y strips (for a pitch of $25\mu m$) totalling $2000 \times 2 \times 4 \times 20 = 320{,}000$ readout channels.

The radiation dose to the detectors will likely be dominated by charged particles emerging from pp collisions. The experiment does not have 4π calorimetry so damage from slow neutrons should be small and since the detector is withdrawn from the proximity of the beam during manipulations, the incidental radiation dose from beam set-up, injection and acceleration is minimized. We thus estimate [A.2] that at a luminosity[1] of 10^{31}, a corner of a detector located *2mm* from the beam will receive a dose of *6.7Mrad* during a one year run. The dose decreases as the square of the perpendicular distance from the beam to a level of *13krad* at the location of the readout electronics.

The silicon microvertex detector furnishes hit information to a high-speed data-driven processor which provides a Level-2 trigger based on event topology. The Level-1 trigger will be a simple interaction trigger which produces about $7 \cdot 10^5$ interactions per second at a luminosity of 10^{31}. The silicon hit information for all of these triggers must be read out and processed. Assuming the detectors are read in parallel and that the average hit multiplicity per detector is 9 (based on ISAJET simulation), the readout system must be able to sustain a rate of $6.3 \cdot 10^6$ hits per second. In the simulation work done for P238, it was found that even without pulseheight information from diode strips, it was possible to efficiently trigger and cleanly reconstruct B-mesons. Clearly, however, if the pulseheight could be read out sufficiently quickly, the additional resolution would be advantageous both at the trigger level and the reconstruction level.

The requirements on gating speed are more relaxed than those for s full-luminosity LHC experiment. In a *100nsec* gate, for example, the number of gates containing more than one event is 0.07 times the number of gates containing a single event at a luminosity of 10^{31}.

1 This luminosity is a compromise, which appears to allow a meaningful measurement of CP-Violation (see reference in [A.1], while keeping the trigger, spectrometer, and data rate requirements to a manageable level.

Most of the superimposed events could be eliminated using real-time calculations on signals from a time-of-flight hodoscope. Thus a preamplifier risetime of the order of 100*nsec* would be adequate. Nonetheless, a chip capable of resolving 15*nsec* bunches would simplify the task of reducing false triggers due to superimposed events.

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[A.2] D.E. Groom, Proc. of the ECFA Study Week on Instrumentation Technology, Barcelona, Vol. 1, p. 103.

APPENDIX B.

REQUIREMENTS AND PERFORMANCE SPECIFICATIONS FOR FRONT-END ELECTRONICS

Constraints

Analog or Digital system

An analog system is defined to be a system where the full analog pulseheight information is being read out, whereas a digital system is a system where a simple yes/no decision is being made at the earliest stage such that this is the only information available for the outside world. In the following it is assumed that a purely digital system has to be designed with shaping times below 15*nsec*. In the case of an analog system, longer shaping times can be tolerated, since the data can be validated through time slicing.

Argument for basing a readout system on analog readout:

- Adequate analysis of the pulse-form will allow optimal rejection of noise, background and out-of-time signal via time tagging.
- Provides possibilities for correcting wanted signals for possible pile-up.
- Time slicing allows longer shaping times which again reduces the speed and power constraints on the amplifier.
- Increased immunity to excess external noise or pick-up.
- In the off-line analysis it may allow
  - (i) to obtain better spatial resolution because centre of gravity calculations can be performed.
  - (ii) possibilities to use Landau correlation to reduce the ambiguity problem.
  - (iii) to determine number of charged particles by pulseheight measurement, in particular in the case of γ-conversions.

Arguments against an analog system:

- Possible increase in the front-end complexity. (Not necessarily true. Discussed later).
- The need for analog to digital converters. (Not necessarily fast ones)

Here it is assumed that a readout system preserving analog information is advantageous, if it can be achieved without too many complications compared with a purely digital system.

Noise

Given the relatively small signal from Si strip detectors (~ 24,000 e for the typical 300 μm thick detectors), good noise performance of the front-end electronics is essential. From past experience with Si vertex detectors, it is clear that one should try to achieve the best possible noise performance, however keeping in mind that in the case of the LHC the noise from detector leakage current will play an important role, given the high radiation levels these detectors have to be operated in. Design considerations can, however, not be based on achievable noise figures alone. A given design will always be a trade-off between noise, power and speed. This is discussed in detail in a later section.

Power consumption

A first consideration of the trade-off between noise, speed and power consumption indicates that it is not likely for a system like this to go much below a value of P =3mW per complete front-end channel. However, this should be aimed for as to be the maximum allowable value. This is consistent with other proposals for silicon detectors for LHC [B.1], but the value is several times bigger than suggested for similar projects at the SSC [B.2].

On-chip data reduction/Sparsification

In order to reduce the amount of data to be read out of the system it is clear that on-chip data reduction is necessary.

The proposed method is to transfer the addresses and analog pulseheight value of those channels which fulfil given constraints. In addition, for centre of gravity calculations, the analog pulseheights of the neighbouring channels are also made available.

The data will be prepared for sparsification in the available time after the 1st level trigger but the real execution of the data reduction will take place during the transmission.

Robustness/Testability

Because of the complexity of a detector like this, it is more important than ever that the system is robust, reliable and testable.

One of the most important parameters with respect to robustness and reliability is the radiation hardness. The electronics is supposed to survive annual radiation doses of $>10^4$ Gray of charged particles and ~ 10^{13} of neutrons per cm^2 [B.3,B.4]. This will be discussed further in a section about choice of technologies.

The system must have efficient built-in test facilities for verification and calibration. This will be included as a part of the development from the very beginning.

Other constraints

The layout pitch of the front-end chip should on average equal $50\mu m$.

Noise Considerations

The goal of this section is to determine a peaking- (shaping-) time T_p , which is the best compromise between performance and practical considerations. Here, we assume that we really have the freedom to choose between different peaking times, i.e. to have a shaped signal that might extend over several beam cross-overs (BCO's). The validity of this assumption will be discussed in the next section.

Relevant noise-sources

There are two major sources of noise to take into consideration. These are:

- White noise mainly generated in the input transistor of the front-end preamplifier. Also the series input resistance can contribute to this noise.
- Shot noise generated by the detector leakage current. This is originally white current noise, but if to be compared directly with the electronic white noise which is a voltage, it exhibits a $1/f^2$ behaviour because of the inherent filtering in the detector itself.

Because of the different behaviour in the frequency domain of the two sources, it is clear that the total *ENC* coming from these two sources also exhibit different behaviour with respect to the peaking time (when referring to the time domain) [B.5].

The impact of T_p upon *ENC*

The expression for the total *ENC* can be expressed (including only parameters that are relevant for this discussion) :

$$ENC_t = \sqrt{ENC_p^2 + ENC_d^2} = \sqrt{\alpha/T_p + \beta I_d T_p} \tag{B.1}$$

where ENC_p and ENC_d are the individual *ENC* for the preamplifier and detector respectively. The values of α and β are determined by the choice of filter type, the transconductance (g_m) value of the input transistor, the total input capacitance and temperature. Exact values for α and β can be found in [B.5].

From this expression, one can derive what will be the optimum choice of peaking time with respect to lowest possible *ENC* :

$$T_{popt} = \sqrt{\frac{\alpha}{I_d \beta}} \tag{B.2}$$

For a first estimate of T_{popt} it is assumed to have a *CR - RC* filtering, $g_m \cong 4mA/V$, a total input capacitance of gate and detector of $C_t \approx 12pF$ and T ≈ 300°K. As has been argued in section 3. , it is expected that detectors running for 3 years with an average luminosity of ~ 50% of the maximal $10^{34}\ cm^{-2}\ sec^{-1}$ will have a rather high value of leakage current, due to long term radiation damage, of $I_d = 3\mu A$. This may be a pessimistic assumption, seeing that there are probably possibilities of making detectors more radiation hard. It should be noted that in the case of a Si vertex detector, radiation damage from charged particles is expected to dominate over radiation damage caused by neutrons. These assumptions lead to a value for T_{popt}:

$$T_{popt} \approx 25\ ns \tag{B.3}$$

An important aspect to take into account is the total charge collection that can be achieved for a given peaking time. For the sake of comparison with a purely digital system, we discuss the case of $T_p = 15$ns for a digital system. Talking in terms of efficiency (η), this has in more traditional much slower systems been assumed equal to 1 since the charge collection time has been much shorter than the peaking time. However, this is not true in this case and the effect of having a value of η less a 1 will directly be reflected in the overall *ENC* of the system.

Taking this into account, the expression for the equivalent *ENC* for very fast systems becomes:

$$ENC_t = ENC_t'/\eta = \sqrt{\alpha/T_p + \beta I_d T_p}/\eta \tag{B.4}$$

Now, rather than deriving a new expression for T_{popt} from this equation, which is impossible because of the lack of knowledge of the exact mathematical T_p dependence on η, the following exercise can be performed:

So far, few studies of the effective charge collection time (which determines η) in heavy irradiated detectors have been done [B.6]. A reasonable assumption is :

$$\eta(T_p = 15ns) \approx 0.7 \tag{B.5}$$

while

$$\eta(T_p = 45ns) \approx 1 \tag{B.6}$$

For the same numbers of α, β, and using the value of $I_d = 3\mu A$ per strip, using (B.4) the *ENC* value for the two peaking times becomes for this example:

$$ENC_t(T_p = 15ns) = \sqrt{1200^2 + 720^2}/0.7 = 2000\ [r.m.s\ e^-] \tag{B.7}$$

$$ENC_t(T_p = 45ns) = \sqrt{690^2 + 1250^2/1} = 1430\ [r.m.s\ e^-] \qquad \text{(B.8)}$$

The conclusion is that with an expected realistic leakage current of $3\mu A$, the noise figure is much better in the case of $45ns$ peaking time than it is for a peaking time of $15ns$. For lower leakage currents, longer peaking times will be even more advantageous. The *average* leakage current, over the whole detector and over a lifetime of 3 years, is expected to be significantly lower than the worst case value.

Practical design considerations

From the point of view of the preamplifier/shaper design, a longer peaking time than the minimum ($15ns$) seems to be very preferable. Recent studies indicate that if a traditional charge-sensitive preamplifier in CMOS is to be used, a peaking time of a few times this value makes the design a lot easier to achieve for a typical analog CMOS process of today (SOI technology is not likely to change much with respect to this). The argument for using CMOS technology is that it is well established for low-noise charge-sensitive preamplifiers.

In a later section, we explain that it is possible to use a longer peaking time than the bunch crossing time, and consequently we propose to do this because of the benefits with respect to the noise performance as well as reduced design constraints (i.e. less power consumption requirement).

Choice of filter type

Making a compromise between the desire for simplicity and for minimizing of the power consumption, it is likely that the commonly used $CR - RC^{(n-1)}$ [B.5] type of filtering is the best choice. With respect to the choice of number of integrating poles (n) there are some few remarks:

- A filter with more integrating poles (n) would improve the electronic performance w.r.t the detector shot noise. In addition it would also give a shorter tail of the shaped output which might be an advantage if the occupancy is high.
- However, there is a disadvantage in that for a given peaking-time of the system, the more integrating poles the higher speed is required. This is due to the relationship:

$$\omega_c = \frac{n-1}{T_p} \qquad \text{(B.9)}$$

where ω_c is the centre frequency of the filter. Higher speed would require more power and consequently it will be advantageous to use a filter with minimum n , i.e. $n = 2$ corresponding to the simple $CR - RC$ filter.

- Another drawback of having many integrating poles is that the abruptness of the output signal at the moment when the signal arrives is reduced. As described in a later section, this abruptness might serve as a very efficient time tag for the signal. In this case, the CR - RC filter is the best choice.

The conclusion is that the use of the simple CR - RC filter is adequate. Therefore this type will be proposed to be used.

Time-Tagging and Occupancy

In this section an attempt is made to discuss whether or not one has the freedom to choose peaking times longer than the time between each beam cross-over and, if so, what happen and what are the limitations.

Of course, the use of peaking times that will produce a pulse shape extending across several BCO's will introduce some concerns, namely increased occupancy and uncertainty in which beam-crossing slot the event took place. These have been simulated [B.7] using calculated pulse shapes and noise digitized from a sampling oscillator.

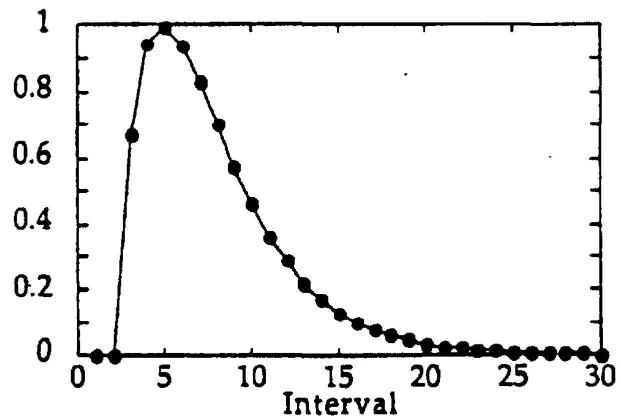

Fig. B.1
Normalized ideal *CR-RC* pulse.

Figure B.1 shows an example of a pulse, normalized to its maximum value, as it might be made time-discrete at LHC using an amplifier with a time constant of 45*nsec*. In this example the pulse originates in time slot 2.

Figure B.2 shows the effect of combining noise with pulses whose maximum values are 3×, 6×, 9× and 12× the r.m.s. noise.

An algorithm for pulse processing must ensue high acceptance for the minimum signal possible, while simultaneously offering good rejection of noise, at a level much less than the time occupancy if possible.

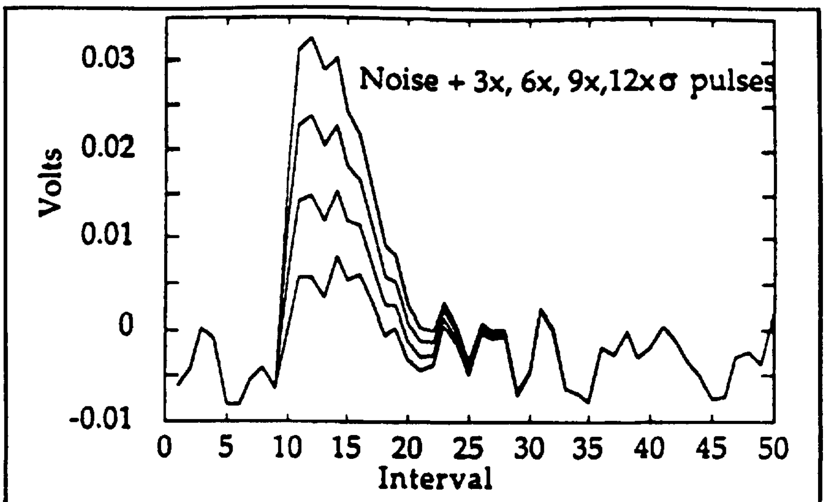

Fig. B.2
Simulated pulses with noise present.

Several algorithms have been evaluated. A promising example requires (referring to the interval numbering in Fig. B.1) :

$$(v_5 - v_2) > \text{threshold}_1$$

$$(v_3 - v_2) - (v_2 - v_1) > 0$$

$$(v_3 - v_2) > \text{threshold}_2$$

In other words, the expected maximum pulseheight is discriminated and an abrupt, positive change in amplifier output level is required in the beam-crossing slot being tested.

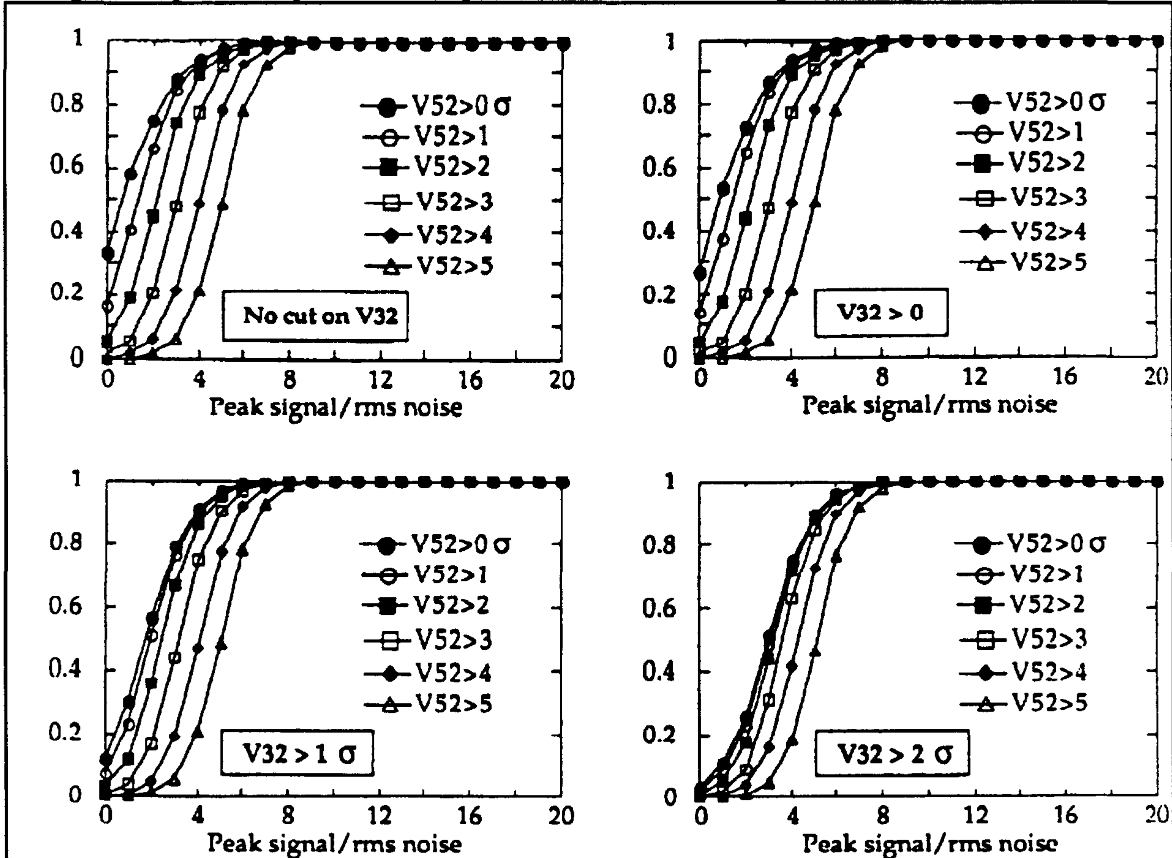

Fig. B.3 Acceptance of simulated events using algorithm III with various thresholds on v32 in units of σ_{noise}.

Some of the results are shown in Fig. B.3. They show that a cut on $v_{52} \geq 4\sigma$ will give good performance on both the required criteria. (Zero peak signal implies only noise was present for the test.) Further work is required to optimize the algorithm and ensure maximal noise rejection.

However, the algorithm already has promising performance against pile-up. The efficiency of the algorithm is reduced slightly for about 10 beam crossings when a pile-up of two similar size pulses occurs. The false trigger rate for this algorithm for time slots close in time to genuine events is < 2% in the slot following a genuine signal and $\leq 10^{-3}$ in all other cases.

Figure B.4 shows fraction of events passing the algorithm with specified setting, in the case of signals arriving before the trigger. Clearly there is a reasonably good rejection in all the examples in the figure.

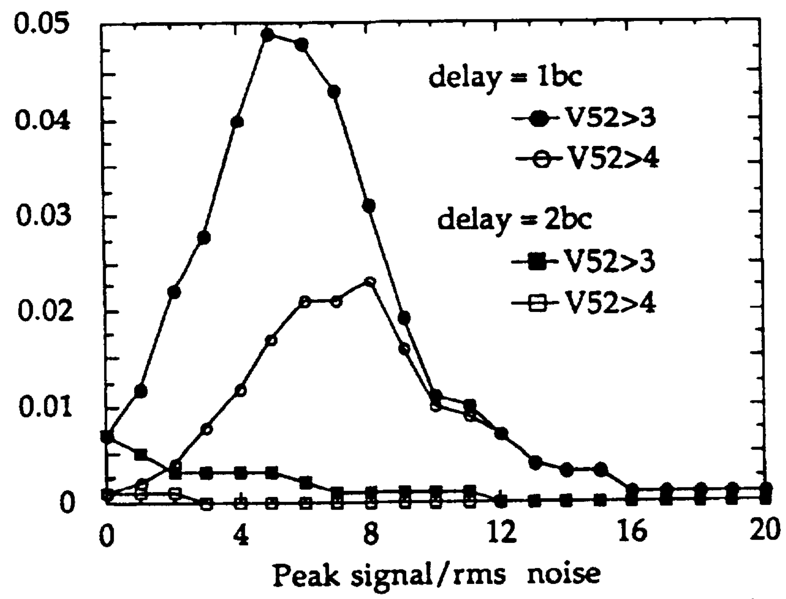

Fig. B.4
Fraction of events passing the tests described.
The cuts are in units of r.m.s. noise.

PROPOSED CHIP AND SYSTEM SOLUTION

Front-End

Based on the conclusions drawn in the previous subchapter, the proposed outline of the front-end chip is shown in Fig. 4.1 in Chapter 4. It consists of the following basic building blocks:

Control unit.

This is a fully digital block that takes care of the distribution of all the timing signals for the other blocks. This includes the control of data flow between each processing stage. The input to the block will be such as main system clock, 1st/2nd level trigger and global/local readout commands.

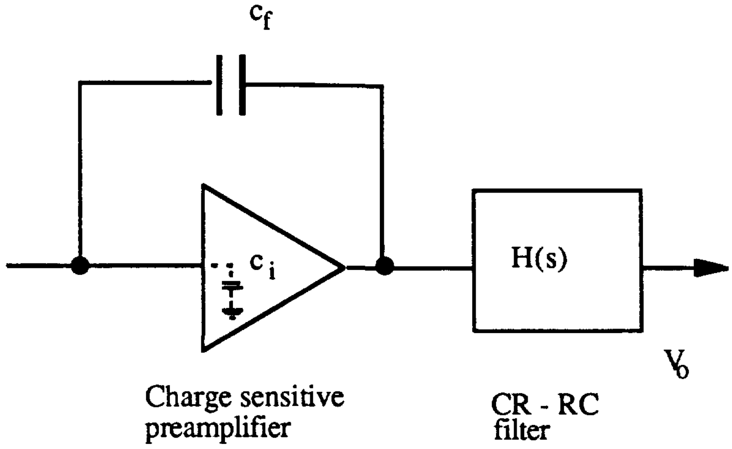

Fig. B.5
Charge sensitive preamplifier with filter.

Charge sensitive preamplifier with shaper

For this part ,the typical configuration shown in Fig. B.5 will be used. The details of the principle is described elsewhere [B.5,B.8]. The main difference for this particular application is that attempt will be made to optimize the design with the following constraints in mind :

- $T_p = 45ns$
- Gain ≈ 20-30mV/MIP
- Power consumption ≈ 1.5mW

Using these numbers, a design has already been worked on to give an expected noise performance of (excluding the noise generated by the detector leakage current):

$$ENC_p / C_t \approx 60\ r.m.s.\ e^- / pF \qquad (B.16)$$

where C_t is the total input capacitance.

Consequently for $C_t \approx 12pF$, corresponding to a detector capacitance of $C_d \approx 9pF$ and an inherent input capacitance of $C_i \approx 3pF$:

$$ENC_p \approx 720\ r.m.s.\ e^- \qquad (B.17)$$

Primary/secondary analog storage, digital storage.

The basic analog storage elements (pipe-lines) needed in this system have been proposed and are described elsewhere [B.1,B.9]. The pipeline basically consists of an array of capacitor elements. It is organized as a ring buffer such that the data can only be stored for a limited predetermined time before it is being overwritten by new data. The minimum storage time for the primary storage must be more than the time delay of the 1st level trigger, while for the secondary it must be more than the time delay of the 2nd level trigger.

The digital storage is simply a shift-register.
The timing and the control of data flow in and out are controlled by the control block. The time-continuous output of the shaper will be sampled directly on to the cells. It's a voltage type of sampling which makes it unlikely to have nonuniformity problems.

Analog pulse shape processor (APSP)

The APSP constitutes the local intelligence of the system and is also the element that makes this concept fundamentally different from other similar on-going projects [B.3,B.9]. The element will take the 1st level data from the primary storage and process them analogically using a simple algorithm like the one discussed in the section about time tagging. An outline of the suggested principle is drawn in Fig. B.6 (see also Fig. B.7 for additional information). The timing of this module is also performed by the control unit.

The goal of the APSP is to obtain the best information whether or not the signal fulfils given constraints that defines it for being a real signal. This implies that the signal is above a certain threshold and that it really belonged to the correct BCO. Keep in mind that if the shaped signal extends over several BCO's, there will be a huge number of channels with output levels above threshold, but which are not belonging to the correct BCO.

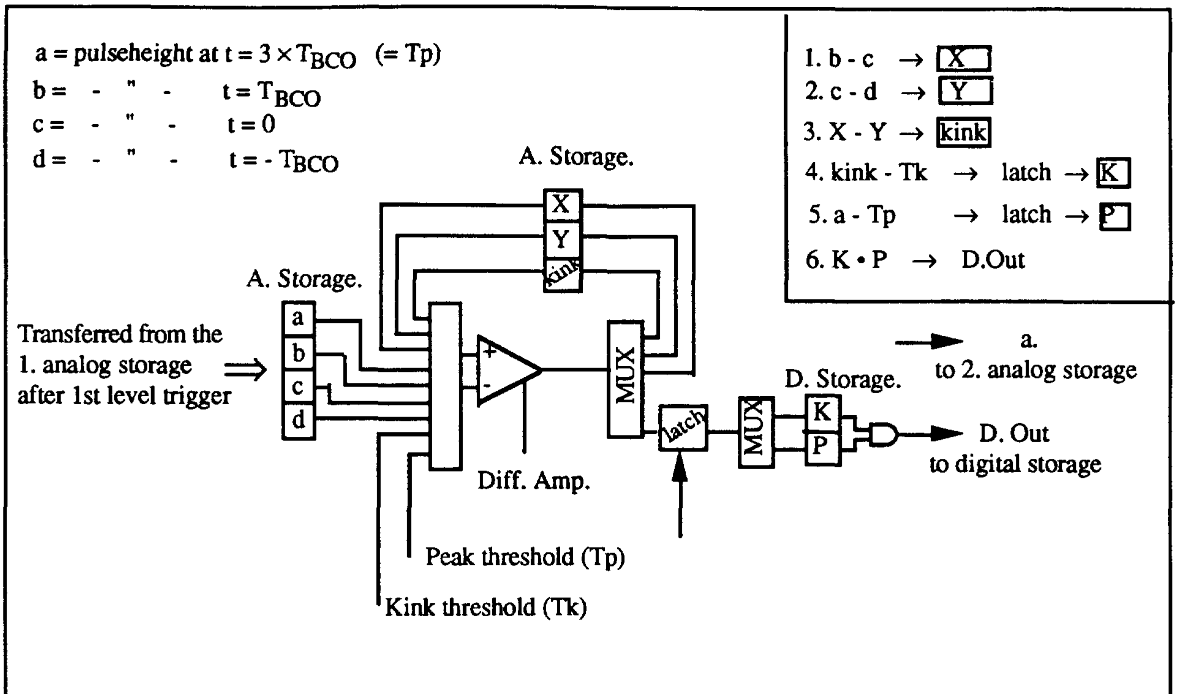

Fig. B.6
An outline of the analog pulse shape processor (APSP).

The output will be a 'yes/no' answer which will be put on the digital storage in addition to the single sample for $t = T_p$, which is the analog pulseheight value, which will be put in the parallel secondary analog storage.
The design will be facilitated due to the low speed requirements at this stage (~ $10\mu s$ for the whole operation). For the same reason also the power consumption required is likely to be low.

Readout block

This block takes care of proper readout. Whenever a global readout command comes, it will take the corresponding data from one slice in the secondary analog/digital storage of all channels and prepare it for readout. Immediately it will flag whether there was any hit channel or not on the chip. If there was, it will upon request of a later local readout command dump the data on the output buses in a parallel sparsified form.

Specifically, this will be only the addresses of the channels having a 'yes' decision in the digital storage together with the corresponding analog information plus the analog information of the two neighbouring channels. The compacted information will all be read out in parallel which will require 7 digital address lines and 3 analog pulseheight lines.

General Description

The system is based upon the time-slice principle which means that the analog time-continuous output from the preamplifier/shaper is being periodically sampled (for every BCO) which transforms the signal into a still analog but now time-discrete form. Thus, if a real signal is coming, the sampled output will look like in Fig. B.7, assuming a peaking time of 45*ns* and that the timing of the sampling is such that there is one sample just before the beam crossing. All of the sampled values will be stored temporarily in the primary analog storage.

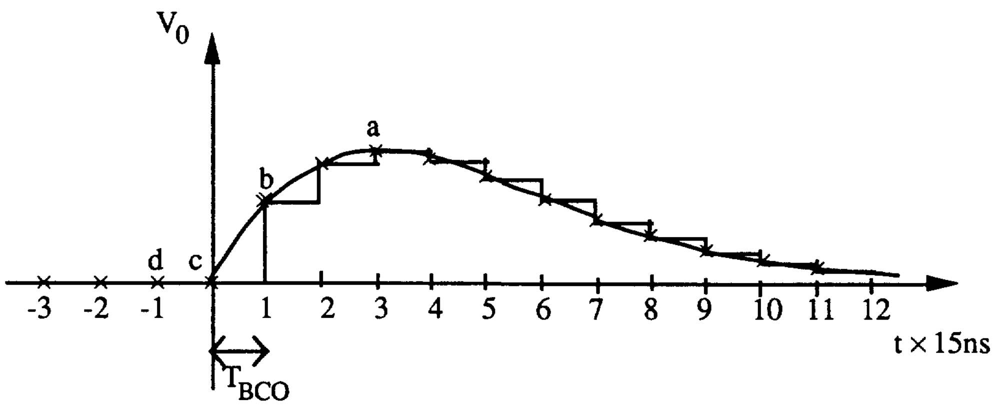

Fig. B.7
Time slicing of a CR - RC shaped signal from preamplifier/shaper periodically sampled and stored in the primary analog storage.

On a positive 1st level trigger, relevant information, i.e. some predetermined samples corresponding to the BCO for which the trigger was for, will be protected from being overwritten and transferred to the APSP whenever this is ready to process this data.

During processing, the control block will not allow a new transfer of data to the APSP even if more 1st level trigger occurs. It will just only protect the relevant data inside the primary storage from being overwritten and leave it waiting in line. Because of this, the primary storage needs some additional cells in case of pile-up of 1st level triggers. No data will be lost.

In addition to the transfer of the data to the secondary storages after the processing is done, the 'yes/no' answers from all the channels in the chip, can be OR'ed together and made available on a separate output pin for eventual use in the 2nd level trigger decision.

Upon a positive 2nd level decision the corresponding data will, similarly to the transfer on the 1st level trigger, either be kept waiting in the storages if the readout block is busy, or upon request of a global readout command telling that the previous readout has finished, be transferred to the readout block.

Data Acquisition

So far, only the interface to the DAQ has been discussed. Contact with people participating in relevant R&D efforts has been established and concepts will be worked out together with the groups involved in the developemnt of higher level data acquisition systems.

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APPENDIX C.

REQUIREMENTS FOR A COOLING SYSTEM AND AVAILABLE TECHNOLOGIES

We can define the requirements for a hypothetical silicon strip tracker as follows :

- total power dissipation	about 8 - 25kW
- temperature stability	0.2 deg
- wafer temperature	-20 till +20 C
- local differences of temperature	less than 5 deg

This specification corresponds to a few millions of readout channels, each using $3mW$, i.e. a few thousands of individual silicon strip detectors. If such an assembly occupies a small volume of $1m^3$, then we could consider the following methods of cooling, which potentially satisfy the above requirements:

a) liquid circulation in close channels being in direct/close contact with VLSI electronics [C.5]

b) evaporation of a liquid in close channels using conventional heat pipe technology [6] or micro refrigerator ideas [C.7],

c) open evaporation cooling [C.8]

d) open gas cooling [C.3].

Preliminary Evaluation of an Open Gas Cooling Capability

Seeing a lot of flexibility and advantages of a gas cooling system, we have made a preliminary evaluation of a possible efficiency of this kind of system.

The following assumptions were taken as an input data :

- all the tracker is closed in a tight envelope which forms, together with a mechanical structure, a kind of channel for the gas flow,

- helium gas, having very good thermal properties, is used as a cooling medium,

- all the wafer edges are exposed on the gas stream and the VLSI chips are placed close to these edges

- the silicon wafers are used as radiators for heat transfer from VLSI electronics to the cooling gas.

Based on the above assumption a preliminary study of heat transfer for a wafer in a gas stream was made. Fig. C.1 shows the model that was taken for the evaluation of efficiency of gas helium cooling system for silicon detectors. The results for a flow of $5m/s$ are shown in Fig. C.2.

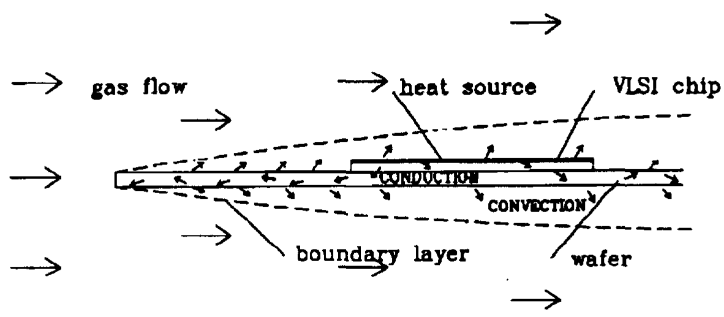

Fig. C.1
Model taken for evaluation of efficiency of gas helium cooling system for Si detectors.

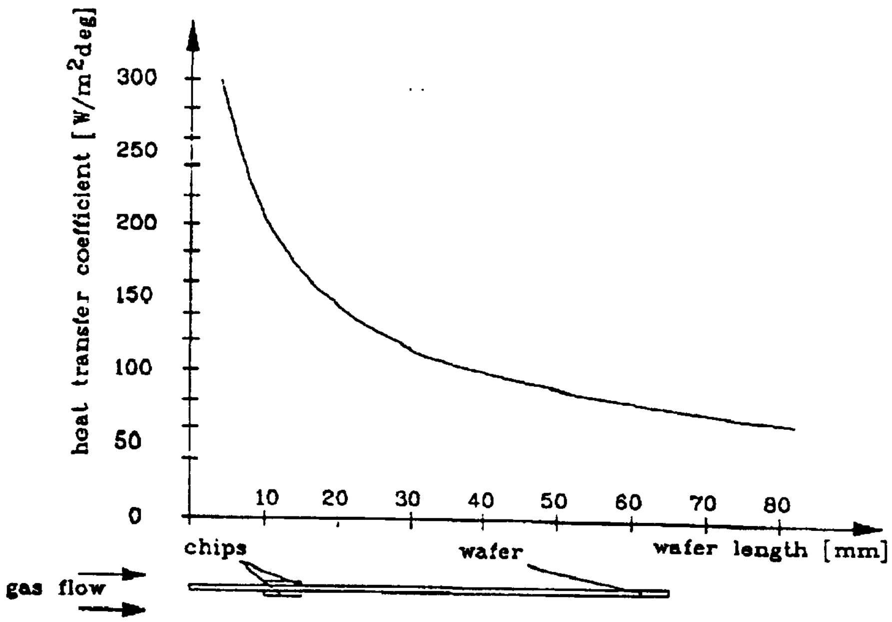

Fig. C.2
Heat transfer coefficient as a function of length of the wafer.

The heat transfer coefficient as a function of length of the wafer was calculated based on the Prandtl boundary layer theory in a laminar flow [C.1]. The coefficient depends linearly on the thickness of the boundary layer [C.2]. The layer is formed from the edge of a wafer and starts from zero thickness.

The temperature distribution inside the wafer foreseen with the Finite Element Analysis system MSC/cal is shown in Fig. C.3. using the following input data for the analysis :

- detector is double-sided	
- wafer length	- 65*mm*
- wafer thickness	- 300μm
- thermal cond. of Si	- 129W/mK
- helium velocity	- 5m/s
- pitch of strips	- 50μm
- length of chip	- 5*mm*
- power dissipation	- 1$mW/channel$

the VLSI chip is placed 10*mm* from the edge of the wafer.

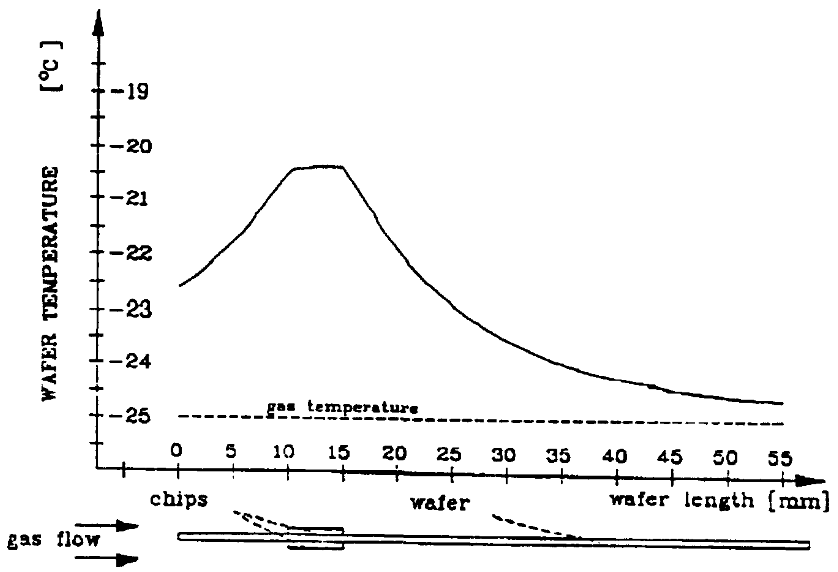

Fig. C.3
The temperature distribution inside a wafer calculated with the Finite Elements Analysis system MSC/cal.

The max wafer temperature is below -20*C*, when the gas temperature is only -25*C*.

This estimation shows that there are possibilities of designing an efficient gas helium cooling system for a Si tracker. This kind of system is not easy to design, needs much development work and has strong influence on a support structure design but it could provide some important advantages:

- very low mass inside the tracker
- simple control system with a wide range of temperature available
- long term and safe operation

- low temperature differences between the gas and wafers with high thermal stability (an important condition for a good mechanical stability)
- the dry gas flow in a tight loop allows operation at low temperature without water condensation

Requirements for a Mechanical Structure when Helium Gas Cooling is to be Used

A detector arrangement and a mechanical structure should be designed having in mind the following requirements:

- The mechanical structure has to form a suitable channel or channels for the gas flow along wafers,
- edges of all wafers, where VLSI chips are placed, should be exposed to gas flow.
- in the chip region and close to the wafer edges gas velocity should be close to $5m/s$,
- there has to be space for a supply and an exhaust of the gas,
- to cool down the detector to $-20C$ the wafers should be fixed only on one side with the second edge having a kinematic support giving necessary freedom for thermal expansion,
- the material chosen for the mechanical structure should have an expansion coefficient as close as possible to that of the silicon.
- the mechanical structure should have good immunity to mechanical vibration.

References

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[C.5] DELPHI microvertex cooling system.

[C.6] Noren Products Inc., 1010 O'Brien Dr. Menlo Park CA 94025.

[C.7] MMR Technologies, Inc. 1400 Stierlin Road, Suite A-5, Mountain View, CA 94043.

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