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RD19: Status report and Addendum Development of hybrid and monolithic silicon micropattern detectors

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Summary

In 1991-92 our prime achievement has been the first demonstration in a high multiplicity experiment of the feasibility of high speed, active silicon pixel detectors with integrated readout electronics. The hybrid detector has binary output with a readout string of 16-bit words for a matrix of 1006 cells of 75 μm x 500 μm. It achieved a precision of 25 μm and a noise level of 100 e^- r.m.s. Comprehensive analysis of the data shows an efficiency of better than 99.2 % and a threshold non-uniformity of 750 e^- r.m.s. Further studies have led to a number of design improvements, many of which have already been implemented in a new detector, to be constructed as a 50 mm x 50 mm array in the summer of 1993.

Objectives of the development in 1992 have been the increase of the size of detecting area without loss of efficiency, the reduction of material thickness in the detector, understanding of the threshold non-uniformity and study of the sensitivity of the pixel matrices to light and low energy electrons for scintillating fiber detector readout.

Apart from the hybrid detectors we have implemented and tested a number of monolithic structures in a Silicon-On-Insulator (SOI) technology which show the feasibility of this approach. Finally we have also made a small analog pixel array.

We produced 4 technical notes and published 6 papers to which we refer for the details of our results. This report is focussing on our plans for the coming 3 years and the budget for 1993.

A. INTRODUCTION

We like to define the micropattern particle detector as the semiconductor device that consists of a matrix of contiguous particle sensing elements with dimensions between ~10 μm and ~500 μm which have an individual signal pulse amplifier, comparator, memory, etc. with similar cell size connected to each sensor element and for the whole matrix an intelligent readout architecture that provides the user with a pattern (true 2-dimensional coordinate information) of the hits at every chosen timeframe. The detector may be built monolithically in a single semiconductor chip or it may be in a 'hybrid' form, with the 'sensor-chip' connected by bump-bonds to the 'readout-chip'. Characteristic features of this type of detector are the incorporated signal processing at a microscopic level and (part of the) information extraction operations already on the detector. This should allow its use in high multiplicity and high rate environments in the future hadron colliders, heavy ion and B-physics experiments. In comparison, earlier silicon pixel detectors like the Charge Coupled Device, useful as they are at low rates, are different in that they 'passively' integrate the signal current together with the dark current on the matrix elements and the complete matrix has to be scanned in order to recognize the particle hits. Because in CCD there is no electronics in the pixels, the pixel size can be smaller.

Status

At the end of 1991 we have tested the world's first hybrid silicon micropattern particle detector in the 'Omega-Ion' experiment WA94 at CERN [1]. The detector combines a two-dimensionally segmented silicon detector of 1006 sensor elements in 16 columns and 64 rows with a geometrically identical matrix of electronic readout circuits with fast, low-noise pulse processing electronics in each cell. During 1992 we have analysed the data from this test [2] and made a detailed study of the characteristics of the electronics [3] in order to improve the performance. An overview article [4] is appended to this status report.

In parallel with the work on the hybrid device a group in RD19 is developing in collaboration with IMEC(Leuven) an adapted Silicon-On-Insulator (SOI) processing technology. In this process we have manufactured working detectors with a reverse leakage current of 10 nA cm^{-2} , CMOS components have been tested and electrical parameters determined. Simple amplifier circuits are currently under test. The status of the SOI development has been presented in the 1992 Nuclear Science Symposium/Orlando [5,6,7] and the main article is also appended.

Until now we have been relatively modest in our performance targets for the binary pixel circuit. We aimed at proving feasibilty in the Omega fixed target experiment instead of pushing immediately for LHC objectives. The reasons for this are two-fold. It was important to encounter and understand the practical problems associated with building a micropattern detector for a real particle physics application. We have been able to overcome many of these problems by

addressing them one-by-one by virtue of the fact that we had some margin between our targets and the requirements of the Omega experiment. The other reason for our approach was to increase the level of confidence in the particle physics community in what has been considered a rather exotic detector. We think we have now achieved these aims and are ready to go forward to address the specific problems of the LHC p-p collider environment.

Therefore we propose at this moment to update the plans of RD19 in order to focus the R&D program on the high particle multiplicity, high rate environment of the LHC. Discussions on the application of the micropattern detectors in the inner vertex and tracking detectors of the potential LHC experiments: ATLAS, CMS and the heavy-ion collaboration LHC-HI are conducted in parallel with a continued generic technical development. For the moment the direction of the R&D is still more determined by general technological considerations than by precise differences in requirements between these potential users. They all benefit from a common effort, keeping in mind that making devices of the projected sophistication may strain personnel resources in particular beyond those available now in the particle physics community. Inspiration and practical solutions may be found also in related fields [8].

Objectives and phases of the R&D plan for 1993-1995

A number of areas of technological activity can be distinguished. Each of these require a specialist approach, involving close collaboration between industry and particle physics institutes. In part B, in sections 1 to 8 a description is given of the main areas in which development has to be done to arrive at the construction of a reliable LHC micropattern detector.

By the end of 1995 the basic concepts for a semiconductor micropattern detector for use in the highest-luminosity version of LHC should have been established, preferably in the form of operational prototypes. In order to show the crucial aspects in a realistic way we will participate in the installation of less advanced systems in running experiments, in parallel with the development of detectors taylored for LHC, as described in part C, sections 9 to 14. During 1993-94 we expect to produce a silicon pixel detector system with 50 x 50 mm arrays for use in the Omega heavy ion fixed target experiment WA97 (sect.9). The next application of silicon micropattern detectors could be an extended array for use in the very forward region in DELPHI with sparse data scan readout electronics adapted to the LEP collider mode operation (sect.10). Considerations for the LHC prototypes are given in sec. 11 for p-p and in sect. 12 for LHC-HI. The use of micropattern detectors in two approaches to scintillating fiber detector readout is the subject of sects 13 and 14. In sect.15 reference is made to non-particle physics applications and finally we mention here the interest from the GaAs collaboration RD8 for using the readout chip in connection with a GaAs semiconductor matrix.

B. TECHNOLOGY AND CIRCUIT DEVELOPMENT

1. Further development of the binary pixel cell

Like in most electronics readout chains for LHC we are confronted with trade-offs between noise, precision, speed and power. We have seen from our first experience that noise is not a problem with such a highly granular detector because the noise is low due to the small capacitance of the sensor element. It is rather straightforward to achieve noise levels of less than 100 e^-. This easily allows a signal level of 10 000 e^- as provided by a 150 μm thick Si detector layer.

The pixel to pixel variation of the threshold has a non-uniformity of 750 e^- r.m.s. and appears to be of a random nature suggesting that it is due to the poor reproduction of bias currents from one pixel to the next due to geometrical uncertainties in processing. This variation is calculated to be equivalent to 15 mV r.m.s. at the input to the discriminator. Monte-Carlo simulations of the comparator circuit by Karttaavi (CERN and SEFT), using statistical data on the processing parameters as provided by the manufacturer, have helped to identify the most critical components in the design. The transistors thus identified can be made less critical by increasing their size, or alternatively, the non-uniformity can be reduced by the use of a 1 μm technology instead of a 3 μm technology, while keeping the dimensions the same. The need for a change of technology arises anyway because in 1993 Faselec will phase out the 3 μm SACMOS manufacturing at the Zurich facility. At present the pitch of the cells is 75 μm in the small dimension. We expect to reduce this to 50 μm using a more dense technology, e.g. the 1 μm SACMOS, which at the same time will improve the detection precision to 15 μm.

We now come to the problem of trade-off between speed and noise. We need to be able to give an exact time tag to hit pixels in order not to spoil one of the virtues of the silicon pixel detector, its fast signal. However, because of the very low occupancy of one pixel it is not necessary for the amplifier-discriminator chain to complete signal processing *within* the bunch crossing interval but merely with a *time walk* of less than this. Thus we can save power by optimising the *time walk* to the bunch crossing interval. It is interesting to note here that the time walk of a channel of the Omega2 chip from x2 to x10 threshold is already below 20 ns.

Design work on the binary cells for Omega and LHC at CERN is undertaken by Campbell and Jarron, in collaboration with Krummenacher, Enz and de Raad of Smart Silicon Systems (SSS), and alternative cells for Delphi and LHC are studied at CPPM by Cohen Solal and Mekkaoui.

Evaluation and simulation work has been done in addition by Beker, Chesi, Heuser, Karttaavi, Middelkamp, Neyer and Pengg. This part of the work is very essential for further progress towards a good design and is likely to take much effort also in the future.

2. SOI technology for monolithic device implementation

Monolithic detector development at IMEC (Dierickx, Hermans, Debusschere, Claeys) has been undertaken with CPPM (Habrard, Mekkaoui, Sauvage), Pisa (Bosisio, Focardi, Forti) and CERN. The presentations on SOI by Bosisio and Dierickx in the 1992 NSS in Orlando are combined in the article in the appendix. We propose to continue this development in the coming years towards a real demonstrator pixel matrix because the performance of the test devices made so far is better than our expectations, because a monolithic device is the only solution in vacuum applications and because the feasibility of SOI monolithic devices is of interest anyway in case the SOI technology will be chosen for reasons of radiation hardness.

For summer 1993 it is planned to design a new mask set which will include an operational pixel matrix of at least 100 cells. The processing of this new design can be terminated in March 1994 and the results will become available by the end of that year. Pengg and Dierickx will work on this primarily.

3. Development of analog pixel cells (Anapix)

The analog design has originated from Krummenacher (SSS), with an additional effort provided by Campbell at CERN and Inzani and Bonvicini in Milano. This cell contains a low noise amplifier, followed by a peak detector, memory and driver. An 8-channel chip has been connected to a segmented detector by wire bonding and the analog characteristics are being evaluated. The noise of the circuit is 100 e^- r.m.s. at zero sensor capacitance and is linear up to a signal of 50 000 e^-. Evaluation of this circuit involves also Redaelli, Pindo and Perego in Milano.

The principal objective of the analog matrix to be constructed in the next phase is the study of charge division in various detector configurations. In a low multiplicity environment one might consider analog readout for high precision particle localization using capacitive or resistive charge division schemes which would profit from the high signal/noise ratio caused by the small capacitance. Furthermore, once a comparator has been added to the present analog cell, the availibility of the analog signal together with the corresponding discriminator response should allow a more precise study of the factors influencing the comparator threshold distribution.

At the same time, the availability of both an analog and a binary matrix will allow us to make a practical comparison between the relative merits of either solution under different circumstances.

The proponents of the LHC heavy ion experiment (sect. 12) prefer to use an analog pixel array as the innermost layer in order to identify heavily ionizing particles with relatively low momentum.

4. Interconnection techniques and MultiChipModule substrates

The bump bonding development has been undertaken in the first instance with GEC-Marconi (Caswell). Several other suppliers have been contacted by CERN and CPPM (Delpierre and Sauvage), and an alternative is being pursued for the case of large bumps, of more than 100 μm diameter, which can be used for the Delphi matrix. The cost of the solder bump-bonding process has been relatively high, initially about 500 FS per device. Discussions with the manufacturer in view of making the procedures more economic have resulted recently in a reduction of the cost to 200 FS per device. Reduction in cost is made possible by the use of semi-automatic chip-placement machines. The effectiveness of several such machines is being evaluated in collaboration with the manufacturer, where RD19 has made parts available for this purpose.

The development of larger arrays and thinner components (for reduced multiple scattering) also requires a close cooperation with the various partners in industry. The most promising approach seems to be presented by low-mass multi-chip modules(MCM), preferably with silicon base. These modules have to be compatible with the bump-bonding technology. The modules should have a 'universal' ladder shape such that a variety of detector systems could be constructed with identical modules. This will reduce the module cost and increase the possibilities to get them built by industry. Under this point one could consider also the evaluation of the use of epitaxially built silicon detectors, with sensitive thickness between 60 μm and 100 μm.

A Silicon Base Module (SBM) development is under discussion between CERN, CPPM and Canberra on the one hand and GEC-Caswell and GEC-Lincoln or IMEC on the other hand. We have to go through careful compatibility testing and this development may take a considerable effort. Thinning of readout wafers and the use of thin detector wafers are part of this program. These technological aspects are studied by Campbell, Heijne, Menetrey, Neyer and Sauvage.

5. Readout architecture

Intelligence on-chip will be needed to provide efficient readout/ information extraction in large arrays at LHC speed. A first approach towards sparse data readout has been implemented at the Collège de France by Boutonnet, Delpierre, Jæger and Waisbard [9] and this will be used in the matrix now under design for DELPHI. As explained in our original proposal this system makes use of a daisy chain on the lines and on the columns in such a way that the readout signal propagates directly to the lines and columns with hit pixels, and retrieves the addresses without ambiguity and without having to scan large numbers of empty pixels.

In order to further optimise the readout of such a highly granular detector it is important to consider very carefully the occupancies including both signals and background. A number of simulations have been done already at CPPM for the ATLAS LOI.

We expect the inner tracker detector to cover a rapidity of up to 1.5 resulting in 20M pixels per tracker plane, if each pixel has an area of 50 μm x 500 μm (if possible 200 μm). As the number of particles generated in one LHC bunch crossing is expected to be around 2 000, this implies an occupancy of 10^{-4} per pixel per bunch crossing (excluding pile-up and noise). This means that one pixel is highly unlikely to be hit more than once in the 2 μs latency time for the level one trigger (assuming a 15 ns bunch crossing interval). This in turn implies that we need to store at most one time-tag per pixel per level 1 trigger, i.e. pipelining is not required at the level of a single pixel.

This last statement has a direct effect on the readout architecture to be chosen. It makes the pixel readout architecture quite distinct from that of the projective tracking detectors. With such a low occupancy the optimum power consumption will be obtained using a data driven architecture if possible with unidirectional data transfer. The time stamp may be stored locally in one pixel in digital or analog form and passed to the periphery of the chip only after a level 1 trigger has been produced. In this case each pixel must be able to reset itself after one level 1 latency period. An alternative architecture would pass the time stamp information to the periphery in a continous manner ('peristaltic data transfer'). In either approach the digital control circuitry will have to be rather sophisticated. It may be desirable in a first iteration to implement this on a separate chip. We note that in this case a readout system based on flow of information along a single coordinate (e.g. by columns) presents certain practical advantages.

A number of control functions, bias current supplies, data bus, masking to suppress noisy pixels, etc. have to be implemented also on the chip periphery or on a separate control chip. Such a chip could be placed besides the direct readout chip and the connections, using bump bonds, all would be made at the same time via the Silicon Base Module.

The study of the LHC readout architecture has started recently, involving so far Campbell, Darbo, Delpierre, Heijne, Jarron and Neyer.

6. Radiation hardness requirements

In the early stages of development there is little virtue in radiation hard devices because the prototypes will be used only in relatively low dose experiments and will not suffer significant damage. The cost of radiation hard processing is higher than that of normal CMOS and the turn-around time longer. Furthermore, the use of submicron silicon CMOS technology may already offer improved radiation tolerance (maybe ~500 krad for the new SACMOS1, the current SACMOS3 process allows ~30 krad) because of reduced threshold shifts for thinner oxides.

In a later stage we intend to port the pixel design to a true radition-hard technology. We count in this respect on the investigations by RD9 (Aspell, Faccio, Heijne, Jarron) and on the efforts at Saclay and CPPM towards the DMILL (RD29) technology (Blanquart, Dentan,

Mekkaoui). At CPPM some pixel cell designs have been made using DMILL. At this time there is no conclusive evidence about the finally accepted radhard process. The Thomson-TCS 1.2 μm SOI process looks increasingly attractive. It is expected to sustain 10 Mrad and 10^{15} neutrons cm^{-2}. No submicron version of a radhard process is currently available in Europe, but by 1995 Thomson TCS is planning to have a 0.8 μm technology in production. The final optimization of the readout circuits to satisfy the specifications in terms of timing, power and density must obviously be done directly in the radiation hard technology.

7. Mechanical support and cooling

Mechanical design of polyvalent modules for a variety of systems, flat or curved, etc. is related to the development of the Silicon Base Module (SBM). The final mechanical design is likely to be the responsibility of each experiment itself. Close contact in the early stage is desirable, however. For the Omega WA97 we have been working on the mechanics at CERN with the experience of Menetrey, Chesi, Quercigh, et al.

Cooling design is being undertaken currently in the framework of RD20 by CPPM (Fallou and Hallewell) and in the framework of RD2 by CERN/Dortmund (Gildemeister, Gößling). The cooling is made more difficult because care has to be taken in reducing overall material thickness. In the ATLAS SITV group three different techniques are studied (gas cooling, water cooling and heat pipes). CPPM is studying a mechanical structure with cooling by heat pipes (small tubes with evaporative liquid inside) for the micropattern detector planes as well as for the Si microstrip detectors. The first tests show that one can evacuate 0.8 W/cm^2 with less than 2.5°C temperature difference.

More precise power estimates will be needed to establish the ultimate cooling requirements of the micropattern detector arrays in LHC.

8. Testing and reliability including preassembly tests for pixel readout chips and detector

Evaluation of the detector assemblies is the most important activity in our R&D effort because it should provide the input for future improvements. Several people, mentioned already before, have been working on this for a large fraction of their time during 1992.

Another aspect concerns the feasibility of multi-chip arrays. These depend crucially on the availibility of tested, fully functional components and one has to study the yield and reliability at all levels in the assembly in order to obtain in the end satisfactory arrays. Extensive testing of the electronic chips before bumping is necessary because bump bonding is not a reversible process, with the consequence that a malfunctioning chip involves the loss of the whole array of several ladders. We have been studying a set of parameters which allows with a high level of confidence to screen malfunctioning chips efficiently. A first parameter is the measured value of the DC

currents in the bias resistors. When testing the Omega-D chip we found that most of the malfunctioning chips showed at least one DC value that is different from the standard one.

The Bari group (Simone et al.), Beker (Roma), Neyer (ETHZ), Campbell and Chesi (CERN) are implementing now a 2-step procedure to test the components before the array construction. The DC parameters will be tested on wafer using a standard probe station with dedicated probe card. Afterwards, these wafers are bumped, cut and bonded to the matching detectors. The second step is the test of finished, bump-bonded 'ladders' before glueing these on a common ceramic support. A special fixture to be mounted on the wafer probe station will be designed to safely hold a full ladder structure. This the " :lows DC and dynamic testing using the complete read-out electronics. Pulsing of the electronics and the detector has been investigated; a successful attempt using laser-excitation for the electronics was made, a gamma-source for the detector has been used, pulsing of the test row and pulsing at the detector back plane are also feasible. Acceptance limits for the measured parameters have to be defined, in order to decide which chips and which ladders are accepted for mounting of the final array.

In the LHC production effort it will be important to have special equipment that allows a complete DC and dynamic test using the complete read-out electronics also in between the wafer test and the ladder test after cutting of the bumped chips. This additional check on the electronic chips should allow to assemble ladders with an even higher yield.

Chip testing using a laser scan for the purpose of acceptance has been studied at CPPM (Clemens, Sauvage, cs.) , but this has not yet reached a stage of 'large' scale application. This method will certainly be useful as final verification of the assembled array.

C. APPLICATIONS IN EXPERIMENTS

9. First application of the silicon pixel detector in the OMEGA heavy-ion experiment WA97

The ultimate goal of the heavy-ion program is to find evidence for a new state of matter, the Quark Gluon Plasma, which is predicted to be formed during the collision of heavy ions at ultra-relativistic energies. Strange particles and in particular hyperons are important diagnostic tools for this search since their production would be enhanced by the onset of the new state. The WA97 experiment aims to make a comprehensive study of hyperon production in nucleus–nucleus collisions using the new heavy-ion beams expected to become available at CERN in 1994. The experimental challenge consists in recognizing the hyperon decays amidst the large density of tracks, up to several per cm^2, existing in the region where the hyperon detectors need to be placed for such a study. This challenge can only be met by tracking devices capable to determine the space points on a track directly, i.e. with a two-dimensional readout, thus avoiding the large number of spurious points that would be generated from the intersection of wires or strips.

An elegant solution is offered by the silicon micropattern detector. In view of using this technique in WA97, a telescope consisting of three small prototypes (64 × 16 pixels of size 75 × 500 μm^2) has been built and successfully tested during the 1991/92 Ion run. The off-line data analysis involved the groups from Bari, CERN, CPPM, Milano and Padova and the results are shown in the article in the appendix.

In the laboratory we have successfully tested a multi-chip 'ladder' device covering 0.5 × 4 cm^2. By 1994 we plan to have three multi-chip arrays, covering each a surface of 5 × 5 cm^2, which should be integrated into the WA97 hyperon detector. The space points provided by these arrays will improve the pattern recognition capabilities of the detector. We believe this to be an important step towards the main goal of the experiment: a good statistics study of hyperon production up to the rare Omega.

Following the test in 1991/92, the assembly of a 5 × 5 cm^2 detector was studied. It became clear that for this assembly more functions had to be integrated into the readout chip and that more data and control lines are needed to interconnect the chips. A solution has been found where each of two ceramic supports (fig. 1) carries 6 detector ladders with the bus lines running perpendicularly underneath (fig.2). Two successive planes can be staggered such that the full 5 × 5 cm^2 area is covered by the detectors.

We intend to keep the read-out very simple. Each row of pixels on an individual detector produces a 16-bit word and these words can be clocked into a bus at several MHz. A simple zero suppression at the receiving end provides sufficient data reduction for a read-out speed compatible with that of the other WA97 detectors.

WA97 will take care of most of the financing, but is relying on RD19 for the development of the detector and readout chip and of the interconnection techniques, e.g. bump bonding.

10. Silicon pixel detectors in the DELPHI experiment at LEP200

The proposal for the use of a silicon pixel detector in the DELPHI very forward tracker has been detailed in [10].

For the physics at LEP200, the DELPHI collaboration wants a microvertex detector with a full angular acceptance (close to 4π) and three detection layers. The proposal is twofold : extension of the cylinders from 40° to 25° (particle angle with respect to the beam) with the aim of b-tagging , and end cap disks from 25° to 10°, mainly for tracking. The first part of the proposal has been approved by the last LEPC , the second part will be proposed at the next one. The end cap disks include four layers from which two are proposed in strips and two in pixels. The main recommendation is a design at reduced cost with performance matching what is needed for tracking. A pixel size of 350 x 350 μm^2 is sufficiently small and such a (relatively) large size will allow for larger contact pads and a more economical bump bonding than the one initially chosen for very small pixels. Three techniques are under evaluation (N. Redaelli, D.Sauvage) : conductive glue deposited by screen printing on the wafer, epoxy tape with embedded directional contacts and industrial gold bump bonding. The design of the frontend cell and the readout system with Sparse Data Scan (SDS) will follow those already developed for the existing prototypes (sects 1 and 5) with only minimal modifications needed for the larger pixel size (M.Cohen-Solal) and for the actual matrix dimensions (C.Boutonnet, JJ.Jaeger, J.Waisbard). The detector design should include the busses for the SDS from chip to chip in order to achieve a double ladder detector module as shown in fig. 3. A Multi-Chip-Module (MCM) -like object on high resistivity silicon is a completely new technology. Detector and structure elements designed at the CPPM (D.Sauvage) are in production in three different firms : Canberra Semiconductor (Belgium), CSEM (Switzerland) and TESLA (Slovakia). The layout and the mechanical structure is being finalized at the CPPM (A.Fallou, L.Lopez). Cooling is not a problem since the power consumption is only about 0.2 watts per detector module. Each pixel disk includes 48 detector modules, that is about one million of pixels for the two layers on both sides (backward and forward).

The data acquisition of the hit pixels will be done only after a positive answer of the DELPHI trigger level-1. At that time the FASTBUS boards (under study at the Collège de France by C.Aubret, JM.Brunet, P.Courty, L.Guglielmy and G.Tristram) will start the SDS in all detectors modules in parallel and then read the addresses of the hit pixels from intermediate buffers.

The DELPHI group directed by Delpierre expects a full detector module working by the end of 1993, and the full detector mounted and tested for the start of LEP200.

Silicon micropattern detector in the LHC experiments

The prime reason for the silicon micropattern detector development is the possibility to tackle the high rates in the LHC p-p interactions and the high multiplicities in jets, in B-decays and in heavy ion interactions. We have initiated the study of intelligence-on-chip in view of efficient data processing and information extraction in a hierarchical system of pixel arrays at LHC speed. An important aspect is the calibration and verification in-situ of the LHC array. The design of control functions will be an iterative process, following the experience which will be gained in the course of the development of successive generations of chips.

11. Silicon micropattern detectors in the ATLAS experiment

The SITV (silicon detector for tracking and vertexing) in the ATLAS experiment, proposed for proton-proton physics at the LHC, includes three double layers of silicon detectors (ATLAS LOI). The baseline for the design of this detector comprises silicon pixel detectors for the layers <20 cm from the beam and silicon microstrip detectors at larger radius. The choice of pixels for the inner layers is made because of the tracking performance (in particular inside a jet) and better radiation resistance, especially when using 150 μm thick detectors. The radiation dose at full LHC luminosity on the inner layer at R=11cm is ~5 Mrads per year from the pions and protons.

The surface to be covered is ~0.5 m^2 for each of the two layers of the inner cylinder. The present proposal is to use Silicon Base Modules (SBMs) consisting of high resistivity Si, of ~10 cm^2 area on which 16 electronic readout chips of 8 x 8 mm^2 are bump-bonded. This gives a total of ~1200 detector modules. The preferred pixel size is 50 x 200 μm^2; if this is impossible, longer pixels could also be acceptable (300 to 400 μm). The material thickness of the detector/amplifier module can be as little as 300 μm but this does not include the cooling and mechanical frame. The total thickness of the SITV using cooling with heat pipes would be about 4% of a radiation length at azimuthal angle 90°.

The specifications for the frontend electronics are severe. The total jitter (time walk + others) should be less than 5 ns for a power consumption less than 100 μW per pixel. A readout system is needed which transmits only the addresses of the pixels hit at a bunch crossing with positive ATLAS trigger (with 15 ns between beam crossings). The experiment is in continuous data acquisition (no interrupt on trigger). Because of the large number of sensor elements (about 10^8) and the small number of hit pixels the readout system should not send high speed signals to all sensor elements but only to hit pixels. This avoids common mode problems but asks for more intelligence in the pixel cells. As described in sect.5 work on the readout architecture has started and at CPPM two alternative systems are being simulated, in which hit pixels are reset automatically after the trigger latency time (2.1 μs), except if there is a positive trigger. This readout is similar to the earlier mentioned sparse data scan, but includes time stamping.

12. Silicon pixel detector in the LHC-HI dedicated experiment

In the dedicated heavy ion experiment at the LHC, a silicon pixel detector will be ideally suited as the first layer in the vertex tracker. The extremely high particle density in heavy ion reactions (up to 8000 charged particles per unit rapidity at Pb+Pb collisions at the LHC) requires two-dimensional position information without ambiguities and very good two particle separation for pattern recognition. In particular the HBT correlation analysis and the reconstruction of secondary decay vertices (Hyperons) will benefit from the excellent position and double track resolution of pixel devices. A more complete description of the physics goals and details on the mechanical arrangement will be found in the Letter of Intent to the LHCC.

The current experimental layout foresees a silicon vertex detector made up of 7 planes. For the innermost cylindrical plane located at a distance of 7.5 cm from the colliding beams we plan to use a silicon pixel barrel with a total length of 25 cm. The detector will be built in the hybrid technology, using separate silicon for the detector and the front end read-out electronics connected with the bump bonding technique. The pixel size of 75 micron x 270 micron is dictated by the required spatial accuracy, as the plane is used not only for resolving ambiguities but is also fully integrated in the momentum reconstruction. In a detector surface as small as 0.1 m^2 we will have about $6x10^6$ pixels keeping the occupancy low even at high multiplicity.

Like with the other components of the vertex detector (silicon strip and drift detectors) we aim for an analog readout of the pixels in order to measure the dE/dx. This will allow identification of low momentum particles, in the $1/b^2$ region, which will not reach the other particle identifying parts of the detector due to the magnetic field and will also permit the identification of conversions.

In order to reduce the multiple scattering effects, the thickness of the hybrid detector has to be reduced to 50-100 μm for the read-out chip and to 150-200 μm for the detector, which is in line with the current developments.

The choice of a truly two dimensional (and therefore unambiguous) detector for the first layer will help to align the vertex detector itself.

This project is a natural development of the RD19 program in which in several years we have accumulated a lot of experience with this kind of detectors and we do rely on a continued progress in the basic technique in this framework in order to reach our ambitious aims, especially in the field of analog readout. We do also expect significant relevant progress coming from the fixed target heavy ion application of the pixel detector in WA97 described in sect. 9.

13. Photoelectron detection in vacuum tubes with silicon pixel detectors for small diameter fibre readout

Within the framework of the RD7 Collaboration, a delay tube to read out small diameter (60 μm) scintillating fibre is being developed. It is intended to replace the conventional readout of the image intensifier (a phosphor screen and a CCD) with a silicon pixel detector directly bombarded by 30 keV photoelectrons. This new readout system will exhibit better performance with respect to spatial- and time resolution, readout speed and zero suppression.

At present, hybrid pixel detectors have been shown functional for MIP detection. Their incorporation in an image intensifier is intended to be tried out. However, difficulties arise with the resistance of Sn-Pb bumps to the temperature cycles needed to outgas vacuum tubes, and the problem of compatibility between the photocathode and the polyimide passivation layer currently used with these hybrid detectors has to be solved.

A monolithic approach using the SOI-technology on a high resistive detecting substrate seems to meet better the conditions of an image intensifier tube environment (as explained above, proximity of the photocathode or required vacuum for example). Further investigations on this technology should thus be taken in consideration.

Photoelectrons with an energy of 30 keV penetrate silicon to a depth of less than 10 μm. Consequently, the design and quality of the surface of the detecting substrate are rather critical. The use of a thinned substrate would provide the advantages of reduced material, less severe demands on the substrate quality, reduced reverse bias voltage and lower sensitivity to irradiation. Therefore, this possibility should also be investigated.

In view of all these considerations, the RD7 Collaboration, would be extremely grateful to participate in, and profit from the R&D work of the RD19 Collaboration. T. Gys has joined RD19 to this end.

14. Direct detection of visible photons from an image intensifier for large diameter fibre readout

A novel type of visible photon pixel detector, which may combine the usually conflicting features of (moderately) fine spatial resolution and high readout speed with on-chip processing, is being investigated (G. Stefanini and C. Da Via). For this purpose, a few detector wafers have been modified, at minimal cost, by suppressing the aluminium metallization on the back and replacing it by a special, low energy ion-implantation in order to obtain a thin window. The detectors were then bump-bonded in the 'usual' way to the readout chips. Tests have just started on one array, initially using a 1.06 μm LED source focused onto a 250 μm plastic fiber the tip of which is brought in close proximity of the detector surface (pixel size 75 μm x 500 μm). Clear signal response from individual pixels has been observed. The detector performance will now be analyzed also at shorter wavelengths. Although the structure is not yet optimized for photon

detection, first results are convincing and leave room for improvement.

This photo-pixel detector can be used for high-speed 2-dimensional photon imaging (e.g. thick scintillating fibre detectors), possibly in conjunction with an image intensifier for light amplification. It may replace CCDs or multi-anode PMTs in several applications. The readout is at present binary, but it may evolve following the main RD-19 programme.

15. Applications outside particle physics involving direct detection of low-energy X-rays

From several sides we have been approached with questions about the availibility of our devices for applications in synchrotron radiation experiments, in biology, medicine, etc. The 2-dimensional detection of soft (20 - 60 keV) X-rays is of great relevance for medical and biological diagnostics.

The feasibility of pixel detectors is being investigated by a Pisa group (A. Stefanini, Bertolucci, Bottigli) together with CERN (Heijne, Jarron, Campbell, G. Stefanini). The Pisa group is currently involved in testing Si double-sided microstrip detectors for digital radiography. This application would eventually require <200 μm space resolution on a surface of ≈25cm^2. Silicon is not the best material, since detection efficiency for X-rays above 10 keV is very low. However, the development of the readout chip can largely profit from the RD-19 programme. The Si detector may later be replaced by GaAs pixels in a hybrid structure, without major difficulties; preliminary work is already in progress.

Another request has come forward from the European Molecular Biology Laboratory (Heidelberg) in collaboration with Geneton-Genomic (F) for evaluation of the possibilities of the micropattern detector for microradiography in view of clone screening in the genome analysis.

The requesting groups have been asked to take up themselves the evalution work, while devices and readout cards as far as available could be provided at nominal cost.

D. CONCLUSION

After the first experience we can estimate to a better degree the possible progress in the development of the silicon micropattern detectors in the next few years. The tasks will be executed in a coordinated way between various European institutes and industries and this will allow results to be achieved faster, while also the financing can be shared. While the number of active people currently is around 50, it may be that more will be needed in order to fulfill all activities in a reasonable time-scale. In particular a long time has to be spent on device evaluation. Several institutes have an observer status and may eventually join actively.

One should be aware that each iteration in the detector development and evaluation takes between 1 and 2 years. A group of experienced specialists may develop a fully operational device in 2 to 4 iterations and this leads to a typical development time of ~5 years. This timescale is similar to that for typical VLSI IC development, in particular for microprocessor or memory devices. In industry much larger groups are engaged for such projects, but we cannot and need not pretend at comparable reliability and manufacturing cost optimization. In comparison with the development time, on the contrary, final production can be much shorter, usually taking less than 2-3 months. Component testing, if well prepared industrially, can be performed also in a relatively short time. Moreover, the cost for the final manufacturing will be significantly lowered if a comprehensive test protocol has been developed well in advance and no surprises are allowed to be discovered in an advanced state of system construction. We think that a heavy accent, both in money and in manpower, must be put on early design and thorough development and **evaluation** whereas in comparison with completely home-built detectors a lesser effort will be needed during the final construction (chip and sensor manufacturing), which is mostly farmed out to industry.

In parallel, other groups in Europe and in the USA also have made significant progress but they are following different approaches. At Stanford a monolithic detector has been manufactured and the first results have been reported [11]. This detector is of the current-integrating type and does not yet contain readout and data reduction electronics. An SSC collaboration has worked with Hughes Aircraft on a hybrid device, and also in that case no processing has been implemented as yet. In the Max Planck Institut in Munich pixel detectors with integrated amplification and charge storage are being developed. At IMEC in Leuven various types of pixel detector have been developed in 1986-89 by Vanstraelen and Dierickx. Finally should be mentioned the group of Damerell at the Rutherford Appleton Laboratory which pioneered CCD type pixel detetectors and which is now showing the advantages of a truly 2-dimensional detector very convincingly in the SLD collider experiment [12].

Acknowledgments

It is a pleasure to acknowledge the effective work of our industrial partners. The initial stage of the development of this silicon pixel detector has been a part of the CERN-LAA detector R&D project which is always gratefully acknowledged.

E. ACCOUNTS AND BUDGET

The total expenditures on micropattern detector development for the 2 years since the beginning of RD19 have amounted to 1.3 MSf of which 450 kSf was provided by CERN. A part of the contributions were made via other sources, namely the Omega experiments and the fiber tracker groups. The planned budget for 1993 amounts to 750 kSf of which 250 kSf is requested from CERN.

Figure Captions

Fig. 1 Layout of the connecting lines on the ceramic plate which will carry the array of 6 detector ladders with altogether 36 readout chips (sect. 9).

Fig. 2 Artist's view of a part of the completed array (sect. 9).

Fig. 3 Drawing of the basic module of the DELPHI array (sect. 10).

E. REFERENCES

[1] F. Anghinolfi, P. Aspell, K. Bass, W. Beusch, L. Bosisio, C. Boutonnet, P. Burger, M. Campbell, E. Chesi, C. Claeys, J.C. Clemens, M. Cohen Solal, I. Debusschere, P. Delpierre, D. Di Bari, B. Dierickx, C.C. Enz, E. Focardi, F. Forti, Y. Gally, M. Glaser, T. Gys, M.C. Habrard, E.H.M. Heijne, L. Hermans, R. Hurst, P. Inzani, J.J. Jæger, P. Jarron, F. Krummenacher, F. Lemeilleur, V. Lenti, V. Manzari, G. Meddeler, M. Morando, A. Munns, F. Nava, F. Navach, C. Neyer, G. Ottaviani, F. Pellegrini, F. Pengg, R. Perego, M. Pindo, R. Potheau, E. Quercigh, N. Redaelli, L. Rossi, D. Sauvage, G. Segato, S. Simone, G. Stefanini, G. Tonelli, G. Vanstraelen, G. Vegni, H. Verweij, G.M. Viertel and J. Waisbard

A 1006 element hybrid silicon pixel detector with strobed binary output
IEEE Trans. Nucl. Sci. NS-39 (1992) 650 also:CERN/ECP 91-26

[2] M.G. Catanesi, H. Beker, W. Beusch, M. Campbell, E. Chesi, J.C. Clemens, P. Delpierre, D. DiBari, E.H.M. Heijne, P. Jarron, V. Lenti, V. Manzari, M. Morando, F. Navach, C. Neyer, F. Pengg, R. Perego, M. Pindo, E. Quercigh, N. Redaelli, D. Sauvage, G. Segato and S. Simone

Results from a hybrid silicon pixel telescope tested in a heavy ion experiment at the CERN Omega spectrometer
to be published in Nucl. Physics B (Como 1992)

[3] M. Campbell, F. Anghinolfi, P. Aspell, W. Beusch, E. Chesi, T. Gys, E.H.M. Heijne, P. Jarron, G. Meddeler, F. Pengg, E. Quercigh, G. Stefanini, H. Verweij, C. Boutonnet, P. Delpierre, J.J. Jæger, J. Waisbard, J.C. Clemens, M. Cohen Solal, Y. Gally, M.C. Habrard, R. Potheau, D. Sauvage, C. Neyer, G.M. Viertel, D. Di Bari, M.G. Catanesi, V. Lenti, V. Manzari, F. Navach, S. Simone, M. Morando, F. Pellegrini, P. Inzani, R. Perego, M. Pindo, N. Redaelli, P. Burger, K. Bass, A. Munns, C.C. Enz and F. Krummenacher

Design and performance of the 'Omega-ion' hybrid silicon pixel detector
internal report CERN/ECP 92-6 (6th Munich/Milano Symp. 1992)

[4] H. Beker, W. Beusch, M. Campbell, M.G. Catanesi, E. Chesi, J.C. Clemens, P. Delpierre, D. Di Bari, E.H.M. Heijne, P. Jarron, V. Lenti, V. Manzari, M. Morando, F. Navach, C. Neyer, F. Pengg, R. Perego, M. Pindo, E. Quercigh, N. Redaelli, D. Sauvage, G. Segato and S. Simone

A hybrid silicon pixel telescope tested in a heavy-ion experiment
submitted to Nucl. Instr. Meth. CERN/ECP 92-18

[5] L. Bosisio, E. Focardi, F. Forti, S. Kashigin, B. Dierickx, D. Wouters, G. Willems, G. Windierickx, I. Debusschere, E. Simoen, C. Claeys, H. Maes, L. Hermans, E.H.M. Heijne, P. Jarron, M. Campbell, F. Anghinolfi, P. Aspell, P. Delpierre, D. Sauvage and M.C. Habrard

Detector diodes and test devices fabricated in high resistivity SOI wafers
Conference Record IEEE Nucl. Science Symp. Orlando 1992

[6] B. Dierickx, D. Wouters, G. Willems, G. Windierickx, A. Alaerts, I. Debusschere, E. Simoen, J. Vlummens, C. Claeys, H. Maes, L. Hermans, E.H.M. Heijne, P. Jarron, F. Anghinolfi, P. Aspell, M. Campbell, F.X. Pengg, L. Bosisio,E. Focardi, P. Delpierre, A. Mekkaoui, M.C. Habrard and D. Sauvage

Integration of CMOS-electronics in an SOI layer on high-resistivity silicon substrates
Conference Record IEEE Nucl. Science Symp. Orlando 1992

[7] B. Dierickx, D. Wouters, G. Willems, A. Alaerts, I. Debusschere, E. Simoen, J. Vlummens, H. Akimoto, C. Claeys, H. Maes, L. Hermans, E.H.M. Heijne, P. Jarron, F. Anghinolfi, M. Campbell, F.X. Pengg, P. Aspell, L. Bosisio,E. Focardi, F. Forti, S. Kashigin, A. Mekkaoui, M.C. Habrard, D. Sauvage and P. Delpierre

Integration of CMOS-electronics in an SOI layer on high-resistivity silicon substrates
submitted to IEEE Trans. Nucl. Science

[8] Erik H.M. Heijne

Imaging with 2D and 3D integrated semiconductor detectors using VLSI technology
submitted to Physica Medica (CERN/ECP 92-xx) ICTP Trieste, 1992, Conf. on Physics in Medecine and Biology

[9] J.J. Jaeger, C. Boutonnet, P. Delpierre, J. Waisbard and F. Plisson

A sparse data scan circuit for pixel detector readout.
submitted to IEEE Trans. Nucl. Sci., Coll. de France LPC 92-11 (Nucl. Science Symposium Orlando 1992)

[10] DELPHI Collaboration

Proposal for the upgrade of DELPHI in the forward region
DELPHI 92-142 GEN 135 16 October, 1992

[11] Walter Snoeys, James Plummer, Geert Rosseel, Chye Huat Aw, Chris Kenney and Sherwood Parker

First beam test results from a monolithic silicon pixel detector
to be published in Nucl. Instr. Meth. (6th Munich/Milano Symp. 1992)

[12] G.D. Agnew, R. Cotton, C.J.S. Damerell, R.L. English, A.R. Gillman, S.J. Hedges, J. Hoeflich, A.L. Lintern, L. Mathys, A.K. McKemey, A. Nichols, G.D. Punkar, J. Richman, Rong Gang, R. Stephenson M.G. Strauss, Su Dong, G.J.R. Tappern, S.J. Watts and F.J. Wickens

Design and performance of the SLD vertex detector, a 120 Mpixel tracking system
Proc. Int. Conf. High Energy Physics Dallas, 6-12 August 1992

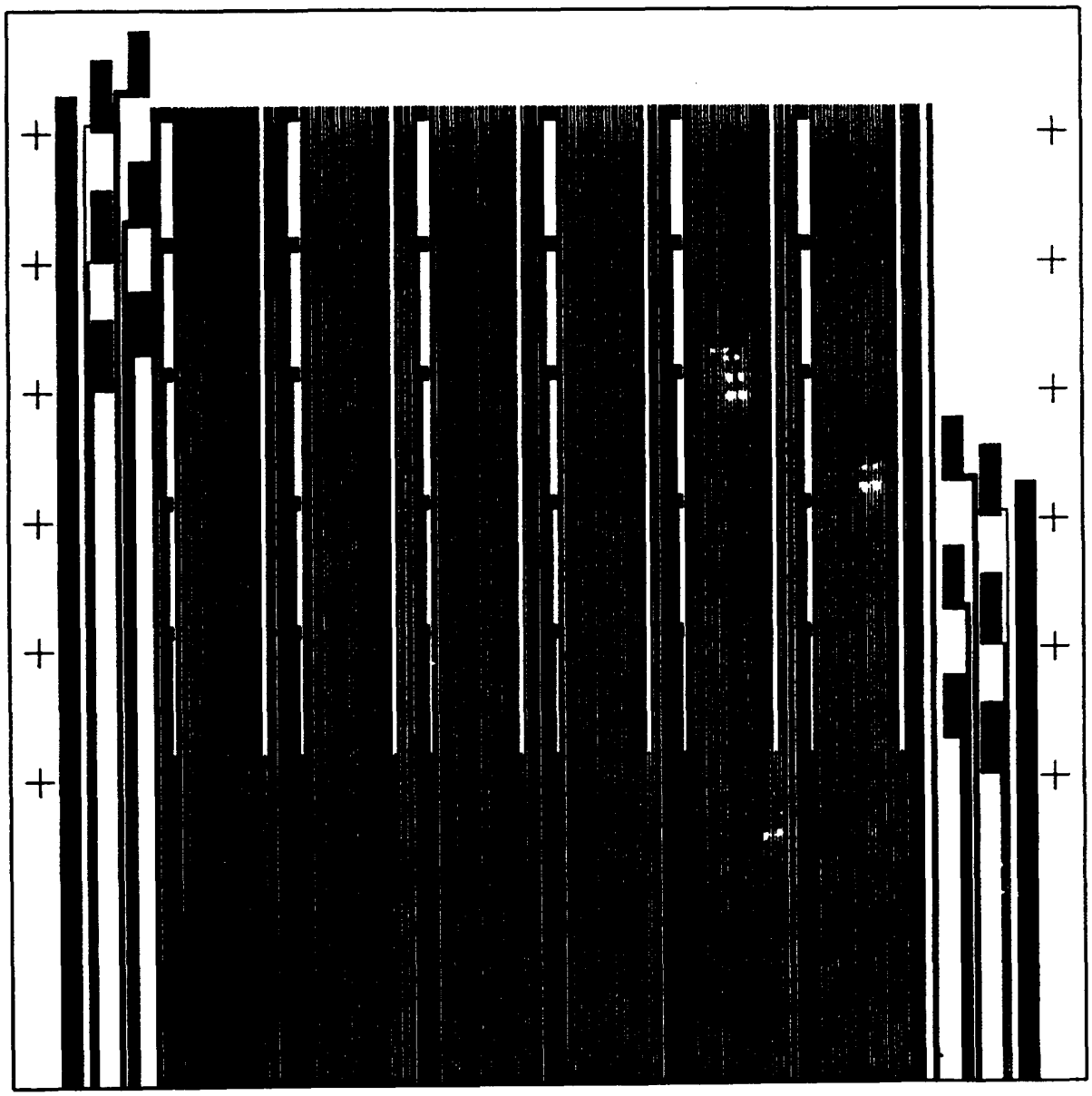

Fig. 1 Layout of the connecting lines on the ceramic plate which will carry the array of 6 detector ladders with altogether 36 readout chips (sect. 9).

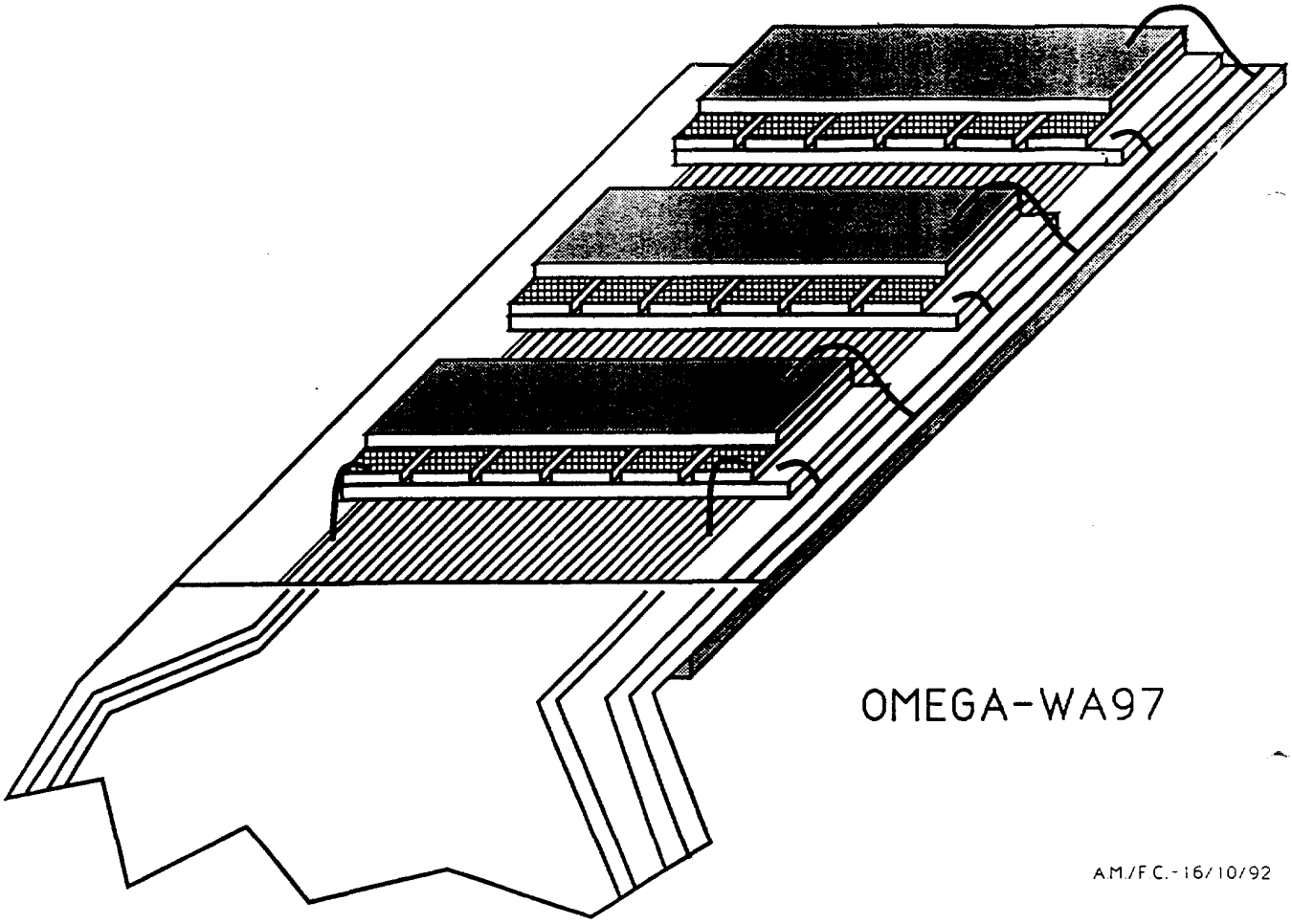

Fig. 2 Artist's view of a part of the completed array (sect. 9).

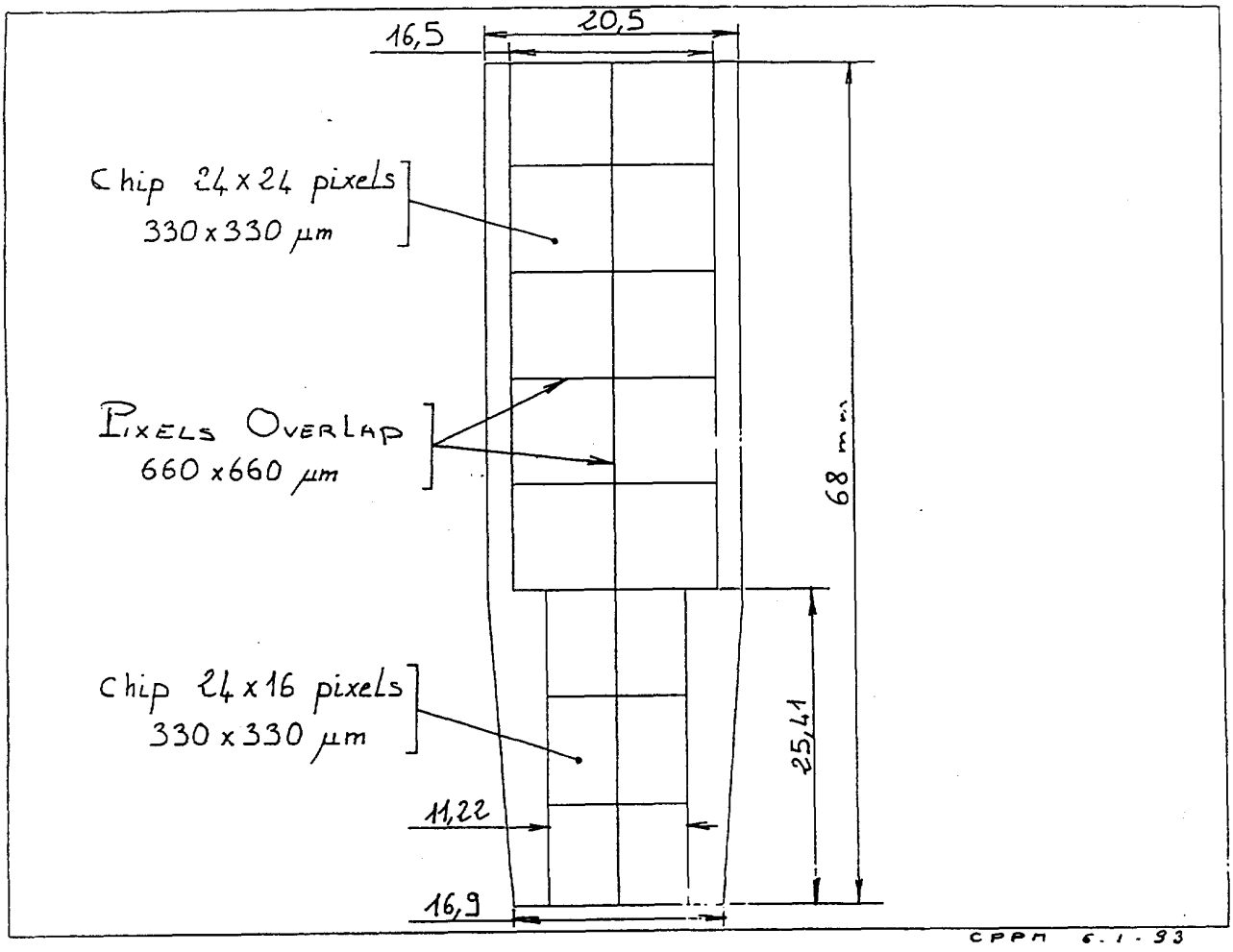

Fig. 3 Drawing of the basic module of the DELPHI array (sect. 10).

APPENDIX

EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

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A HYBRID SILICON PIXEL TELESCOPE TESTED IN A HEAVY-ION EXPERIMENT

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ABSTRACT

Specific features of the Omega-Ion pixel detector are the adjustable delay with external trigger capability and the detector leakage current compensation. A row of pixels can be used for testing the electrical performance of the amplifier and comparator circuits. Detailed results of these electrical tests are presented. A telescope made of three Omega-Ion hybrid silicon pixel detectors has been successfully tested in the heavy-ion experiment WA94. Each plane consisted of a single detector with 1006 active pixels (500 μm × 75 μm), each one being bump-bonded to the readout chip, and arranged in 16 columns and 63 rows respectively. With a sensitive area as small as 8000 × 4725 μm^2 several million events with at least one track originating from the sulphur–sulphur interaction have been recorded in a few hours. Results on target reconstruction, tracking accuracy and efficiency are presented.

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1. INTRODUCTION

In particle physics, particularly in high-multiplicity and high-rate environments like heavy-ion experiments and future hadron colliders, the track detectors in the inner region need a precision of 10 μm [1]. The approach using silicon microstrip detectors may satisfy this precision, but it is not a suitable solution because of the large computation time needed for resolving the ambiguities. A possible solution is to complement the microstrips with two-dimensional silicon pixel detectors: such devices present a finer segmentation and a lower noise [2]. A first effort in the development of silicon pixel detectors with adequate speed was performed in the framework of the CERN/LAA research and development program [3] and now this work continues in the CERN RD-19 program [4].

A telescope made of three new hybrid silicon pixel detectors has been tested in the heavy-ion experiment WA94 at CERN and the first results have been already presented elsewhere [5]. This Omega-Ion device combines a two-dimensionally segmented silicon detector of 1006 sensor elements arranged in 16 columns and 63 rows with a geometrically identical matrix of readout electronic circuits with active, fast pulse processing electronics in each cell.

Besides our own effort, other groups have been studying experimental pixel detectors for similar applications. In particular, should be mentioned the group at the Rutherford Appleton Laboratory which pioneered CCD-type pixel detectors [6] and a separate effort aiming at direct readout pixel detector structures [7]. At Stanford a prototype monolithic detector has been manufactured and the first results have been reported recently [8]. An SSC collaboration has worked with Hughes Aircraft on a hybrid device [9]. In the Max-Planck Institut in Munich pixel detectors with integrated amplification and charge storage are being developed [10]. At IMEC in Leuven new approaches for integration of detector and readout are under development by Vanstraelen and Dierickx [11].

In sects 2 and 3 we present a detailed functional description of the readout chain for an individual pixel element and the general architecture of the readout chip. This chip was tested electrically and the results obtained are discussed in sect. 4. The results from the beam test are described in sects 5 and 6, illustrating the performance of these detectors as well as highlighting some problems. Finally, in sect. 7 we draw some conclusions and discuss further work.

2. PIXEL ELECTRONICS

Each sensor element of the pixel detector is coupled to a complete electronics readout chain which is contained within a silicon area equal to the area of the sensor element, $75 \times 500\ \mu m^2$. A block diagram of this readout chain is shown in fig. 1. It

contains a fast, charge-sensitive preamplifier (CSA), a comparator, a delay and a memory element. A signal from a sensor element is amplified by the CSA, discriminated by the comparator, delayed and gated into memory by the strobe, provided the strobe signal coincides with the delayed comparator signal.

Figure 2 shows the CSA with feedback which incorporates leakage current compensation. Transistors M1 and M3 form a folded cascode pair which provides the transconductance g_m required to transfer the input signal charge to the 7 fF feedback capacitor C_{fb}. The decay time constant of the CSA is around 1 μs. Transistors M2 and M4 control the bias currents of the folded cascode. M6 and M7 are two diodes connected in series which fix the DC operating point of the preamplifier. M9 is a diode which clips the output of the preamplifier for large input signals avoiding any saturation phenomenon which could block the circuit over a long period of time. The detector leakage current is compensated by using M5 to subtract a DC current equal to the leakage current detected on a dummy pixel.

Figure 3 is the schematic of the latched comparator. Transistors M10 and M11 form a differential stage which is AC coupled by the capacitor C_c. This differentiates the output of the preamplifier such that the resulting current in the pair has a peaking time of around 50 ns. The cross-coupled pair M16 and M17 behaves as a bistable feedback element which switches state when the differential current output of M10, M11 exceeds the bias current of M18 which is fixed by I_{dis2}. Thus, I_{dis2} can be used to adjust the threshold of the comparator. The regenerative circuit which is made by transistors M21 to M27 senses the switching of the comparator and latches the comparator output.

The latched output of the comparator is connected to the delay element which, as shown in fig. 4, is a series of three inverters whose switching speed is controlled by currents I_{dn} and I_{dp}. The I_{dn} (and subsequently I_{dp}) can be adjusted externally enabling the delay to be varied. The final inverter is not controlled in switching speed and it is used to clean up the edges of the output signal. The output from the delay resets the comparator via an OR gate. The delay thus defines the pulse width of the signal from the comparator.

Figure 5 shows the architecture of the coincidence logic and memory element. The multiplexor, MuxA, is used to ensure that the trailing edge coming from the delay inverters after twice the delay sets the D flip-flop if it coincides with the strobe. If a falling edge is present then a 1 is clocked into the D flip-flop element. When the strobe is low, MuxB connects all the D flip-flops in one column of pixels together forming a vertical shift register which can be clocked using the *clkout* signal through MuxA. A drawback of this architecture is that the *clkout* must undergo a low-to-high transition during the strobe high phase to avoid false hits.

3. CHIP ARCHITECTURE

Figure 6 shows the architecture of the readout chip. After a strobe has been applied, each pixel which has been hit has a 1 in its D flip-flop. When read out the pixel cells form 16 parallel 64-bit long shift registers which are clocked out using a train of 64 pulses applied to the *clkout* terminal. Each column on the readout chip has 65 elements in total. The top row of pixels is not connected to the detector, but is coupled capacitively to an electrical input enabling the electrical performance of the chip to be evaluated independent of the detector bonding. This test input can be used for a functionality test prior to scribing and mounting of the chips and also during the detector operation for testing if there are no particles. An extra row of pixels at the bottom (not shown in fig. 6) serves as a row of dummy cells for detector leakage current detection and for the generation of bias currents for the column. The leakage current detected in the bottom cell of one column is mirrored to and subtracted from the input of each of the cells in that column.

A picture is taken (fig. 7) with a scanning electron microscope (SEM) of a small part of the readout chip. One recognizes the cells having each a solder bump ready for the input connection to the silicon detector chip.

4. ELECTRICAL MEASUREMENTS

As described above, all pixels in the top row are connected capacitively to an input bonding pad. The approximate value of the capacitor (calculated from the manufacturer's parameters and the drawn size) is around 30 fF. Note that in ref. [5] this capacitance was estimated at the lower value of 20 fF. The higher, but more precise estimation has forced us to scale up our original estimates of noise and threshold variation. The noise after rescaling is ~ 90 e^- r.m.s. Unambiguous determination of the noise figure needs absolute measurements in terms of the electron charge. Such measurements are currently performed using photon-emitting radioactive sources.

Figure 8 shows the thresholds of one row of 16 pixels at two different values of threshold current, I_{dis1}. The pixel-to-pixel variation is around 750 e^- r.m.s. and appears to be of a random nature suggesting that it is due to the poor reproduction of bias currents from one pixel to the next due to geometrical uncertainties in processing. This variation is calculated to be equivalent to 15 mV r.m.s. at the input to the discriminator. As the maximum size of the current mirror transistors is limited by the size of one pixel, we do not expect to be able to improve significantly this random variation in future versions. One possible remedy would be to increase the gain of the preamplifier in order to reduce the size of the r.m.s. variations relative to a given input signal. However, it would be difficult to reduce the size of the 7 fF feedback capacitor any further.

Measurements of the time slewing of the discriminator were made on a separate chip with pixels which had only the preamplifier and discriminator and no delay or coincidence logic. This slewing measured from twice the threshold to ten times the threshold is < 15 ns and is constant for all cells.

A study was made of the strobe timing and variations as this ultimately limits the efficiency of the pixel detector device in a fixed-target application. A first observation proved that the minimum width of the strobe was around 150 ns. This was larger than expected, but it can be explained by the slewing of the strobe signal across the chip due to the large capacitances of the strobe lines. Figure 9 shows the delay between the arrival of the input test signal and the output of the delay element resulting from an input signal of 50 000 e^- for two values of delay control current, I_{dn}. There appear to be two effects superimposed in this case. Firstly, there is a random effect which presumably comes from the geometrical matching problems which we encountered with the threshold non-uniformity. Secondly, there is a left-right effect in the strobe timing. A detailed examination of the chip layout reveals that the power supplies were under-dimensioned leading to a drop in voltage across the chip from left to right. As the external delay control current is applied in parallel to one diode-connected transistor per column, each of these diodes generated a slightly different I_{dn} and I_{dp} for each column. This led to the left-right variation in the delay timing.

The maximum readout frequency was measured to be 5 MHz. This was lower than simulations suggested, but it may be explained by the slowing down of the edges of the *clkout* signal due to the large capacitance of the lines.

5. BEAM TEST

During the run of the heavy-ion WA94 experiment a parasitic test of the pixel telescope has been performed in the 1.8 T magnetic field of the CERN Omega spectrometer. A sulphur beam hits a sulphur target with an intensity of 5×10^5 particles/spill and a spill length of 5.1 s every 19.2 s. The experimental set-up is sketched in fig. 10(a): three pixel detector planes were positioned downstream of the target at 204 mm, 224 mm and 235 mm distance, with their centres 11.5 mm below and 3 mm sideways of the beam axis. In such a way the largest part of the produced particles is not detected and radiation damage did not occur in this test.

Figure 10(b) shows a typical high-multiplicity event. It indicates very clearly the advantage of a true two-dimensional detector over a crossed strip approach.

A first set of runs was made under nominal bias conditions. The results as obtained on-line during the run are shown in fig. 11. Here each pixel is represented as a box

whose length is proportional to the accumulated number of hits in the pixel. As the areas of the boxes are proportional to the square of the accumulated number of hits, the differences are exaggerated by these plots. There are several points of interest. Firstly, all pixels in all planes were able to detect particles (no blank spaces) and there were only four noisy pixels which have been removed from the plot. Secondly, on all three planes there seem to be more pixels hit in the top left corner of the device and less at the opposite corner. The beam was at the top left corner of the chip and this means that the distribution of the hits could be simply due to the beam drop-off. We note here that in planes 1 and 2 the left-hand column seems to receive fewer hits than the rest. Also in plane 3 this effect is seen over the first 4 columns. This is explained later.

The aim of the next set of data taken was to look at the effect of varying the threshold of the discriminators. The bias current I_{dis2} was varied only on the plane 2 leaving planes 1 and 3 under nominal bias conditions. Figure 12 shows that the response of the detector changes only slightly over a wide range of threshold currents. This result is not surprising when one realizes that the discriminator threshold is around 6000 e^- under nominal biasing conditions while the charge deposited by a typical crossing particle is 25 000 e^-.

A further set of data was taken to consider the effect of varying the delay by controlling the bias current I_{dn}. This test was performed only on plane 2. Remembering the results of the electrical tests one would expect a left-right effect across the chip. In the experiment the strobe delay corresponded to the first-level trigger and was around 400 ns. The strobe width was fixed at around 400 ns. Figure 13 indicates very clearly the effect of varying the current I_{dn}. It can be seen that there exists an optimum value of I_{dn} which allows all the pixels of one chip to be sensitive. It is interesting to see that the result of $I_{dn} = 6.375\ \mu A$ is almost identical to plane 1 in fig. 11 and the result of $I_{dn} = 6.875\ \mu A$ is also very similar to plane 3 in fig. 11. This indicates that the values of I_{dn} were not optimized for planes 1 and 3 at the nominal biasing conditions. However, it must be said that this observation is one which only became obvious after off-line analysis.

6. DATA ANALYSIS

For this set of data the values chosen for the currents regulating the threshold (I_{dis2}) and the strobe delay (I_{dn}) are 30 μA and 8.5 μA respectively. The results presented hereafter come from 5×10^5 events which have been collected under stable, optimized conditions in 8 h. Only 4 noisy pixels have been found out of 3018 and they have been removed from the analysis which is presented in this paper. No dead pixels have been detected.

6.1 Geometrical reconstruction

Since the three detectors are not arranged in a projective way a fiducial volume has been defined in order to choose tracks which travel through the whole telescope. We select a subset of our data by requiring that all hit pixels in one event be inside a volume defined as a pyramid pointing to the target and containing the common region of the three detectors (fig. 14).

Moreover, we exclude events with hits in the regions corresponding to columns 1 to 4 in plane 3, because a mistuning of the electronic bias current I_{dn} for this plane may have caused inefficiencies. At this stage of the analysis no constraints are imposed on the hits. About 22% of the events survive this cut. The maps of the three planes representing the number of hits detected in the fiducial volume are shown in fig. 15.

Figure 16 shows the distribution of the number of hit pixels per plane and per event. Because of the very small solid angle covered by the telescope, which is placed off the beam line, the mean value of the distribution is only 1.7 hits. Only for few events the multiplicity is larger than 20 hit pixels per plane (the occupancy is always < 5%). A simple topological and one-dimensional algorithm has been used to study adjacent hit pixels along z (i.e. in the same column, see fig. 17(a)). This simplification was possible because of the different granularity of the detector in the two dimensions (the pixel y-dimension is more than six times larger than the z one). We define as "cluster" a group of hit pixels which are adjacent along z and we call "cluster width" the number of hit pixels. For example, an isolated single-hit pixel is a cluster of width one. Figure 17(b) shows the cluster width distribution of our data: 79% of the clusters have a single hit, 19% have a double hit, 1.9% have a width between 3 and 10, and only 0.1% has a width larger than 10. One should keep in mind that there is a possibility of high multiplicity in the heavy-ion reactions. The mean width of our clusters is ~ 1.3 pixels. The observed percentage of double-hit events corresponds to the charge sharing expected for adjacent pixels when crossed by inclined tracks, and simply taking into account the geometry of the detector (which is 300 μm deep with a pixel pitch of 75 μm).

The fast way to reconstruct the target position is to select candidates to be single-track events for which no complicated reconstruction program is needed. The selection is simply done by choosing events with one cluster per plane. This kind of events represents ~ 1/3 of our sample (around 1.2×10^4 events). Since we do not have any external detector to check the relative position of our telescope planes, we have aligned these planes requiring the self-consistency of the offsets. First, we choose a clean sample of events having only a single hit per plane, then we require that the track candidate comes from the interaction region (target). Therefore, each plane is aligned by minimizing the χ^2 distribution of the trajectory fit of all track candidates. After alignment, a linear fit to the tracks has been performed in the zx plane (minimally affected by the magnetic field) using

the barycentre values of the clusters (fig. 18(a)). The distribution of the intercept between the fitted tracks and the axis z = 0 is given in fig. 18(b): the accumulation in the target region proves that tracks are coming from physical interactions. The tail at negative x corresponds to upstream interactions not filtered by a simple volumetric cut (some matter is indeed present on the beam line in front of the target). This distribution has been fitted assuming a gaussian shape for the target region, superimposed over a flat background. Under these assumptions the target position can be reconstructed with a σ of 1.035 cm.

6.2 Accuracy

It is now possible to evaluate the spatial accuracy of the telescope by using the same sample as for the target reconstruction. First, we define a straight line with the barycentre values of the clusters in planes 1 and 3. Then we compute the difference Δz between the barycentre value of the cluster in plane 2 and the intercept of the line with this detector. The distribution of the residual Δz is presented in fig. 19. This distribution was fitted assuming a gaussian shape. The mean value of –33 μm represents our error on the alignment of the middle plane. The σ of 25 μm is a good estimate of our precision: it compares well with the one expected for an ideal telescope with 3 planes and 75 μm of pitch, which is calculated to be $75/(2 \times \sqrt{3}) = 22$ μm.

The knowledge of the tracking accuracy together with the variance of the linear fit can be used to discriminate in our sample "good" tracks candidates from the "bad" ones. In fact, we define as "good" a track with $\Delta z < 75$ μm (i.e. $< 3\ \sigma$) and a variance $< 10^{-4}$ cm^2 in the linear fit(*).

In such a way we select 11 808 events (around the 94% of our sample). Figures 20(a–c) show the correlations between the z-coordinates of the three planes combined two by two, while fig. 20(d) shows the z-coordinates in the middle plane versus the point where the line constructed using the z-coordinates in planes 1 and 3 intersects the middle detector. The width of the distributions can be explained by the angular spread of the particles emerging from different interaction points in the target.

6.3 Efficiency

We have studied the remaining 6% in order to understand the nature of the so-called "bad" candidates. We have subdivided this sample in two subsamples according to the value of the variance of the linear fit, which suggests a different interpretation of the data. In fig. 21 we show the same coordinate correlation plots for candidates with a very bad

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(*) We call variance the sum of the squared residuals indicating the badness of fit. If the variance is $< 10^{-4}$ cm^2 all the residuals are < 100 μm. In other words we can say that the 3 points are aligned within our tracking precision. If the variance is $> 10^{-4}$ cm then one point is not on a straight line.

variance of the linear fit (> 10^{-2} cm) and a $\Delta z > 3\ \sigma$ (300 events, around 2%). The interpretation of the data is that these are two-track events not fully contained in our fiducial volume. As sketched in fig. 22, the first track intercepts planes 2 and 3 (but not plane 1), the second only plane 1. Those candidates are false single-track events and should be removed from our sample when calculating efficiency.

The second subsample contains candidates with a variance on the linear fit in the range $10^{-4} < \text{var} < 10^{-2}$ and a $\Delta z > 3\ \sigma$ (600 events, around 4%). Those events seem to be low-energy particles (like protons around 1 GeV) which present a big scattering in the middle plane. In this case, in fact, the correlation plots (fig. 23) show a good correlation between planes 1 and 2 and between planes 2 and 3, but a missing correlation between planes 1 and 3 because of the large scattering angle. The fraction of events found is consistent with the analytical evaluation of the probability that a proton of 1 GeV energy has a scattering in the middle plane leading to a deviation of 100 μm or more.

The efficiency is the probability that a track traversing a pixel detector will actually be detected. An estimate of the efficiency for plane 2 was made by applying a similar criterion as for "good" candidates, i.e. one cluster in planes 1 and 3, and no requirement for the middle plane. Moreover, a candidate is accepted if the straight line defined by these two coordinates intercepts the beam axis in the target region as previously defined. This requirement is very important for the sample without hits in the middle plane, in order to strengthen the definition of a real "track". Figure 24(a) shows a distribution of this beam axis intercept (in the target region), to be compared with fig. 24(b), where an enlarged view of the corresponding distribution taken from fig. 18(b) is shown. The two shapes, the centre and the width values are very similar (even if the number of entries is quite different) and this reinforces our confidence in the criterion adopted to define the sample. If we call "N_{empty}" the number of events in the sample with no hits in the middle plane and "N_{full}" the number of events in the sample with one cluster per plane, the efficiency for the middle plane is defined as

$$\text{Efficiency} = \frac{N_{full}}{N_{full} + N_{empty}} = 99.2\% \ .$$

7. CONCLUSIONS

In a complicated device like this first operational hybrid silicon pixel detector, with active signal processing, it is essential to provide means for electrical testing. The electrical test results have been correlated with the results from the beam particle test. Even though the detector worked satisfactorily, a few problems were revealed in this way. In particular, power supply and bias distribution must be implemented carefully. Equally, the ultimate timing accuracy of the circuit is determined by careful line driver design.

This evaluation has enabled us to design the improved version F-Omega-Ion which will be used in the near future. However, the beam test results indicate that even this present version is a very useful detector for the high-multiplicity environment. A larger array, still using this first D-Omega-Ion chip, is now under construction in order to study the practical aspects of assembly, yield and reliability.

For the first time a telescope made of three hybrid silicon pixel detectors was tested successfully in a fixed-target experimental environment. It was possible to develop a very simple and fast pattern recognition, without ambiguities in space, for the study of single and multitrack events. The test has shown the good position accuracy of the pixel detector, which was 25 μm in the direction of the 75 μm pitch. The efficiency was measured to be 99.2%.

Acknowledgements

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REFERENCES

[1] P.E. Karchin, Use of pixel detectors in elementary particle physics, proc. of the 2nd Int. Workshop on Silicon Pixel Detectors, Leuven 1990, Nucl. Instr. and Meth. A305 (1991) 497.

[2] E.H.M. Heijne, P. Jarron, A. Olsen and N. Redaelli, The silicon micropattern detector: a dream?, Nucl. Instr. and Meth. A273 (1988) 615;

P. Jarron, Fast silicon detector systems for high-luminosity hadron collider experiments, proc. of the ECFA Study Week 1989, CERN 89–10, Vol. 1 (1989) 287.

[3] M. Campbell et al., A 10 MHz micropower CMOS front-end for direct readout of pixel detectors, Nucl. Instr. and Meth. A290 (1990) 149;

F. Krummenacher, Pixel detectors with local intelligence: an IC designer point of view, Nucl. Instr. and Meth. A305 (1991) 527.

[4] W. Beusch et al., R&D Proposal for the development of hybrid and monolithic silicon micropattern detectors, CERN/DRDC 90–81, P22 (RD-19) (1990).

[5] F. Anghinolfi et al., A 1006 element hybrid silicon pixel detector with strobed binary output, presented at the IEEE Nucl. Science Symposium 1991, Santa Fe, USA, IEEE Trans. Nucl. Sc. NS–39 (1992) and preprint CERN/ECP 91–26 (1991);

F. Anghinolfi et al., Design and performance of the Omega-Ion hybrid silicon pixel detector, presented at the 6th European Symposium on Semiconductor Detector, Milano, Italy and preprint CERN/ECP 92–6 (1992).

G. Catanesi et al., Results from a hybrid silicon pixel telescope tested in a heavy-ion experiment at the CERN Omega spectrometer, presented at the 3rd International Conference on Advanced Technology and Particles Physics, Como, Italy, to be published in Nuclear Physics (proc. suppl.).

[6] C.J.S. Damerell et al., A CCD-based vertex detector for SLD, Nucl. Instr. and Meth. A288 (1990) 236.

[7] S.L. Thomas and P. Seller, A silicon pixel detector with routing for external VLSI readout, Nucl. Instr. and Meth. A275 (1989) 564.

[8] W. Snoeys et al., First beam test results from a monolithic silicon pixel detector, Nucl. Instr. and Meth., 6th European Symposium on Semiconductor Detectors, Milano, Italy (1992).

[9] S.L. Shapiro et al., Silicon PIN diode array hybrids for charged-particle detection, Nucl. Instr. and Meth. A275 (1989) 580.

[10] P. Klein et al., Design and performance of semiconductor detectors with integrated amplification and charge storage capability, Nucl. Instr. and Meth. A305 (1991) 517.

[11] G. Vanstraelen, I. Debusschere, C. Claeys and G. Declerck, Fully integrated CMOS pixel detector for high-energy particles, Nucl. Instr. and Meth. A275 (1989) 574;

B. Dierickx, Position-encoding smart pixel arrays, Nucl. Instr. and Meth. A305 (1991) 561.

FIGURE CAPTIONS

Fig. 1 Block diagram of the pixel readout circuit D-Omega-Ion.

Fig. 2 (a) Partial schematic of the charge sensitive amplifier (CSA).
(b) Overall schematic of the CSA including biasing and leakage current compensation circuits.

Fig. 3 Schematic diagram of the comparator in the pixel cell. I_{dis1} and I_{dis2} are externally adjustable current sources which control the threshold.

Fig. 4 Schematic of the inverter delay line which is adjustable via the I_{dn} and I_{dp} currents.

Fig. 5 The coincidence logic and the memory, which becomes part of the output shift register upon readout.

Fig. 6 Block diagram of the readout chip architecture.

Fig. 7 Scanning electronic microscope (SEM) photograph of a few cells of the readout chip with solder bumps already prepared.

Fig. 8 The distribution of thresholds of the 16 pixels in the electrical test row at two values of the current I_{dis1}, 44 μA (left) and 30 μA (right). The current I_{dis2} was kept constant at 30 μA.

Fig. 9 The distribution of the binary signal delay for the row of test pixels at two settings of the adjustable current I_{dn}.

Fig. 10 (a) Sketch of the experimental set-up.
(b) Reconstruction of a "good" high-multiplicity hit on three pixel planes in the Omega spectrometer.

Fig. 11 Diagrams representing the number of hits detected during a run in the Omega experiment for each pixel cell in three successive 63 × 16 cell detectors, planes 1, 2 and 3. The beam passed perpendicular to the detectors ~ 10 mm above the top left corner.

Fig. 12 Same as fig. 11, but only the middle plane 2 is shown for two different settings of the threshold: (a) 5700 electrons and (b) 11 600 electrons.

Fig. 13 Same as fig. 11, but only the middle plane 2 is shown for three different settings of the binary delay: (a) I_{dn} = 5.625 μA, (b) I_{dn} = 6.375 μA (nominal) and (c) I_{dn} = 6.875 μA. The left-right asymmetry is becoming apparent.

Fig. 14 Projection on the x-z plane of the truncated pyramid used to select the events in our analysis. The drawings are not to scale.

FIGURE CAPTIONS (cont'd)

Fig. 15 Diagrams representing the number of hits detected for each pixel in the planes 1, 2 and 3 after the cut. The horizontal length of each box is proportional to the number of hits.

Fig. 16 Distribution of the number of hit pixels per plane and per event.

Fig. 17 (a) Schematic picture illustrating our cluster definition: in this example a cluster of width = 1 (single hit) and width = 2 (double hit) are shown.
(b) Cluster width distribution.

Fig. 18 (a) Sketch of the apparatus in the x-z plane; the ratio n (sign inverted) between the constant and the slope of the linear fit (–b/a) represent the intercept along the beam (x) axis.
(b) Distribution of the "–b/a" parameter for 12 745 events with one cluster/plane: the function $F = 995\ e^{-0.5\ ((x\ -\ 1.24)/1.035)^2} + 116.5$ is used to fit the distribution.

Fig. 19 Distribution of the residual Δz for 12 745 events with one cluster/plane: a gaussian shape is used to fit the distribution.

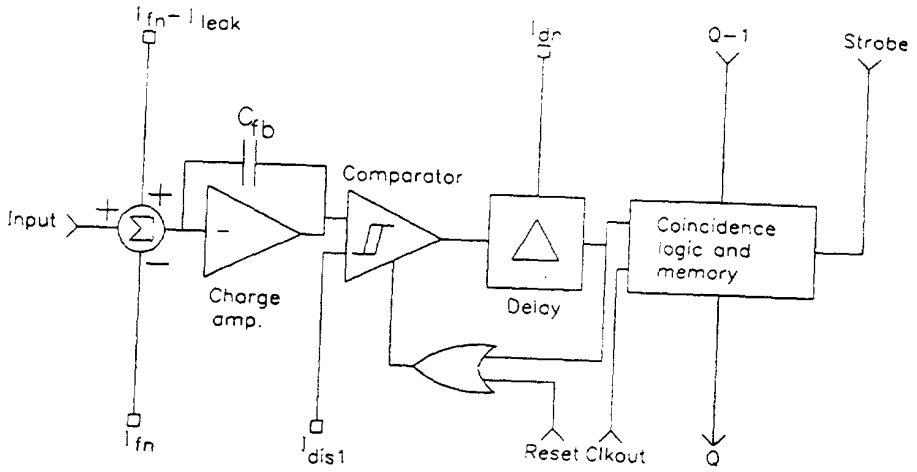
Fig. 20 z-coordinates correlation plots for the so-called "good events": z_i i = 1.3 is the barycentre value (cm) of the cluster on the plane i, z_{2F} is the z intercept on the middle detector with the line made using z_1 and z_3: (a) z_2 versus z_1, (b) z_3 versus z_1, (c) z_3 versus z_2 and (d) z_{2F} versus z_2.

Fig. 21 z-coordinates correlation plots for the events with var > 10^{-2} cm and $\Delta z > 3\ \sigma\ z_i$ i = 1.3 is the barycentre value (cm) of the cluster on the plane i, z_{2F} is the z intercept on the middle detector with the line made using z_1 and z_3: (a) z_2 versus z_1, (b) z_3 versus z_1, (c) z_3 versus z_2 and (d) z_{2F} versus z_2. Only a correlation between z_2 and z_3 in the detectors right-up corner is visible.

Fig. 22 Schematic view in the x-z plane of one event with one cluster/plane generated by two tracks.

Fig. 23 The z-coordinates correlation plots for events with 10^{-4} < var < 10^{-2} cm and $\Delta z > 3\ \sigma\ z_i$ i = 1.3 is the barycentre value (cm) of the cluster on the plane i, z_{2F} is the z intercept on the middle detector with the line made using z_1 and z_3: (a) z_2 versus z_1, (b) z_3 versus z_1, (c) z_3 versus z_2 and (d) z_{2F} versus z_2.

Fig. 24 (a) Distribution of the beam axis intercept for events with one cluster/plane.
(b) Distribution of the beam axis intercept for events with one cluster in the planes 1 and 3 and no hits in the middle plane. In both cases a gaussian shape is used to fit the distribution.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C_{fb}
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Charge amp.
Delay
Coincidence logic and memory
Q-1
Strobe
I_{fn}
I_{dis1}
Reset
Clkout
Q

Fig. 1

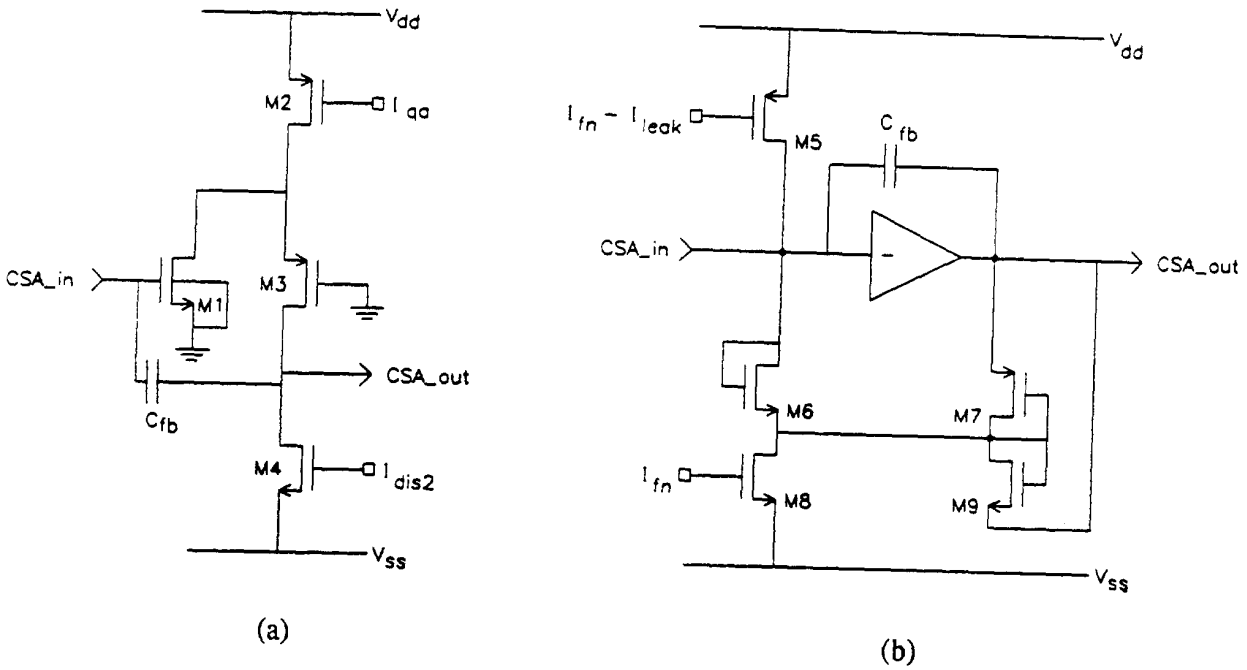

V_{dd}
M2
I_{qa}
CSA_in
M1
M3
CSA_out
C_{fb}
M4
I_{dis2}
V_{ss}
(a)
V_{dd}
$I_{fn} - I_{leak}$
M5
C_{fb}
CSA_in
CSA_out
M6
M7
I_{fn}
M8
M9
V_{ss}
(b)

Fig. 2

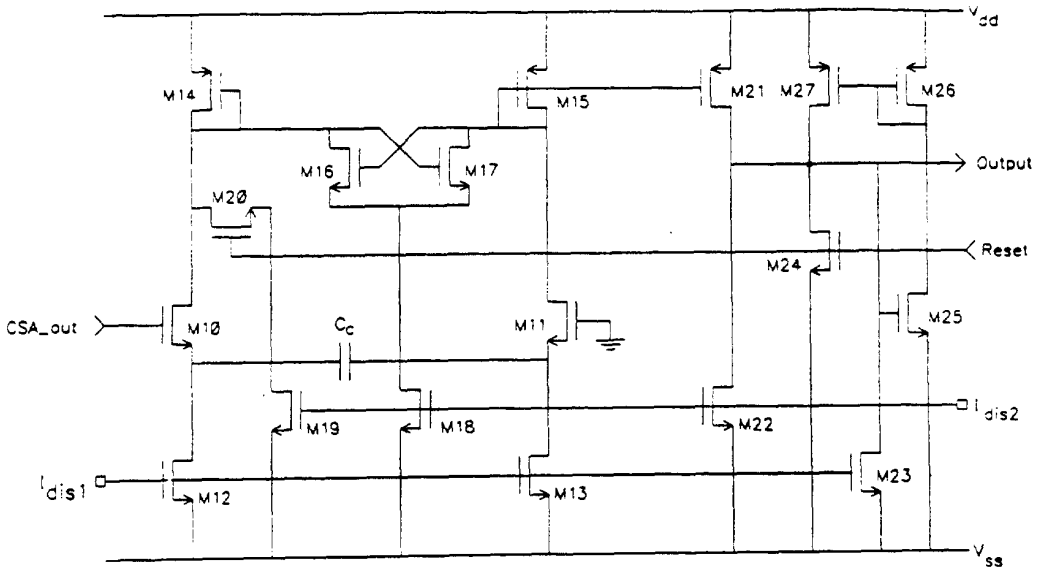


Fig. 3

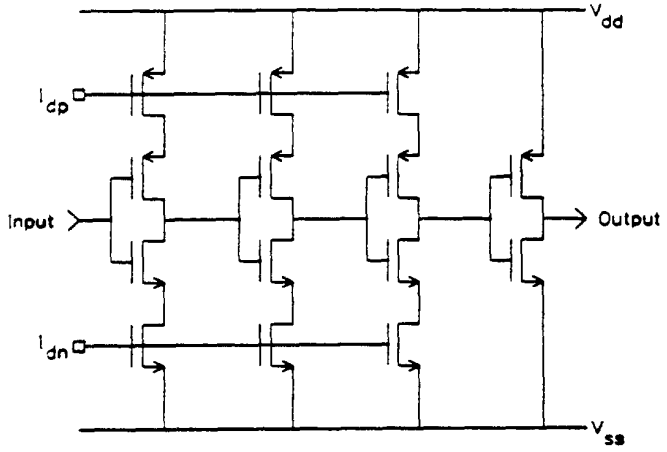


Fig. 4

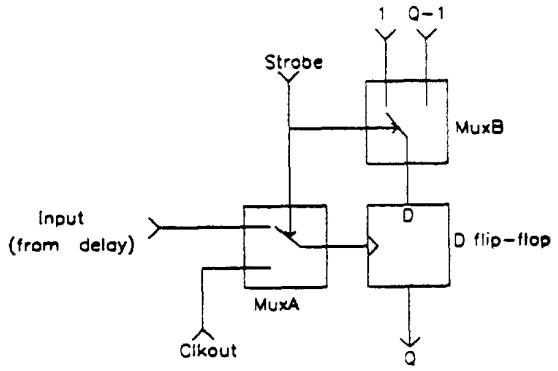
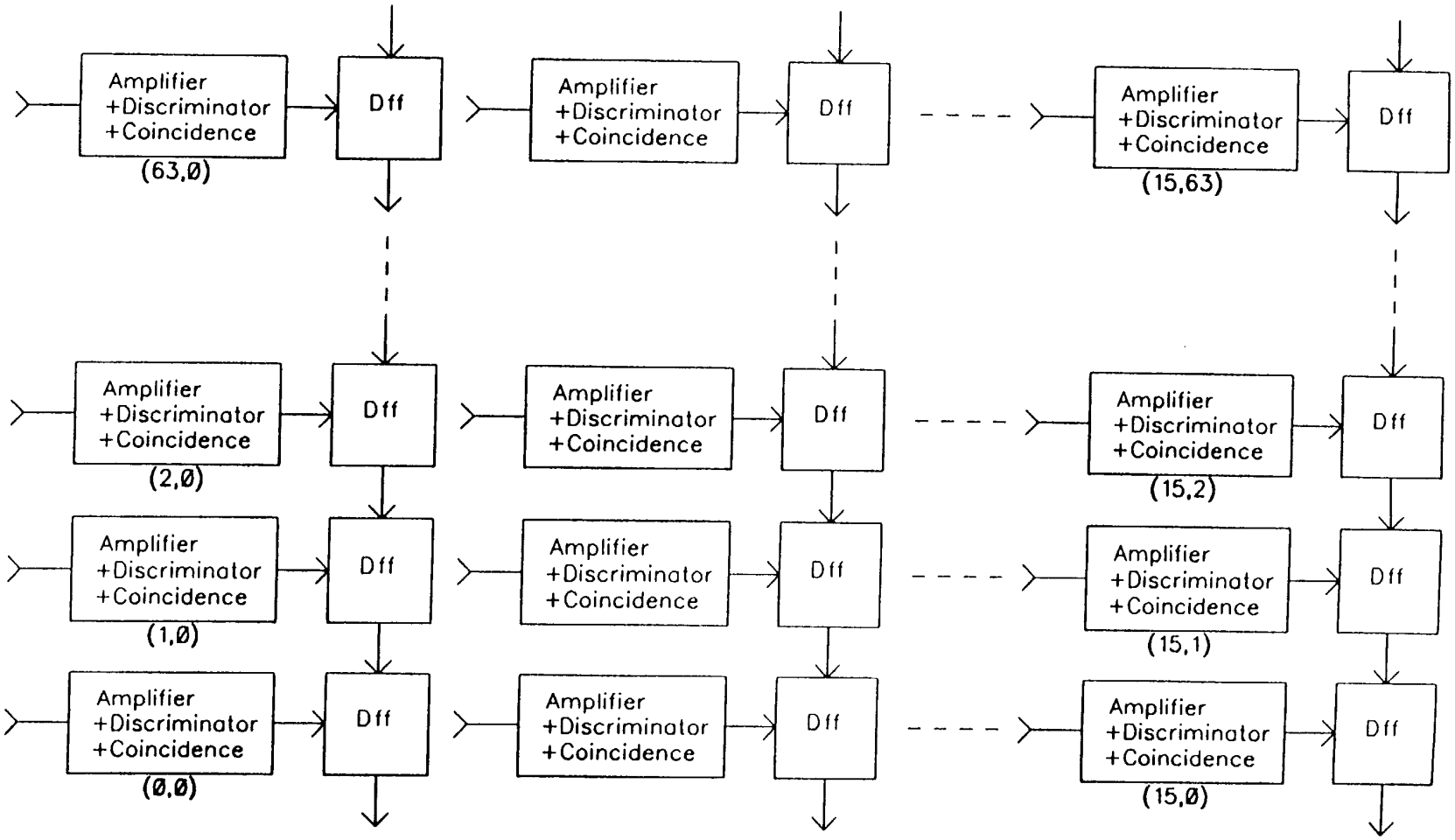


Fig. 5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+Coincidence
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Dff
Amplifier
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+Coincidence
Dff
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Fig. 6

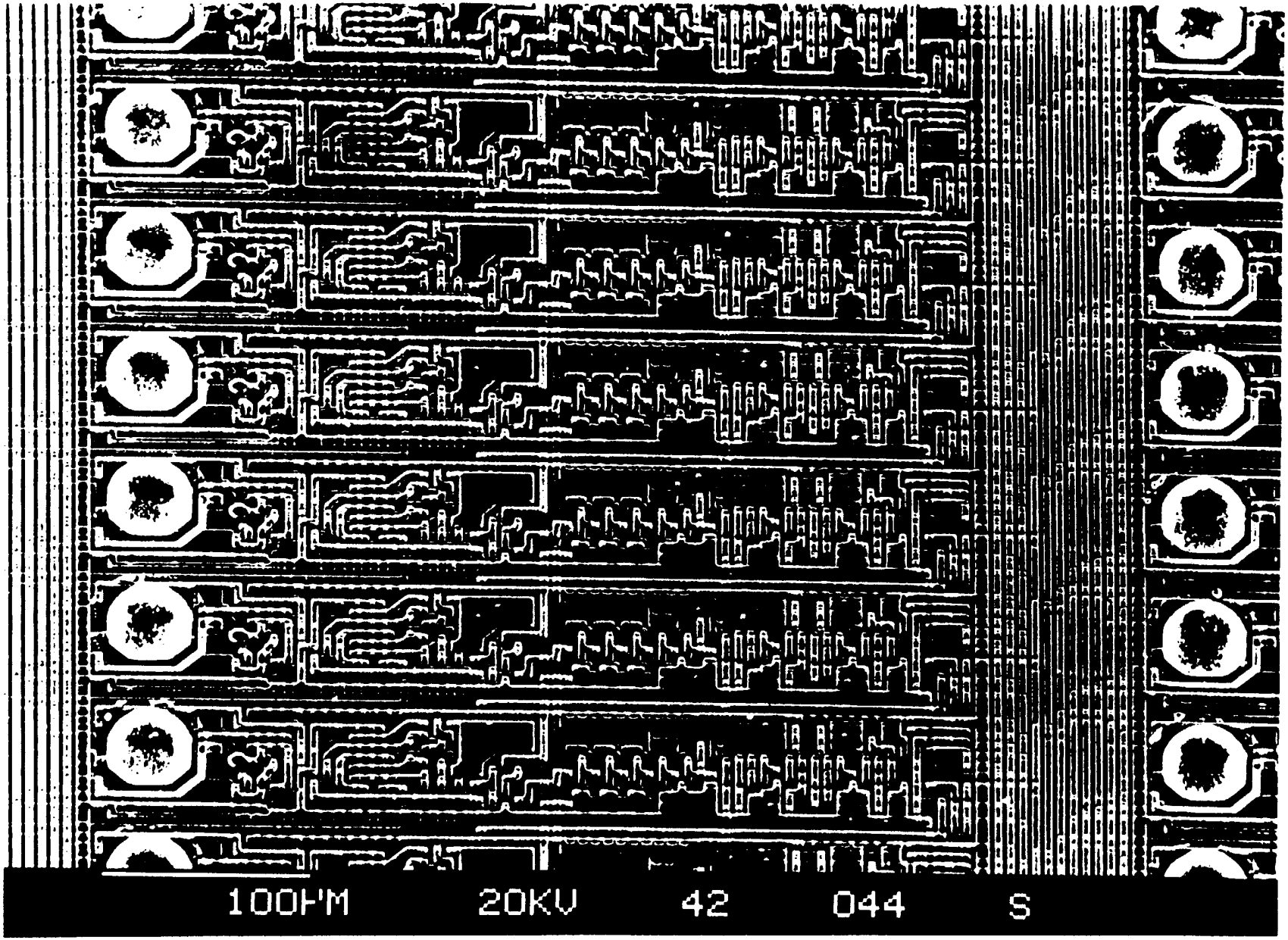
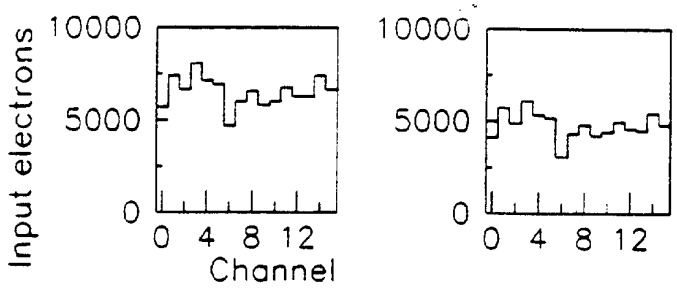


Fig. 7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0
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Channel
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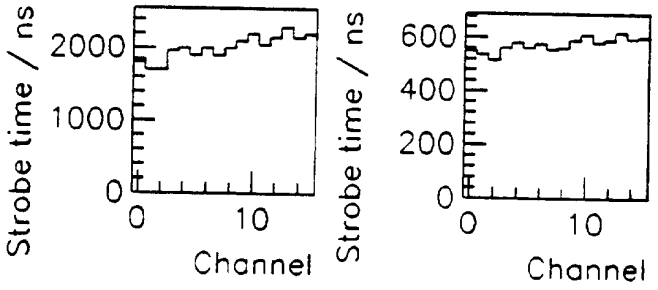
0
0 4 8 12

Fig. 8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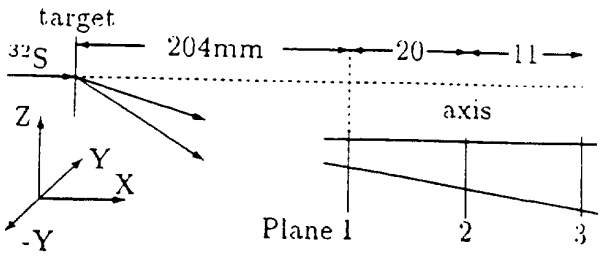
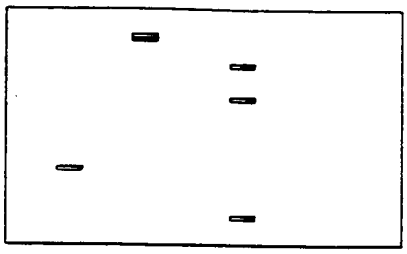
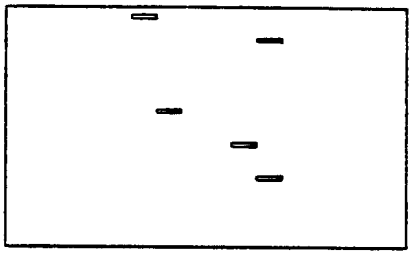
0
0 10
Channel
Strobe time / ns
600
400
200
0
0 10
Channel

Fig. 9

(a)







(b)

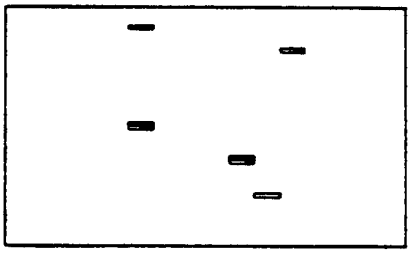
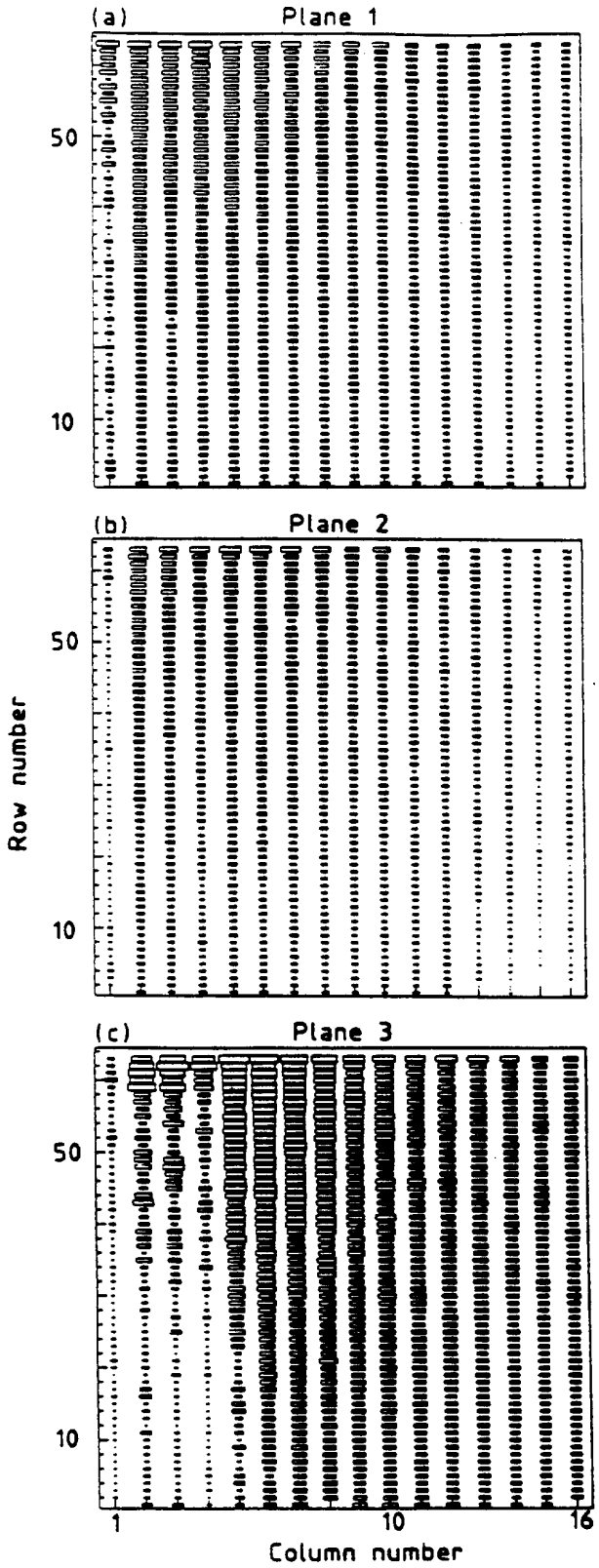


Fig. 10


(a)
Plane 1
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10
(b)
Plane 2
50
10
Row number
(c)
Plane 3
50
10
1
10
16
Column number

Fig. 11

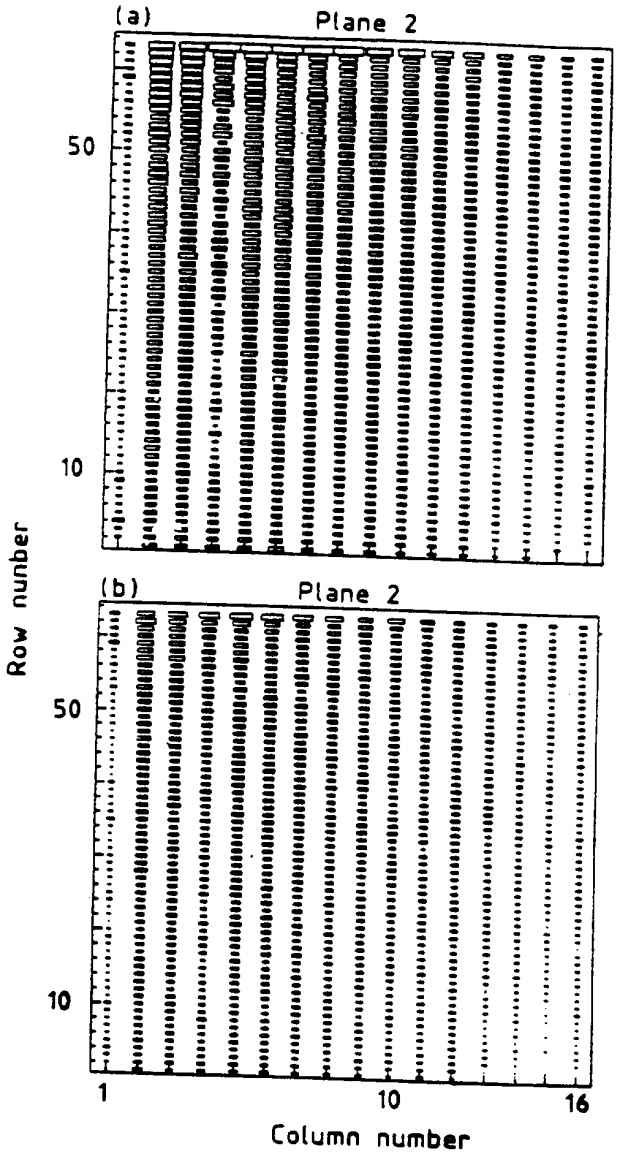
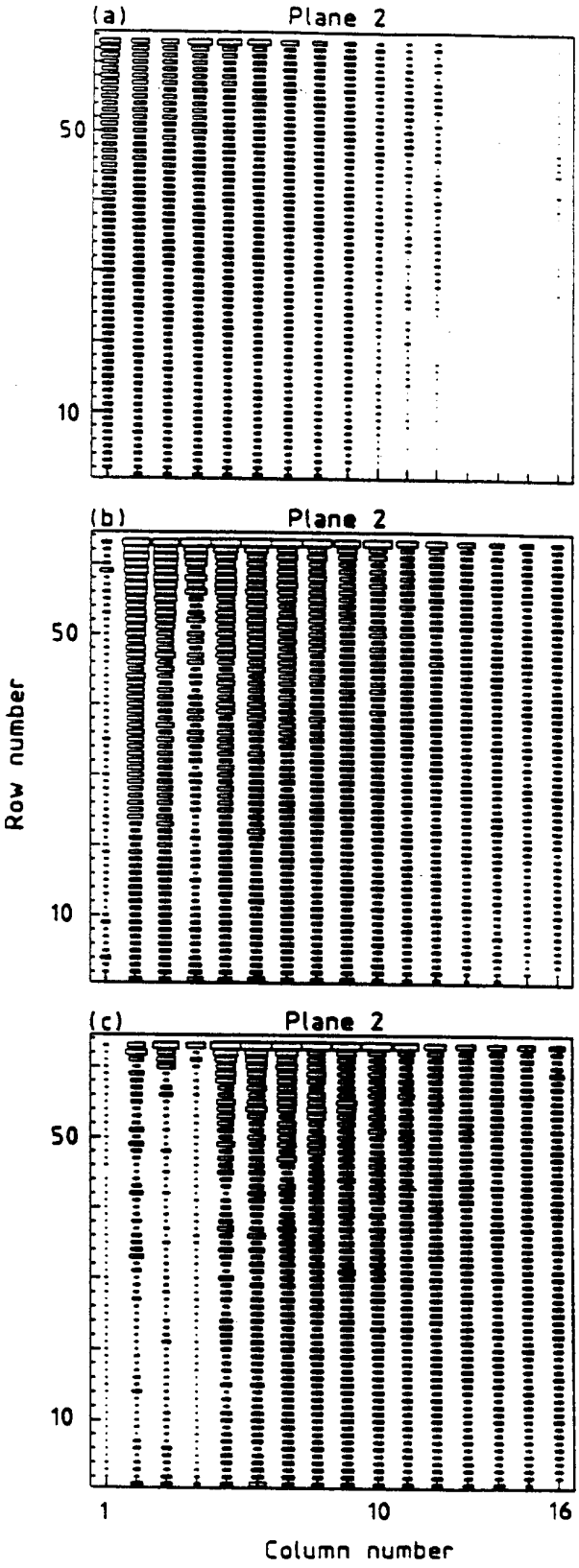


Fig. 12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Plane 2
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Column number

Fig. 13

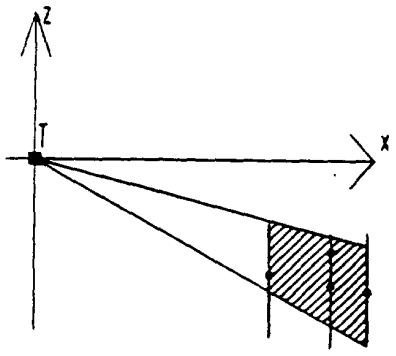


Fig. 14

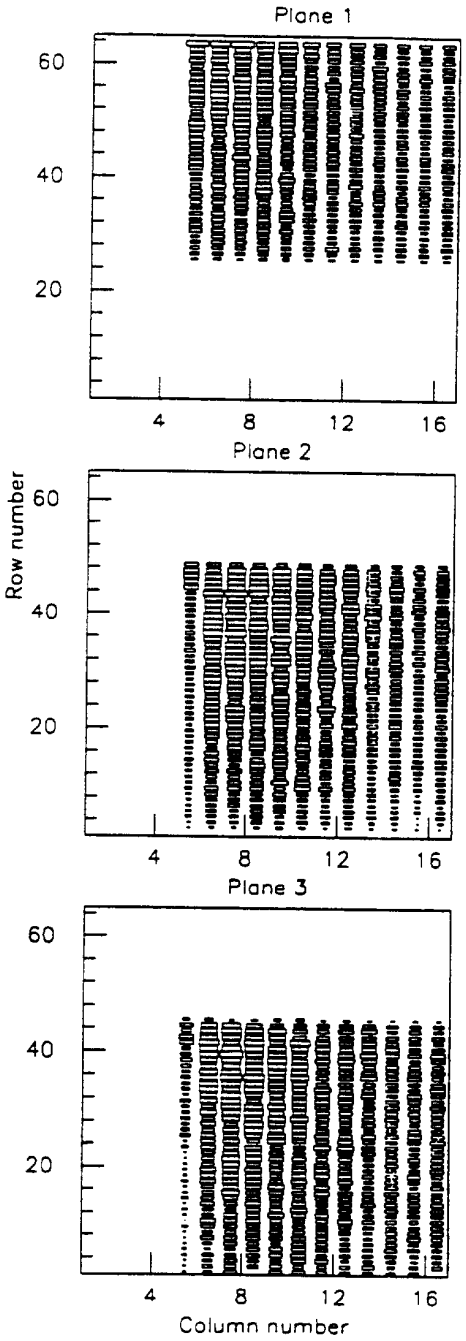

Plane 1
60
40
20
4
8
12
16
Plane 2
Row number
60
40
20
4
8
12
16
Plane 3
60
40
20
4
8
12
16
Column number

Fig. 15

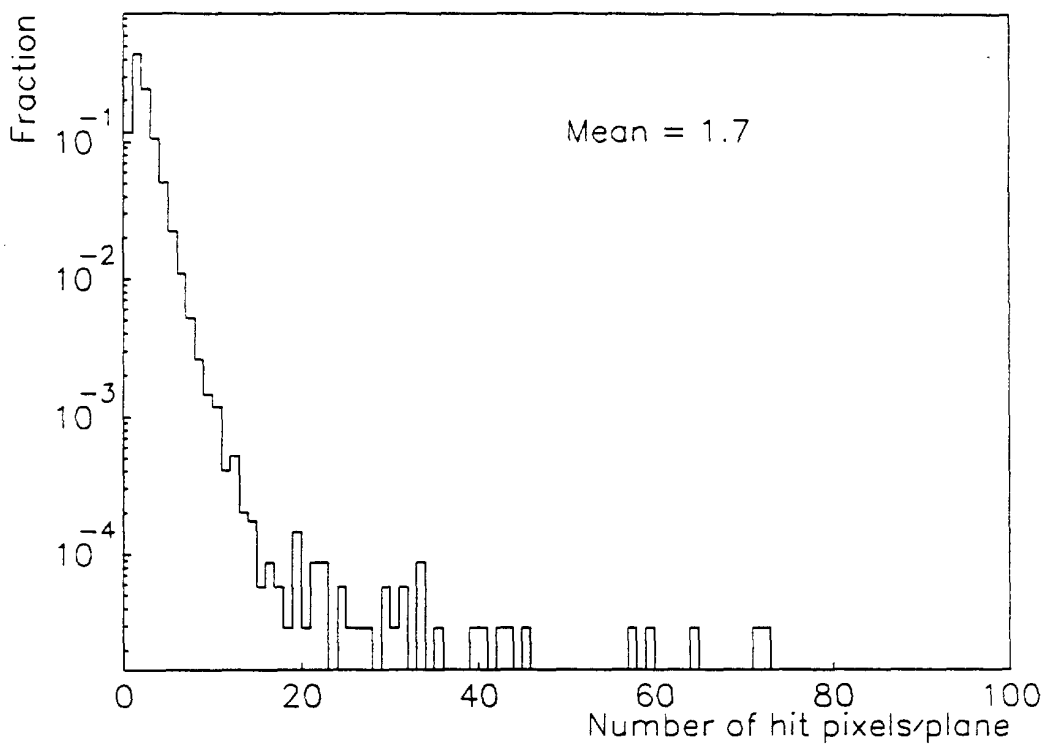
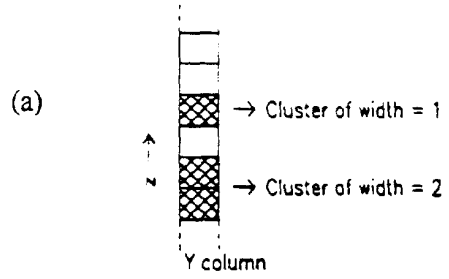

Fraction
10^{-1}
10^{-2}
10^{-3}
10^{-4}
Mean = 1.7
0
20
40
60
80
100
Number of hit pixels/plane

Fig. 16


(a)
→ Cluster of width = 1
→ Cluster of width = 2
Y column

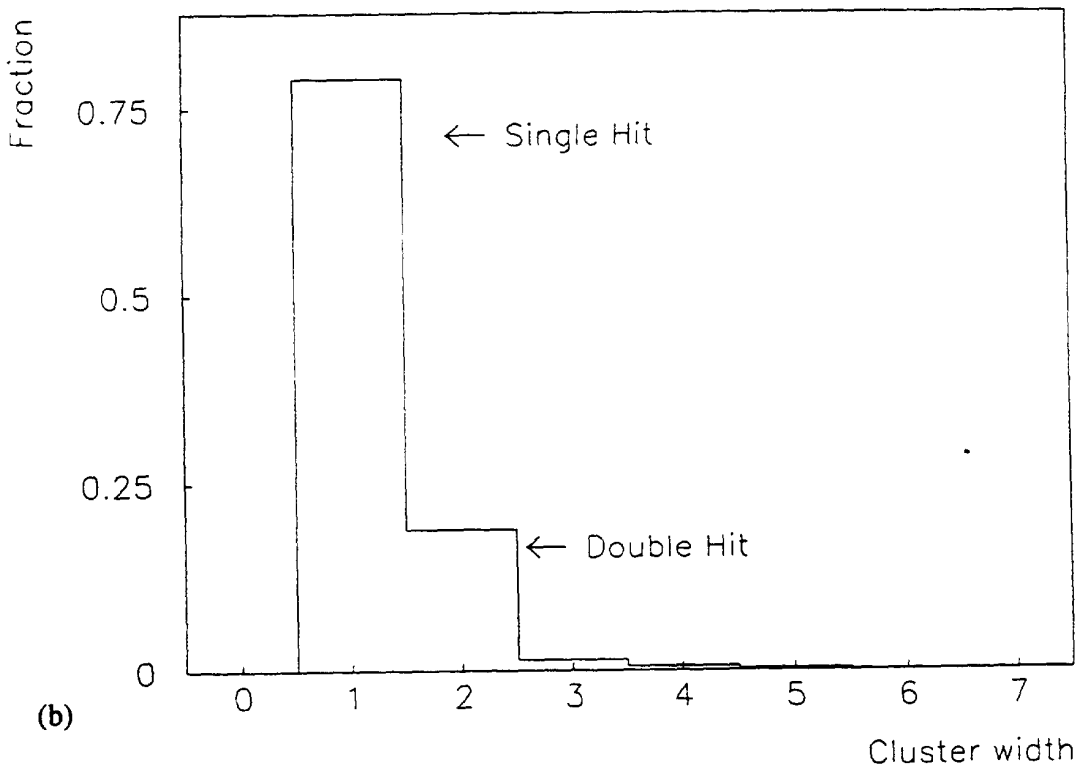

Fraction
0.75
0.5
0.25
0
← Single Hit
← Double Hit
0
1
2
3
4
5
6
7
Cluster width
(b)

Fig. 17

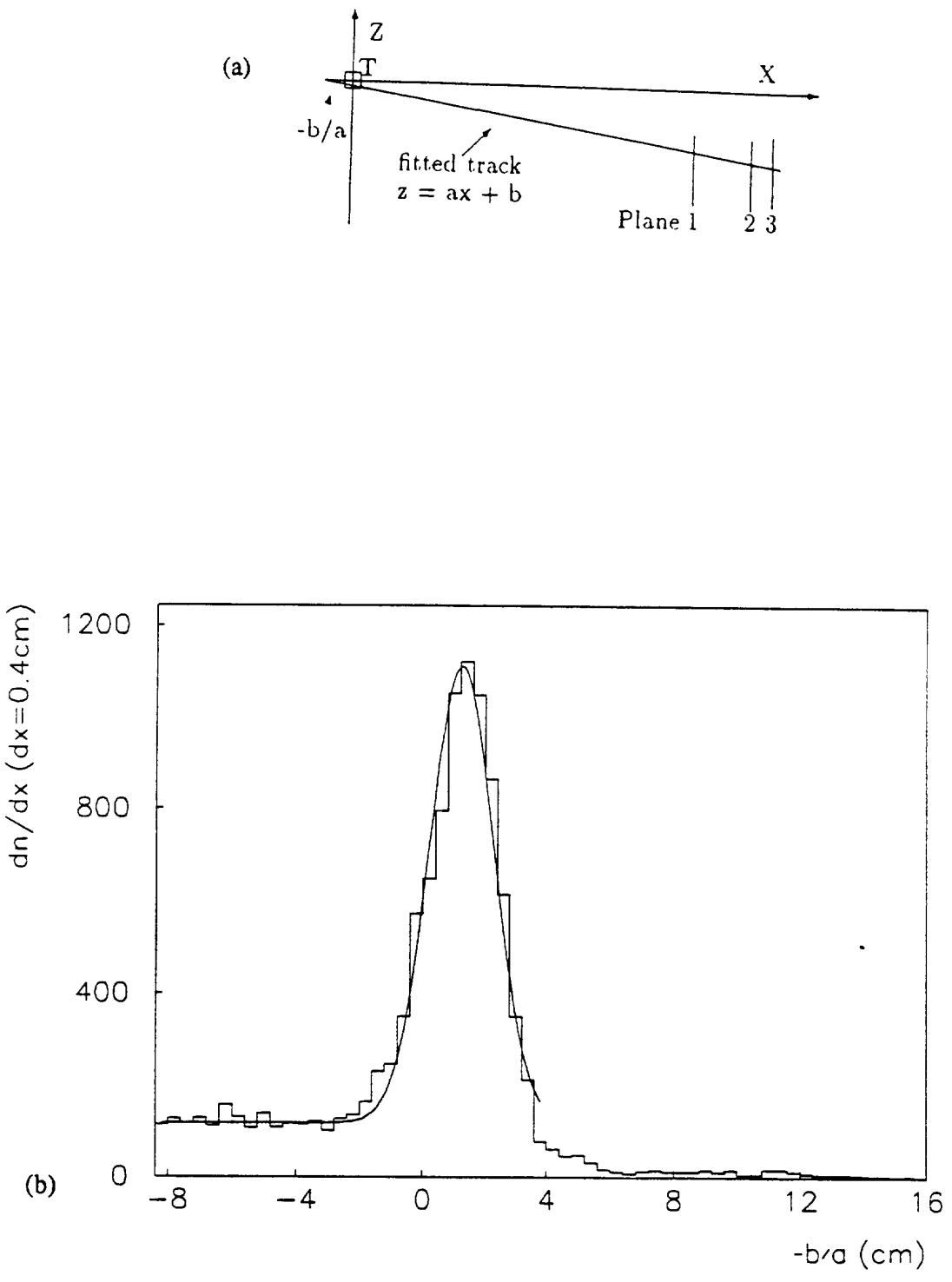

(a)
Z
T
X
-b/a
fitted track
z = ax + b
Plane 1
2 3
(b)
dn/dx (dx=0.4cm)
1200
800
400
0
−8
−4
0
4
8
12
16
-b/a (cm)

Fig. 18

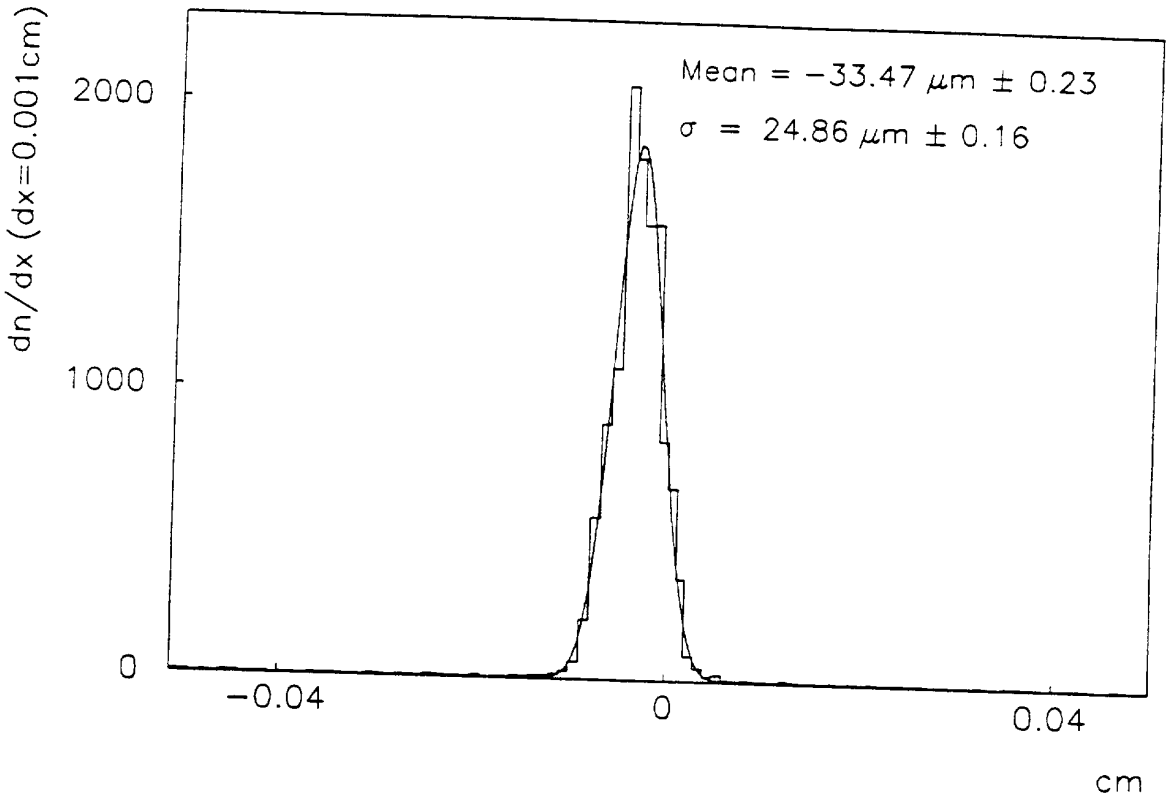

dn/dx (dx=0.001cm)
2000
1000
0
−0.04
0
0.04
cm
Mean = −33.47 μm ± 0.23
σ = 24.86 μm ± 0.16

Fig. 19

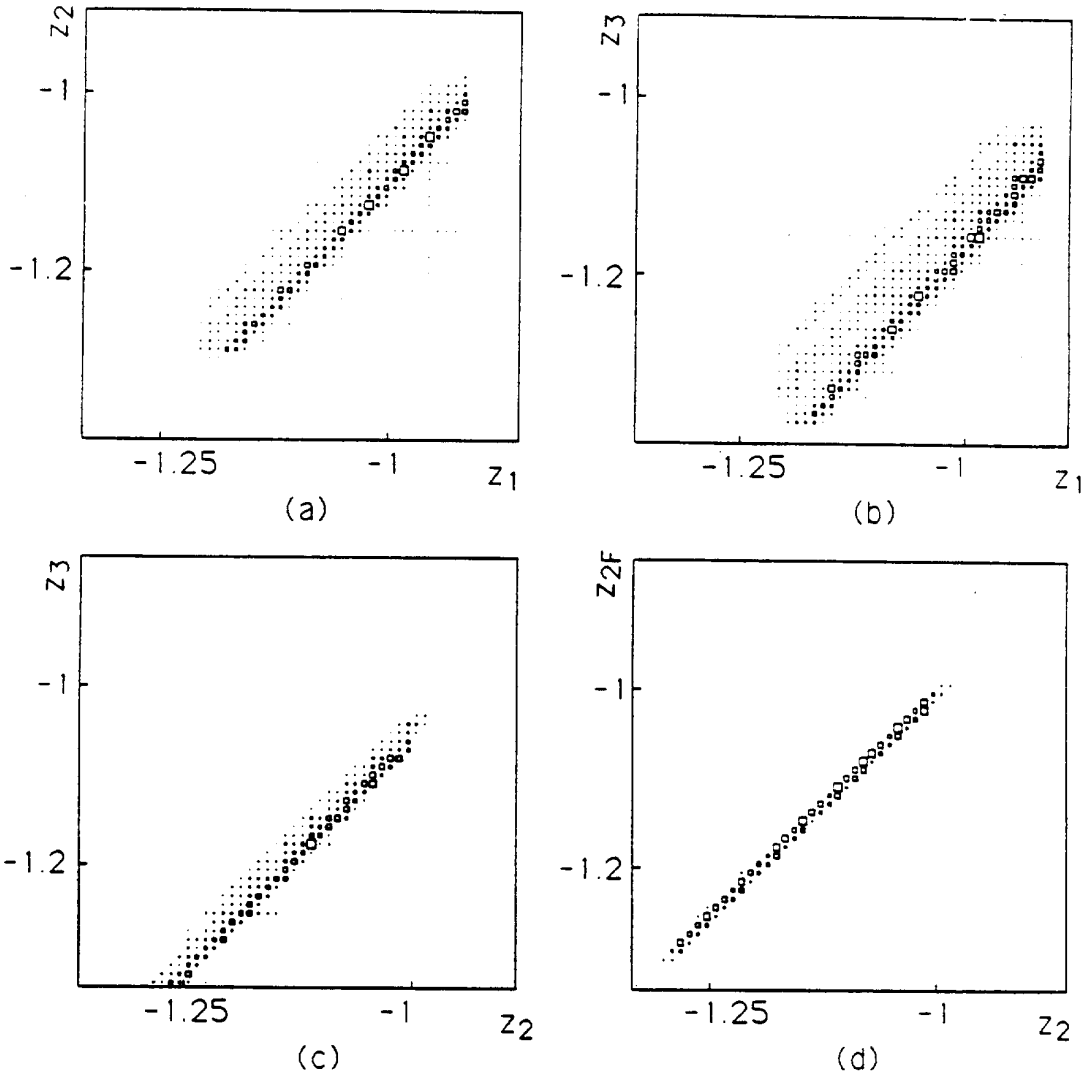


Fig. 20

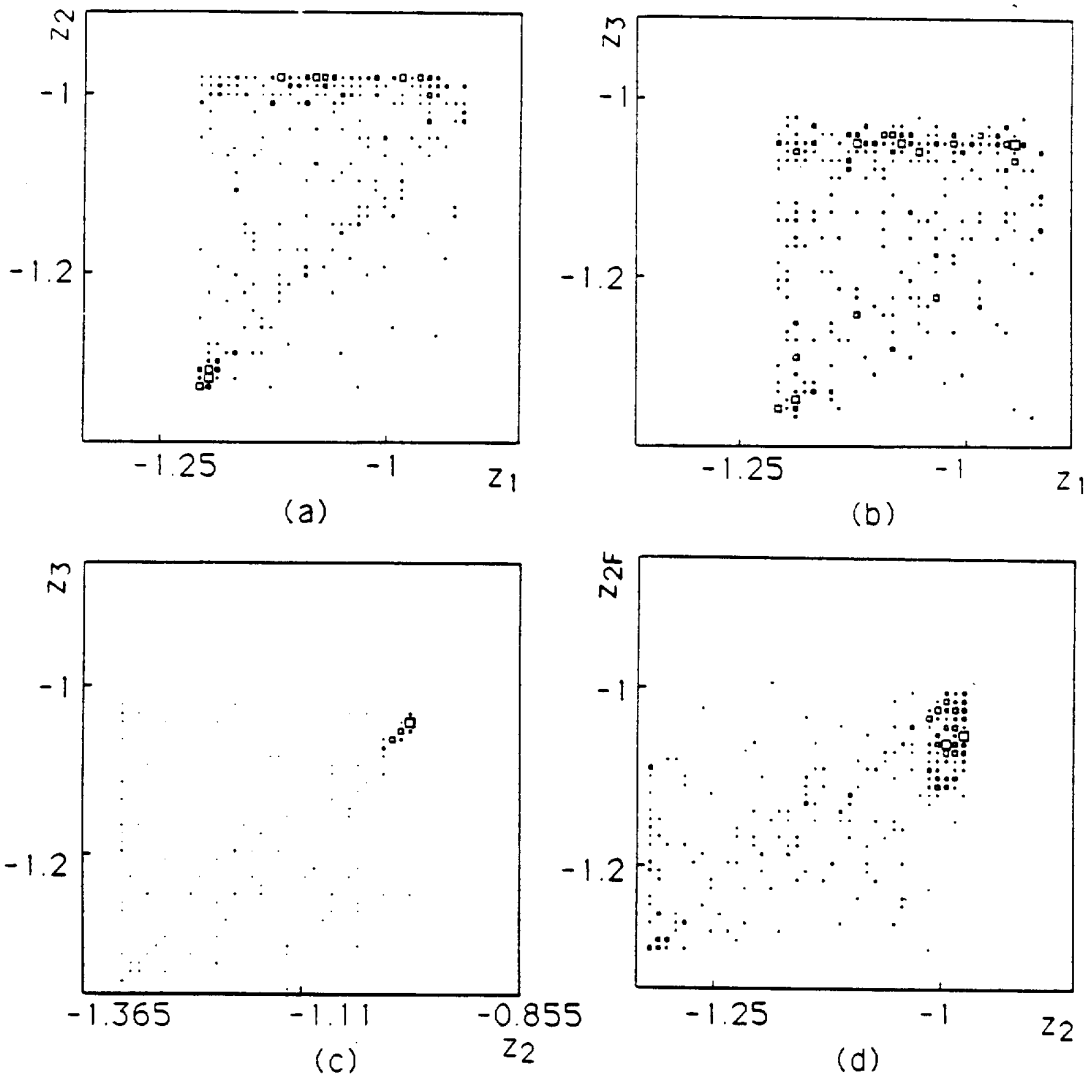

z2
-1
-1.2
-1.25
-1
z1
(a)
z3
-1
-1.2
-1.25
-1
z1
(b)
z3
-1
-1.2
-1.365
-1.11
-0.855
z2
(c)
z2F
-1
-1.2
-1.25
-1
z2
(d)

Fig. 21

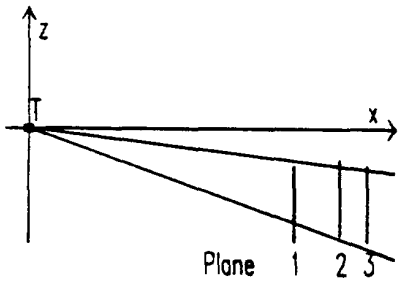


Fig. 22

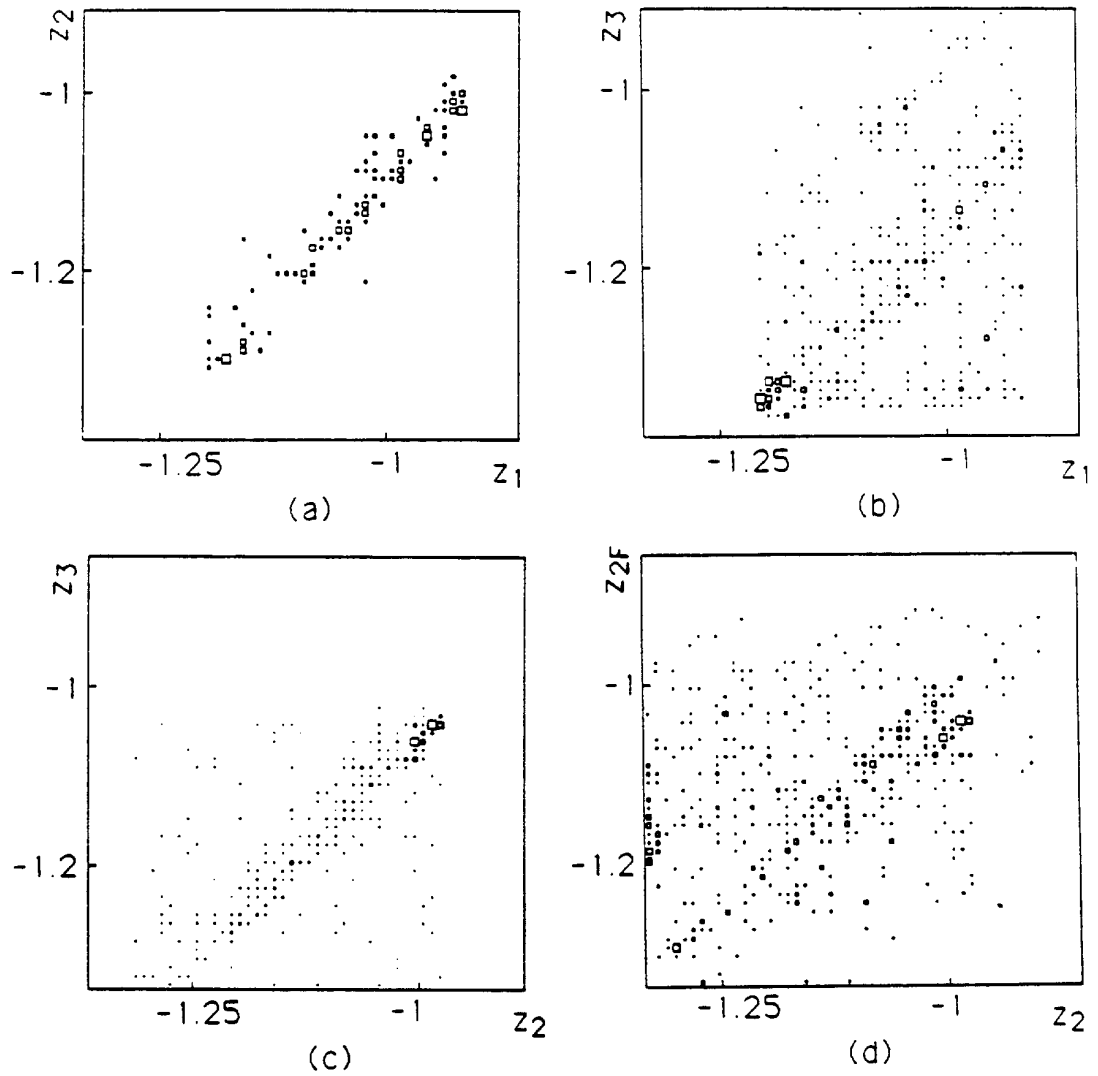


Fig. 23

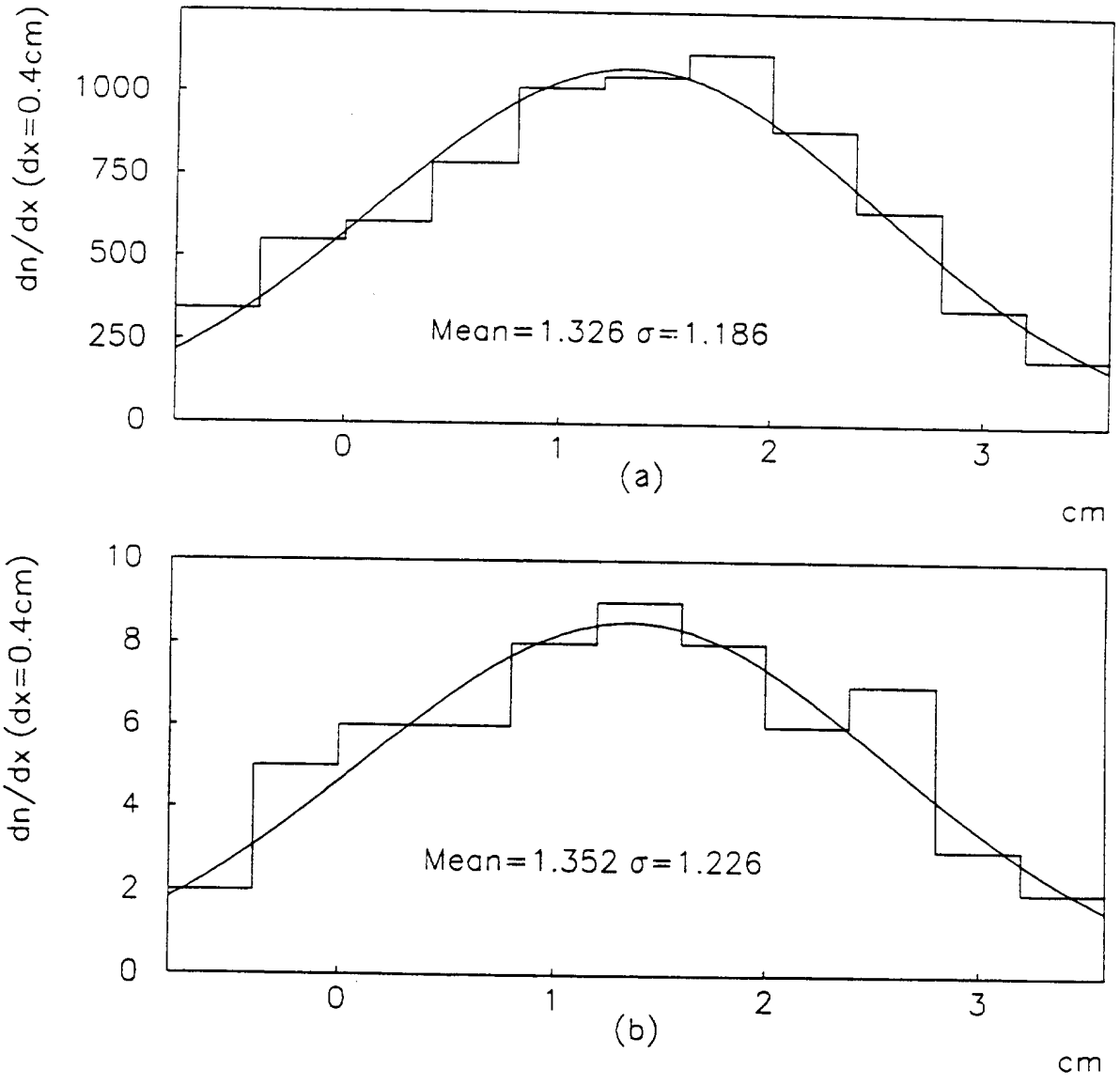

dn/dx (dx=0.4cm)
1000
750
500
250
0
Mean=1.326 σ=1.186
0
1
2
3
(a)
cm
dn/dx (dx=0.4cm)
10
8
6
4
2
0
Mean=1.352 σ=1.226
0
1
2
3
(b)
cm

Fig. 24

Integration of CMOS-electronics and particle detector diodes in high-resistivity silicon-on-insulator wafers

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(Detector R&D Collaboration RD19)

Abstract

A new approach to monolithic pixel detectors, based on SOI wafers with high resistivity substrate, is being pursued by the CERN RD19 collaboration. This paper reports on the used fabrication methods, and on the results of the electrical evaluation of the SOI - MOSFET devices and of the detector structures fabricated in the bulk. The leakage current of the high-resistivity PIN-diodes was kept in the order of 5 to 10 nA/cm^2. The SOI preparation processes considered (SIMOX and ZMR) produced working electronic circuits and appear to be compatible with the fabrication of detectors of suitable quality.

1. INTRODUCTION

The availability of "intelligent" pixel detectors, with a typical element size of the order of 100 mm, would be a precious resource for inner tracking and vertex detection in the next generation of extremely high luminosity colliders. In order to take advantage of the unambiguous pattern recognition capability of these detectors, and meet the speed and signal/noise requirements, a substantial amount of signal processing and control electronics must be located within the area of each pixel. This may be realized in either a hybrid (flip-chip) or a monolithic technology. The monolithic option offers potential benefits.

Monolithic co-integration of detectors and read-out electronics in high-resistivity silicon substrates has been reported before [1-5]. Although promising, these approaches showed serious disadvantages. In ref. [1-2], two-sided processing of the wafers is required. The approach in ref. [3-4] yields a geometrical fill-factor for the detectors below100%, unless serious limitations are accepted in the type of read-out electronics. Neither method allows the use of full CMOS circuitry.

Recently a different approach to monolithic devices has been pursued in the CERN RD-19 collaboration. Here, the detector diodes are fabricated in a high resistivity silicon substrate, while the CMOS electronic devices are located in an overlying SOI layer.

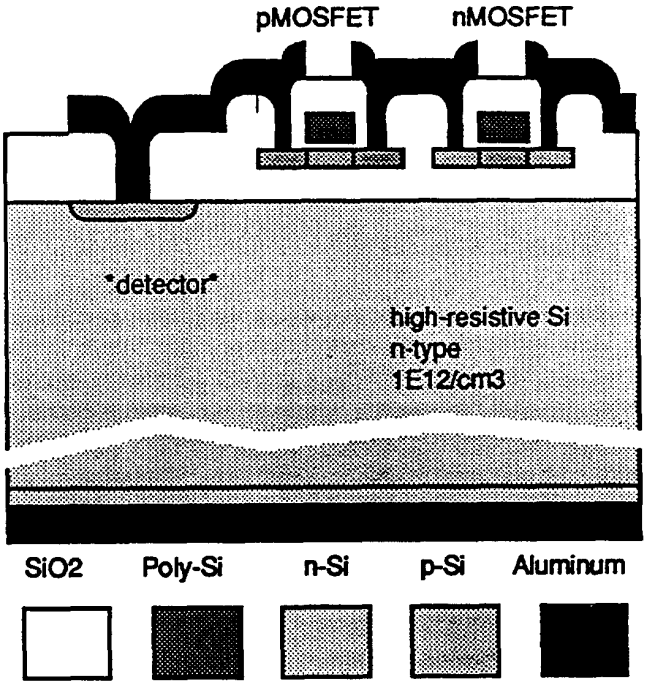

Fig.1 Schematic cross section of a processed SOI wafer with top layer electronics. (i.e. interconnects and complementary

MOSFETs) that are connected to a PIN diode in the high-resistivity bulk material.

The development at IMEC explores the possibility to process CMOS circuits in either SIMOX ("separation by implantation of oxygen") or ZMR ("zone melt recrystallization") layers on top of high resistivity substrates (fig. 1). This combination promises the following benefits:
•well-established CMOS design method and good compatibility with earlier designs
•relative radiation hardness of SOI compared to bulk processes
•there is no need for hybridization of detectors with external electronics. The mass will be lower, the reliability higher, with less parasitic effects. Yet the geometrical fill factor can be 100%. Also very narrow pitch detectors will become feasible.
•Costs will decrease if wafers are processed in larger numbers.

The price to pay for the elegance of such an SOI approach is a slightly more complex processing. SOI fabrication techniques or process temperature steps may influence the quality of the high-resistivity material. Also, the presence of electronics close to the detector will cause electrical interference or cross-talk.

The emphasis is on studying the compatibility of the SOI wafer preparation processes considered with the properties required from a high resistivity substrate in order to obtain detectors of suitable quality. In particular, the SIMOX process, involving a very heavy oxygen implant and an extended (typically 6 hours) anneal at high temperature (around 1360 °C), is worrying because of the possible introduction of contaminants or structural defects. This may results in high leakage currents, signal charge trapping, unpractical depletion voltages in the detectors. ZMR requires a lower (but still high) temperature process; here however the non-uniform heating of the wafer is another possible source of crystal defects.

II. Feasibility Study

In the first phase of the project, completed in 1991, a preliminary "feasibility" study has been performed. High resistivity wafers (4", 400 mm thick, FZ 5 kΩcm n-type <100>) were subjected to 3 SOI layer fabrication methods:
•SIMOX (separation by implantation of oxygen)
•laser ZMR (zone melt recrystallization by laser heating)
•Strip heater ZMR (zone melt recrystallization by halogen lamp heating)
Subsequently the top layer was stripped off, and the material quality was evaluated with a simple diode process for two main characteristics: diode leakage and possible dopant concentration increase.

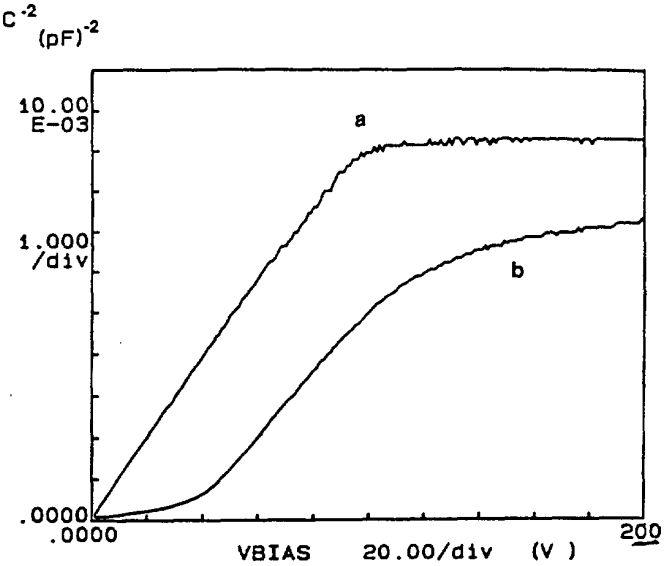

Fig.2 $1/C^2$ versus bias voltage for 0.38 cm^2 diodes on: a) laser ZMR substrate, b) SIMOX substrate. f = 1MHz.

Fig. 2a shows the $1/C^2$ versus V slope for a diode on a ZMR wafer. The constant slope indicates a uniform dopant concentration in the bulk ($N_D=8x10^{11}cm^{-3}$), and a total depletion voltage of about 100 V can be deduced from the saturation point. The corresponding curve for a SIMOX wafer (Fig. 2b) shows non-uniform doping and a still not totally depleted substrate at 200V bias. A doping profile extending almost to the back surface of the substrate is shown in fig.3. Two peaks in the net effective donor concentration are present, at about 50 mm distance from the front and back surfaces of the wafer. In the central region the dopant density is the same as for the ZMR samples, while the peaks are about an order of magnitude higher. Low temperature DLTS measurements performed on the samples are consistent with the hypothesis that these effective dopants are double oxygen donors originating from the SIMOX implant and subsequent thermal treatments.

The effect of SOI fabrication processes on the carrier generation lifetime of the substrates are deduced from reverse-biased I-V measurements. The lowest currents were obtained from the ZMR wafers (fig. 4a). Approximately uniform carrier generation in the bulk dominates the current, as can be seen from the shape of the I-V curve, roughly following a square root dependence, and saturating at total depletion of the substrate. For this device , a carrier generation lifetime of about 0.25 ms can be calculated. On SIMOX wafers leakage currents were higher; an example is shown in Fig.4b, corresponding to a generation lifetime of 0.08 ms.

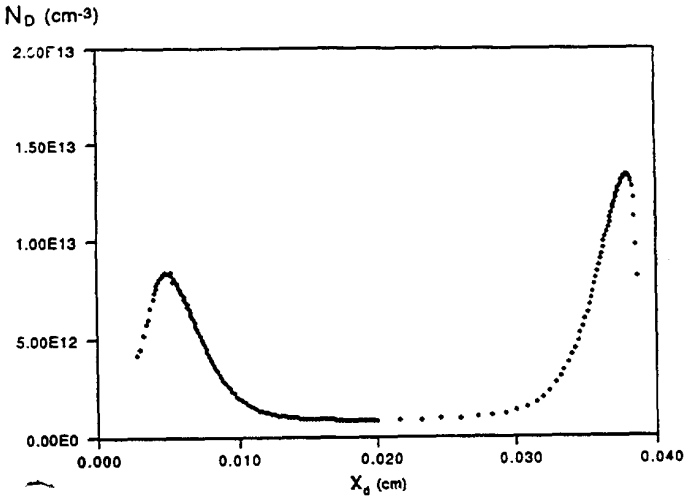

Fig.3 Profile of effective donor density versus depletion depth in the SIMOX substrate. This plot has been obtained from the combination of two 1 MHz C-V measurements: the first one covers the region up to 100 V bias, while the second extends to 400 V.

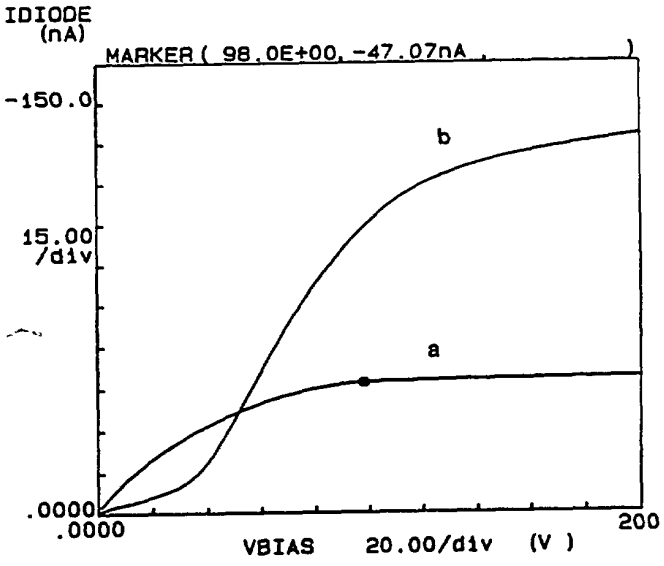

Fig.4 Reverse leakage current versus bias voltage for the same diodes as in Fig. 2

While these lifetimes are one to three orders of magnitude smaller than the best silicon detectors, they are still perfectly adequate for small volume devices: with a 80 ms lifetime, in a (100 mm)^2 pixel, 200 mm thick, the bulk generation would only contribute 20 pA at room temperature (23 °C). Furthermore, the main foreseen applications for such devices will be in heavy radiation environments, with high neutron and charged particle fluxes, where the lifetime is doomed to decrease to much lower levels during operation of the detector. In SIMOX wafers, the regions of increased dopant density do not appear to feature significantly higher thermal generation. They might have an effect on the charge collection efficiency by trapping - yet we see no evidence of slow trapping in the C-V measurements. Studies of this aspect, using ionizing particles or IR-light, are under way, as well as test of possible interactions of the SIMOX-related defects with displacement damage caused by e.g. neutron irradiation.

The conclusion of the study was that all three methods are suited for the fabrication of pixel detectors.

III. SOI ON HIGH-RESISTIVITY PROCESS

In the second phase of the project, a full "SOI-on-HΩ" process was executed at IMEC. The starting material was n-type <100> 1500 Ωcm 5 inch diameter wafers.
SOI wafers were prepared in two ways:
a) laser-recrystallized ZMR wafers. These have a top layer thickness of 400 nm and a buried oxide thickness of 1000 nm. Lines of seeding dots are located on a 200 mm pitch.
b) SIMOX implanted wafers. The top layer thickness is 200 nm, the oxide layer is 400 nm.

An "SOI-HR" mask set was designed for this complete SOI-on-HΩ run. It contains test structures for evaluation of the CMOS process, and an SOI technology test chip. The bulk quality is evaluated on several types of diodes, capacitors, gated diodes, and bulk transistors. Structures to test the interconnects between top and bulk are also available. Further the mask contains single amplifiers (adaptations of existing designs for the HR-diode read-out), and two larger "pixel-detectors" [8]. The complete test chip measures 1.3 x 3 cm.

The SOI-CMOS technology is derived from the IMEC 1 µm SOI process, but is used here with 3 µm line widths and layout rules.
The processing steps include:
- SOI layer preparation
- active area definition
- n-channel and p-channel conditioning (V_{th} adjust, film doping)
- gate poly definition
- bulk diode junction area definition
- n-type and p-type source-drain implant
- contact holes and single layer metallization
- passivation layer and bonding pad openings

The process was executed in the first half of 1992.

IV. "SOI-ON-HΩ": BULK BEHAVIOUR

For what concerns the devices in the substrate, the

relevance of this phase resides in the fact that the wafers have now undergone a full CMOS fabrication process, in addition to the special steps necessary for the substrate diodes.
Measurement results confirm the findings of the previous study. Profiles of the effective dopant concentration versus depth (obtained from C-V measurements on 1 cm^2 diodes) are shown in fig. 5. For the ZMR wafers the doping is uniform, about 2.5 x 10^{12} cm^{-3}, while in the SIMOX substrates the known peak concentration of 1 x 10^{13} cm^{-3} is seen at a depth of 40-50 mm. Due to the higher thickness of the wafers (625 µm) and the lower initial resistivity, the total depletion voltage is about 730 V for the uniformly doped ZMR wafers, and even higher for the SIMOX. Junction breakdown did prevent to profile down to the back surface, but a rising concentration beyond 500 µm is a hint of the presence of a second peak at the backside.

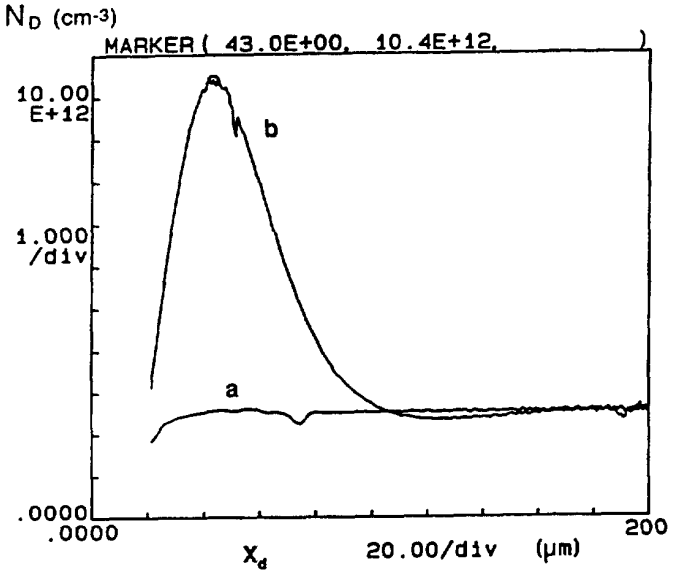

Fig.5 Profile of effective donor density versus depletion depth in the substrate: a) on laser-ZMR wafer, b)on SIMOX wafer. f = 100 KHz.

Further evidence for the plausibility of the interpretation of these peaks as due to oxygen-related "thermal donors", which are activated at around 450 °C, came from the following experiment: One wafer was withdrawn before the final metallization sintering, and profiled: the peak was still visible, but about one third as high as for the sintered wafers. Subsequently the wafers was sintered, and the peak grew to the level of the other wafers. The possibility exists to modify the thermal schedule of the process in order to reduce the amount of these donors (they are known to annihilate around 600 °C).

The leakage currents achieved in the first complete processing, which are significantly lower than the values found in the feasibility study, are typically 5 to 20 nA/cm^2 at 100 V bias; the difference between ZMR and SIMOX is now hardly significant. The corresponding values of the carrier generation lifetimes are 0.5 - 1 ms for the ZMR and 0.3 - 0.6 ms for the SIMOX.
Surface generation at the depleted (bulk silicon) - (buried SOI oxide) interface has been evaluated with gate-controlled diodes specifically designed for this purpose, featuring interdigitated gate and diode electrodes. The surface generation velocity is in the range 15 - 20 cm/s for both ZMR and SIMOX. The interface between the substrate and the SOI oxide was also studied by standard high frequency and quasistatic C-V measurements on MOS capacitors. The curves for a ZMR wafer are shown in Fig. 6. From these, a total effective oxide charge N_{eff} ≈ 7 x 10^{10} cm^{-2} can be derived, and an interface trap density at midgap D_{it} ≈ 3 x 10^{10} $cm^{-2}eV^{-1}$. These values are only an order of magnitude higher than the best thermal oxides grown on (100) substrates. For the SIMOX samples, the technique gave inconsistent results.

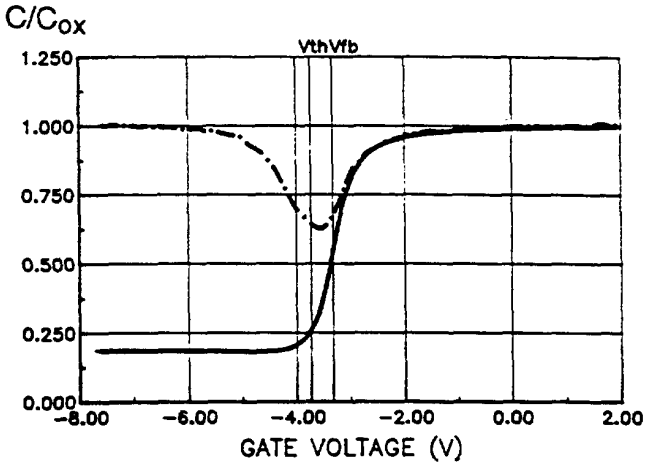

Fig.6 High frequency (100 kHz, solid line) and quasistatic (dotted line) C-V curves for a MOS capacitor on a laser-ZMR wafer.

V. "SOI-ON-HΩ": MOSFET BEHAVIOUR

We considered MOSFETs (Fig. 7a), lateral diodes, sheet resistances and metal interconnects as basic top layer devices. Of these the properties of the MOSFETs are especially important for the following reasons:
•the so-called "kink", a typical non-linearity in the I_D-V_{DS} characteristics of SOI MOSFETs, and the possible suppression of it.
•the coupling of the MOSFET current level to the potential in the substrate, or the back-gate effect. It is closely related with the first effect.
•low-frequency noise (1/f noise), as an important parameter for the envisaged applications.

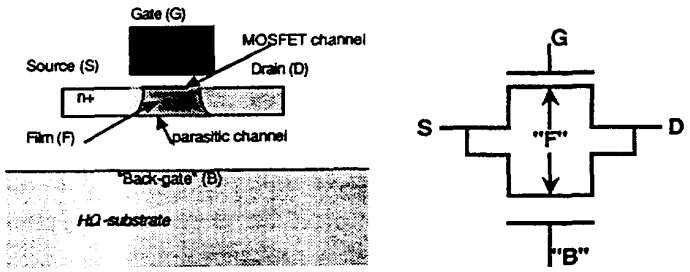

Fig.7 Schematic cross section of a nMOSFET in an SOI layer (a), and equivalent circuit (b). The normal MOS channel is driven by the gate (G) potential. Due to the SOI device nature, there exists a second parasitic channel at the backside of the film. The "back gate" (B), i.e. the surface potential in the high-resistivity substrate, influences both the backside and the front side channel. The film (F) plays the role of the "bulk" terminal in a "classical" MOSFET. An undepleted film is useful in avoiding the kink and reducing the backside - front side coupling.

Except for a high V_{th} in the pMOSFETs (-2.0 V), MOSFET operation is excellent. The kink can be suppressed by explicitly grounding the film, as illustrated in fig.3. The kink effect can be understood as an uncontrolled varying "film"-source voltage (V_{FS}), changing the drain current through the bulk effect (Fig.8 and 9).

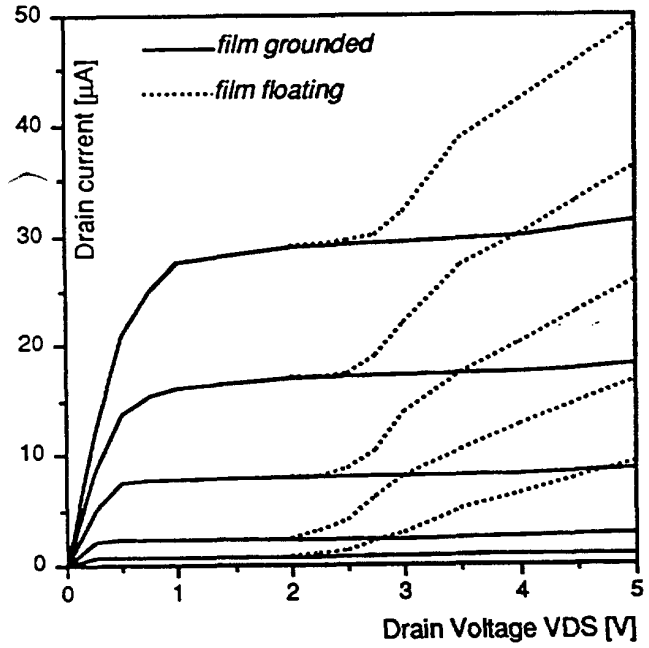

Fig.8 I_D/V_{DS} characteristics of an SOI nMOSFET; W=10 mm; L=10mm; V_{BS}=0; V_{GS} = 1, 1.25, 1.5, 1.75 and 2 V. Plain line: film contact grounded (V_{FS}=0). Dashed line: film contact floating (unconnected).

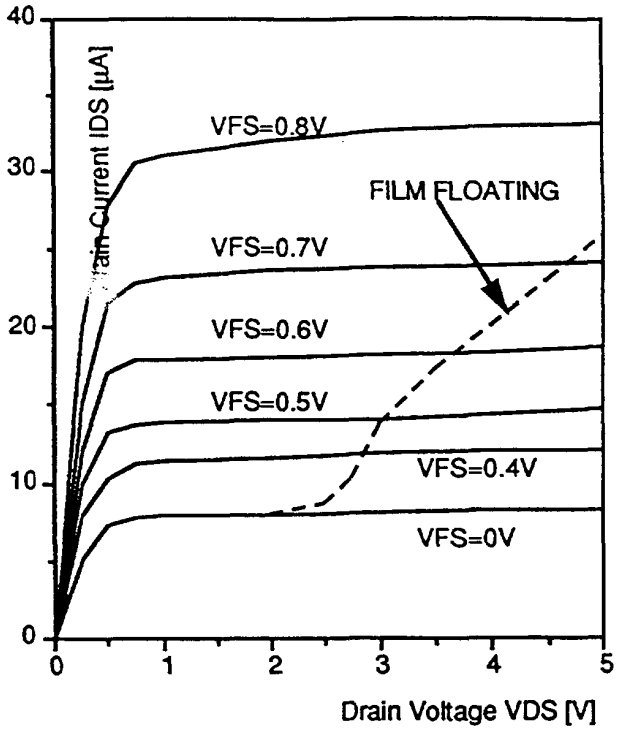

Fig.9 I_D/V_{DS} characteristics of an SOI nMOSFET, for a fixed V_{GS} = 1.5 V and V_{BS} = 0 V, and a set of film voltages V_{FS}. The dashed line is the curve for a floating film contact.

A second effect in SOI MOSFETs that is not seen in bulk MOSFETs is rising from the fact that an SOI MOSFET consists of actually two MOSFETs, placed back-to-back (Fig. 7b). The top transistor is the one intended by the circuit designer, yet there always is a parasitic "backside" MOSFET that shares the source, drain and film of the top MOSFET, but has the SOI substrate potential as gate. In the envisaged application, typically MOSFET circuitry on top of PIN detectors, fluctuations in the detector potential will possibly feed-back to the MOSFET's parasitic mode of conduction. Grounding the film reduces a bit the coupling of the substrate potential to the MOSFET current. Heavy counter-doping the parasitic backside channel will prevent backside conduction. This type of implantation is a critical step in the process, as it must cut off the backside channel without affecting the normal front side channel. This, and radiation hardness, are reasons to prefer a silicon film thickness of more than 200 nm.

Results on the low-frequency noise on MOSFETs obtained from this process are summarized in Table 1. They are slightly worse, but comparable with typical values for a bulk CMOS process used in analog design (LUVCMOS 3U0, IMEC). As a figure of merit we use the Kf factor, as defined by a widely used empirical relation for the equivalent gate

noise spectral density ($S_{V_{Geq}}$) in silicon MOSFETs:

$$S_{V_{Geq}}(f) = Kf/W.L.f \qquad (1)$$

where W and L are the transistor's width and length, and f is the frequency.

process	SOI-on-HΩ SIMOX	LUVCMOS
nMOSFETs	$Kf = 3.8 \times 10^{-20}$	2.0×10^{-20}
pMOSFETs	$Kf = 4.5 \times 10^{-20}$	3.0×10^{-21}

Table 1. Average Kf [V^2m^2] obtained from low frequency noise measurements. 10 MOSFETs of different sizes were measured at several working points. Measurement frequency f is 1 Hz. Drain currents ranging from nA to mA. No significant dependence of the Kf values on the working point was seen.

VI. CONCLUSIONS

The results of the project have proven the feasibility of the monolithic integration of particle detectors and associated electronics. In the SOI top layer (CMOS) devices have a quality that is comparable to bulk CMOS technologies. Also the operation of large analog/digital circuits was demonstrated (i.e. arrays of detector/amplifiers). SIMOX is the material of choice for the top layer devices, as the reproducibility and yield is high, and it does not require the presence of a grid of seeding points and anti-reflective stripes as is used for the laser-ZMR process. A problem area for the design of top layer electronics is the kink non-linearity and the back-gate effect of the top layer MOSFETs. These will be optimized in the scheduled processing runs.

With reference to the detecting elements in the substrate, ZMR wafers give very good results. For SIMOX wafers, the main concern is the higher depletion voltage resulting from the increase in effective doping concentration. Optimization of the process may lead to a reduction of this effect. In addition, charge trapping and radiation damage effects need to be investigated.

For the first time a co-integration of CMOS electronics and high-resistivity PIN-detectors has been demonstrated using an SOI approach.

VII. REFERENCES

[1] W. Snoeys, "A new integrated pixel detector for high energy physics", Ph.D. dissertation, Stanford University, California, USA (1992).

[2] W. Snoeys & al., "A new integrated pixel detector for high energy physics", paper presented at the 1991 IEEE Nucl. Science symposium, Santa Fe, to be published in IEEE Trans. on Nucl. Sci.

[3] G. Vanstraelen, "Monolithic integration of solid-state particle detectors and their read-out electronics on high-resistivity silicon", Ph.D. thesis, Katholieke Universiteit Leuven, Leuven, Belgium (1990).

[4] G. Vanstraelen & al., "New concepts for integrated solid state detector electronics", Nucl. Instr. and Methods, vol. A273, p.625 (1988).

[5] S. Holland, "An IC-compatible Detector process", IEEE trans. Nucl. Sci., vol. NS-36, p.283 (1989).

[6] B. Dierickx & al., "Integration of CMOS-electronics in an SOI layer on high-resistivity silicon substrates", presented at the IEEE Nucl. Science Symp., Orlando, Nov. 1992.

[7] L. Bosisio & al., "Detector diodes and test devices fabricated in high-resistivity SOI wafers", presented at the IEEE Nucl. Science Symposium, Orlando, Nov. 1992.

[8] B. Dierickx, "Position encoding smart pixel arrays", Nucl. Instr. and Methods, vol. A305, p.561 (1991).