


# The ITS3 detector and physics reach of the LS3 ALICE Upgrade

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**Abstract.** During Large Hadron Collider (LHC) Long Shutdown 3 (LS3) (2026-28), the ALICE experiment is replacing its inner-most three tracking layers by a new detector, Inner Tracking System 3. It will be based on newly developed wafer-scale monolithic active pixel sensors, which are bent into truly cylindrical layers and held in place by light mechanics made from carbon foam. Unprecedented low values of material budget (per layer) and closeness to interaction point (19 mm) lead to a factor two improvement in pointing resolutions from very low  $p_T$  ( $O(100\text{MeV}/c)$ ), achieving, for example, 20  $\mu\text{m}$  and 15  $\mu\text{m}$  in the transversal and longitudinal directions, respectively, for 1 GeV/c primary charged pions. After a successful R&D phase 2019-2023, which demonstrated the feasibility of this innovational detector, the final sensor and mechanics are being developed right now. This contribution will briefly review the conceptual design and the main R&D achievements, as well as the current activities and road to completion and installation. It concludes with a projection of the improved physics performance, in particular for heavy-flavour hadrons, as well as for thermal dielectrons, that will come into reach with this new detector installed.

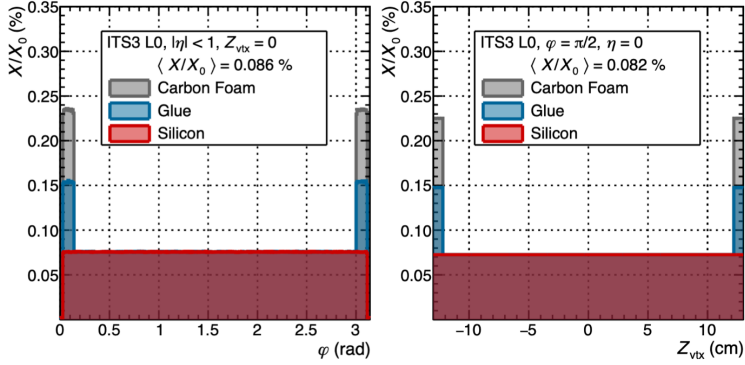
## 1 Introduction

ALICE (A Large Ion Collider Experiment) is a detector at LHC specifically designed to investigate high-energy heavy-ion collisions, which could lead to the formation of the quark-gluon plasma, a colour-deconfined state of the matter. To achieve this, ALICE is equipped with multiple detectors, including the ITS, which plays a crucial role in determining the interaction and decay vertices and precisely tracking particles with low momentum and angular resolution in conjunction with the TPC and other detectors. The ITS was upgraded during LHC LS2 to the ITS2, which is constructed using ALPIDE chips based on 180 nm CMOS technology [1].

With advances in chip manufacturing technology, wafer-scale chips can now be produced using stitching techniques. This development has opened new avenues for the next upgrade of the ITS. After a successful R&D phase 2019-23, a next-generation ITS3 design has been proposed by ALICE [2], aimed at replacing the innermost three tracking layers of ITS2 during LHC LS3 (2026-28). ITS3 features three layers of wafer-scale chips manufactured using

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**Figure 1.** Material budget for tracks of particles originating from the interaction point as a function of the azimuthal angle  $\phi$  (left panel) and the coordinate of the interaction vertex along the beam axis  $Z_{\text{vtx}}$  (right panel)

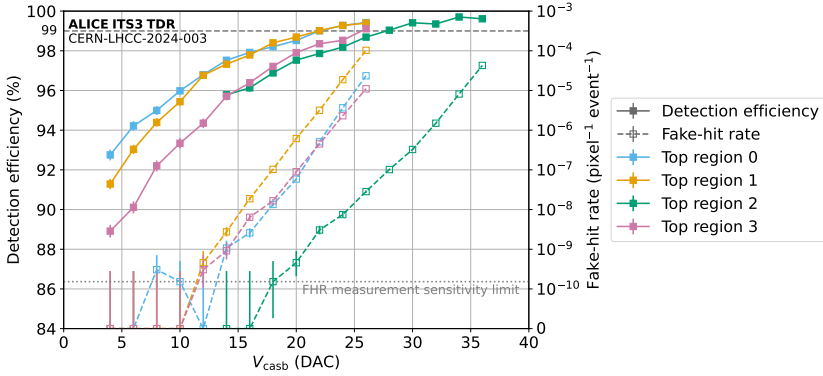
stitching technology, and these chips will be bent into a half-cylinder shape. The chips, based on 65 nm CMOS MAPS technology, with a power density below 40 mW/cm<sup>2</sup>, allow for air cooling to replace the water cooling system used in ITS2. These improvements will significantly reduce the material budget from 0.35%  $X_0$  to 0.07%  $X_0$  per layer from ITS2 to ITS3. Additionally, the material distribution will become more uniform as Fig. 1 illustrates. Furthermore, the beam pipe's radius will be reduced from 18.2 mm to 16.0 mm, leading to a decrease in the radius of layer 0 of ITS3 from approximately 24.0 mm to 19.0 mm.

## 2 Chip design and characterization

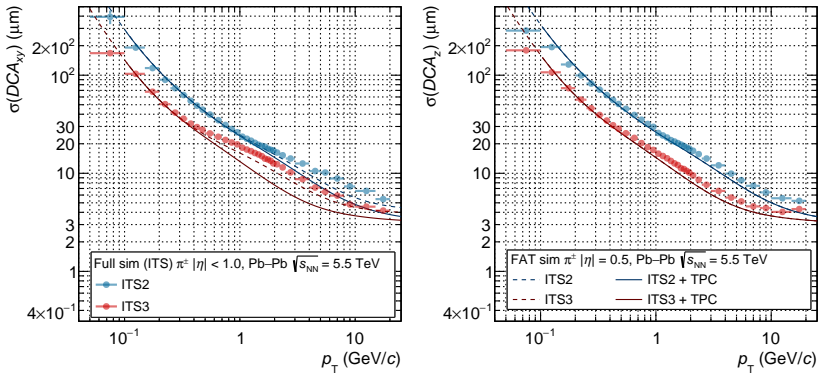
Supporting this ambitious design, the chip development for ITS3 involves multiple phases. In the first phase, the MLR1 phase, three types of chips—Analogue Pixel Test Structure (APTS), Digital Pixel Test Structure (DPTS), and Circuit Exploratoire 65 nm (CE65). Through this phase, the 65 nm process chips were thoroughly studied, including the confirmation of radiation hardness. Even when subjected to 100 times the radiation dose required for ITS3 (10 kGy and  $10^{13}$  1MeV  $n_{\text{eq}}$  cm<sup>2</sup>), the detection efficiency of the chips remained sufficiently high, and the spatial resolution was almost unaffected. For more detailed results, please refer to Ref. [3].

In the ER1 phase, ALICE designed two types of wafer-scale chips: MOlonithic StIched sensor (MOSS) and MOlonithic StIched sensor with Timing (MOST). The MOSS chip is the first stitched chip used for high-energy physics, with a length of 259 mm and a width of 14 mm. The MOSS chip is segmented into a left end cap (LEC), a right cap (REC), and 10 repeated sensor units (RSU), with each RSU containing a top and a bottom half-unit. The top half-unit is divided into four pixel regions, where each pixel has a width of 22.5 $\mu$ m, and there are 256  $\times$  256 pixels per region, with slight design variations among the regions. The bottom half-unit is also divided into four regions, each with a pixel width of 18 $\mu$ m and 320  $\times$  320 pixels. Fig. 2 shows the beam test results for the MOSS chip at CERN PS, which indicate that the MOSS chip achieves a detection efficiency of over 99% with a very low fake-hit rate, below  $10^{-6}$  pixel<sup>-1</sup> event<sup>-1</sup> for region 2 when operated at an optimal working point. More detailed description can be found in the ITS3 TDR[2].

The successful design of the MOSS chip has confirmed the effectiveness of using wafer-scale chips for particle detection, and provided the guidance for the design and fabrication of ITS3 chips in the subsequent ER2 phase.



**Figure 2.** Detection efficiency and fake-hit rate as a function of  $V_{\text{casb}}$  (inversely proportional to the threshold in number of electrons) measured for MOSS at the CERN PS.

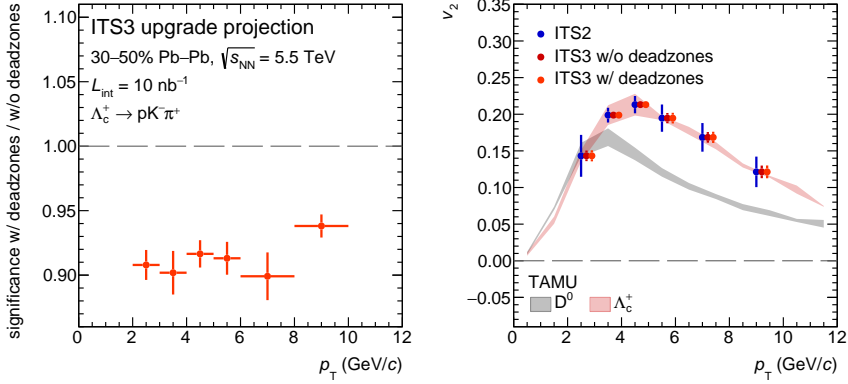


**Figure 3.** Impact parameter resolution in the  $r\phi$  (left panel) and longitudinal (right panel) direction for primary charged pions with  $|\eta| < 1$  as a function of the track  $p_T$  for ITS2 and ITS3 detectors from the  $O^2$  simulation

### 3 Physics performance and physics reach of ITS3

Using the  $O^2$  framework [4] developed by ALICE for the reconstruction, calibration, and simulation of the ALICE experiment for LHC Run 3 and 4, the impact parameter resolution of ITS3 has been estimated using two simulation methods: full simulation and fast analytic tool (FAT), both yielding consistent results. Compared to the ITS2, the ITS3 is expected to achieve a twofold improvement in impact parameter resolution [7]. This will greatly benefit numerous analyses, such as studies of the participation of heavy-flavour particles in the collective motions of the system created in heavy-ion collisions

The production of heavy flavor particles in the QGP mainly arises from two mechanisms: fragmentation, where the transition from heavy quark to hadron occurs via the emission of a parton shower, resulting in a hadron that carries a fraction of the original parton momentum, and coalescence, where partons close in phase space can recombine. These two mechanisms contribute differently to the elliptic flow coefficient [5] of heavy-flavor particles. The performance of the ITS3 in reconstructing heavy-flavor particles is expected to be significantly better compared to the ITS2. As shown in the left panel of Fig. 4, although the dead zones have a minor impact, the reconstruction remains extremely precise, leading to accurate flow calculations. The right panel of Fig. 4 further demonstrates, according to the TAMU model [6], that in the  $p_T > 4$  GeV/c region, there will be a significant difference in the flow of  $\Lambda_c^+$



**Figure 4.** Left: Ratio between the expected significance with or without deadzones. Right panel: Comparison of the expected performance for the measurement of the  $\Lambda_c$  elliptic flow with the ITS2 and the ITS3 with and without deadzones.

and  $D^0$  particles. With ITS3, the statistical uncertainty in the  $v_2$  measurement for  $\Lambda_c^+$  can be reduced by up to a factor of 4. This study utilizing ITS3 will further constrain the modeling of charm diffusion and hadronization in the QGP. More details on the physics performance can be found in Ref. [7].

## 4 Summary

The ITS3, a bent wafer-scale monolithic pixel detector, is set to replace the ITS2 inner barrel during LHC LS3. Characterization results from each phase of chip design and production have confirmed that the bent 65nm process wafer-scale chips fully meet the requirements of ITS3, including radiation hardness, spatial resolution, and detection efficiency. The ITS3 project remains on track for installation as planned. This upgrade, offering a twofold improvement in spatial resolution compared to ITS2, will significantly enhance various analyses, such as heavy-flavor collectivity and thermal dielectrons measurement.

The author is supported in part by the National Key Research and Development Program of China (Nos. 2022YFA1602103, 2018YFE0104600), the National Natural Science Foundation of China (No. 12322508) and the Science and Technology Commission of Shanghai Municipality (No. 23590780100).

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