Serial Powering Scheme and Performance Analysis for the Innermost Layer (L0) of ATLAS ITk modules

Md Arif Abdulla Samy[a,b], Elisabetta Pianori[b], Timon Heim[b], Emily Anne Thompson[b], Gian-Franco Dalla Betta[a,c]

[a] *TIFPA-INFN, Via Sommarive 14, 38123 Trento, Italy ,*
[b] *LBNL, 1 Cyclotron Road, Berkeley,CA, 94720, USA ,*
[c] *Dept. of Industrial Engineering, University of Trento, Via Sommarive 9, 38123 Trento, Italy ,*

Abstract

In this study, we powered in series 4 triplets based on the pre-production ATLAS FE chip for HL-LHC. We ensured that the chosen operational parameters were within our theoretical specs and resulted in the stable operation of the modules within the serial power chain. Triplets were also powered in Low Power mode (LP), used to operate the module at a lower current, and their performance was tested without cooling requirements. The performance of the under-shunt and over-voltage protection were also analyzed.

Keywords: Triplet, serial power chain, SLDO, OVP, ITkPixV1.1

1. Introduction

After ten years of massive success, the Large Hadron Collider (LHC) at CERN is going for an upgrade to the next phase, the High Luminosity Large Hadron Collider (HL-LHC) which is planned to start its operation in 2029. This is expected to have a fine boost to its performance, with an instantaneous luminosity of 5.0×10^{34} $cm^{-2}s^{-1}$ (ultimate value 7.5×10^{34} $cm^{-2}s^{-1}$) with 200 average interactions per bunch crossing which will increase the fluences up to more than 10^{16} n_{eq}/cm^2, resulting in high radiation damage in ATLAS detector [1]. To withstand this situation, it was proposed to make the innermost layer [L0] of the new Inner Tracker (ITk) with 3D silicon sensor modules, which will have a radiation tolerance of more than 1×10^{16} n_{eq}/cm^2 with a TID of 9.9 MGy [2]. Each 3D sensor is bump-bonded to a FrontEnd (FE) chip to form a bare module, and three bare modules are powered in parallel in a triplet module. The L0 layer will have 396 triplet modules. To reduce cable material and improve detector performance, 3 to 5 triplets (depending on the location of the detector) will be powered in series. The FE chip implements a number of features (like a shunt-low-dropout regulator and over-voltage and under-shunt protection [3]) needed to guarantee the stable operation of the detector with this powering scheme.

2. Assembly and Test Setup of Linear Triplet

For this study, ten linear digital triplets were assembled at Lawrence Berkeley National Laboratories (LBNL), using ITkPixV1.1 readout (RoC) chip (Figure 1), which is the pre-production chip for the ATLAS ITk. As LBNL is not an assembly site for triplets, the triplets were assembled manually using double-sided tape. The precision was ensured using a metal vacuum chuck and microscope.

A test setup was designed to test the quality of the digital triplets electrically, as can be seen from Figure 2. The setup

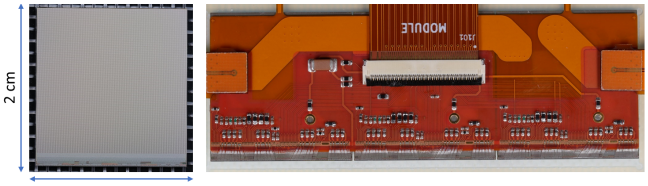

Figure 1: (a) ITkPixV1.1 (pre-production) chip, (b) Digital Linear Triplet with three ITkPixV1.1 chips.

consists of a Low voltage power supply (HMP4040), a Multimeter (DMM600) with a scanner card to enable multichannel reading and a computer with an FPGA to read from triplet. The power supply and multimeter are controlled remotely by the computer using LabRemote. The triplet was placed on a cooling plate, and cooled by glycol and water mixture to control the temperature of the triplet. At the adapter card which makes an interface for all the instruments to connect with the triplet, Vret and Ground_C pins are shorted via a jumper to bring all the grounds at the same level. To make a serial power chain,

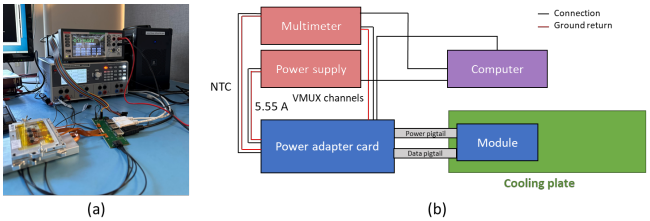

Figure 2: (a) Data acquisition setup for triplet at LBNL with HMP4040 power supply and DMM600 multimeter with ten channel scanner card, (b) Schematic of the DAQ setup, the whole system is automized with the help of LabRemote software.

four triplets were connected in series and were powered by 8 V and 5.55 A at constant current mode, as can be seen in Figure

3. Four triplets were chosen because it's an average of three and five triplets, which are the two serial powering schemes. Another reason is that an FPGA can handle a maximum of four triplets simultaneously. If the four triplets in a chain work, it can be anticipated that three and five-triplet chains will also work.

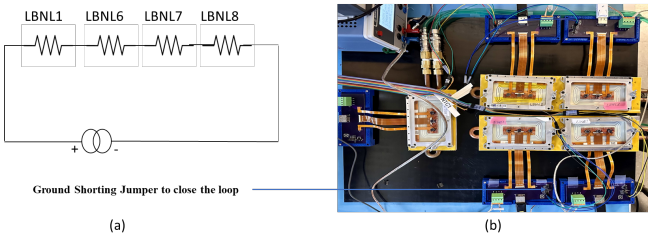

Figure 3: (a) Schematics of how four triplets are arranged to make a serial power chain. (b) Physical picture of the serial power chain, four triplets are connected with four transmission lines of four channel Ohio card, attached with the FPGA. The fifth one is not connected.

3. Result

Four triplets were selected carefully, as can be seen in Figure 4 for this study. At first, all of the triplets were tested individually to verify their electrical characteristics. An SLDO test was done, where the module input current was varied from 9.75 A (considering safety limit) to 5.55 A (nominal operational current), FE voltages were read from Vmux pin of the adapter, and the current was calculated from the input and shunt register values. This scan is important to understand the input voltage and current characteristics of the Front End registers [4]. All the chips' SLDO characteristics can be seen in Figure 5, where all the input voltages and current from all chips follow the same trend: the FE input voltages are linear, input digital current and digital shunt current is higher than analog input and analog shunt current consecutively, as expected from theoretical calculation. The input digital current gets saturated in a higher current region as the register associated with it gets saturated with the voltage. Shunt currents are always more than zero in operational mode to ensure not to enter the under-shunt region.

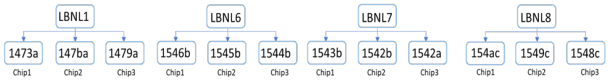

Figure 4: Triplets used in this study and its component chips. These names are given locally, all of them have been assembled at LBNL manually with double-sided tape. Chip names are derived from the wafer name and position at the wafer.

All these four triplets were then connected in series as can be seen in Figure 3(b) to form a loop as seen in Figure 3(a), so that the LBNL 1 directly gets the positive connection from the power supply, and LBNL 4 gets connected with the ground. To ensure that, only in the last adapter card, Vret and Ground_C pins are shorted. An SLDO scan was done on the setup, varying the current from 9.75 A to 5.55 A, which is the nominal operation current, at a constant current mode.

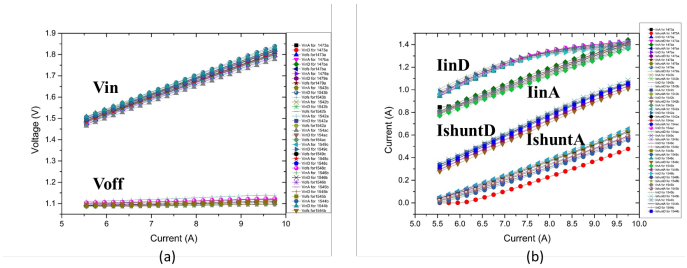

Figure 5: (a) Digital and Analog Front End (FE) input voltage vs module input current curve for all the chips enlisted in figure 4. (b) Input and Shunt current (both Digital and Analog FE) vs module input current curve.

All the triplets in the serial power chain showed similar characteristics in the SLDO scan as they showed as individual triplets, as can be seen in Figure 6. Figure 6 is plotted to put both the results as individual triplets and as a part of a serial power chain. From this plot, the results seem to be similar in trend, with slight numerical differences. To understand the specific difference study, a difference plot is created in Figure 7. LBNL 1, which is the first triplet on the chain, showed almost no difference as an individual and a part of the serial power chain (Figure 7(a) and (e)). The second triplet in the chain, LBNL 2, showed a higher difference in the case of the input digital current of one chip (Figure 7(f)) when the input current is higher than the nominal current, which could be an effect of temperature rise. Other current and voltage deviations were also a bit higher than LBNL 1 (Figure 7 (b) and (f)) but were within the limit. In the case of LBNL 3 (Figure 7 (c) and (g)) and LBNL 4 (Figure 7 (d) and (h)), this deviation was reduced, which was expected in a serial chain. One thing to note is that, at the nominal current (5.55 A) point, the deviation for all the chips is minimal. All the triplets were also powered in Low Power (LP) mode, where triplets are powered with low current (i.e., 1.8 A), and the Voffset is pushed higher by adding a square pulse provided by FPGA, both as an individual and as a part of the serial power chain. At LP mode, the SLDO scan was done from 10 A to 1.8 A. When the SLDO scan was done on individual triplets, all the chips showed similar characteristics, where at around 9 A, input FE voltages get saturated at 2 V (Figure 8 (a)), which is the Over Voltage Protection (OVP) characteristics to protect the chip. The same characteristics have also been seen on all the chips when the SLDO scan was done at the serial power chain at LP mode (Figure 8 (b)). A rise in temperature can be seen because of the sudden rise in current, which then comes to nominal temperature due to the cooling plate.

4. Conclusion

The goal of his research was to do a comparative study of electrical characteristics of triplet powering individually and as a part of a serial power chain, to understand if the scheme is feasible to power up the triplets at the detector. It was seen that the differences between FE input currents and voltages from individual triplet and as a part of the serial power chain at nominal current is minimal. LP mode also worked in the same way in

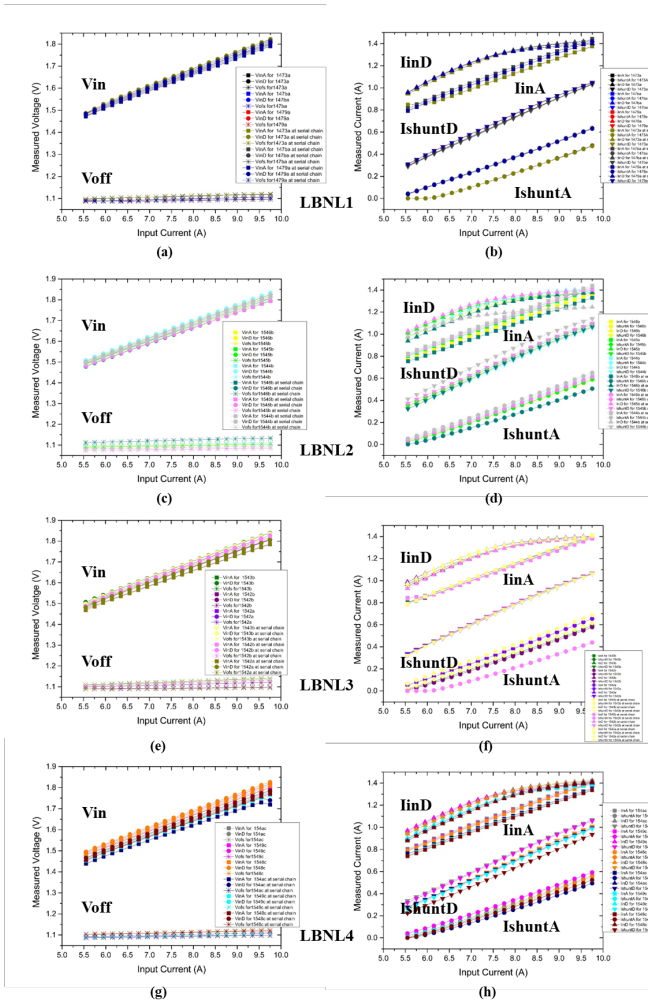

Figure 6: Front End input voltage vs module input current (a, c, e, and g) and Front End input currents vs module input current (b, d, f, and h)of the four triplet modules as a part of the serial power chain as well as an individual triplet.

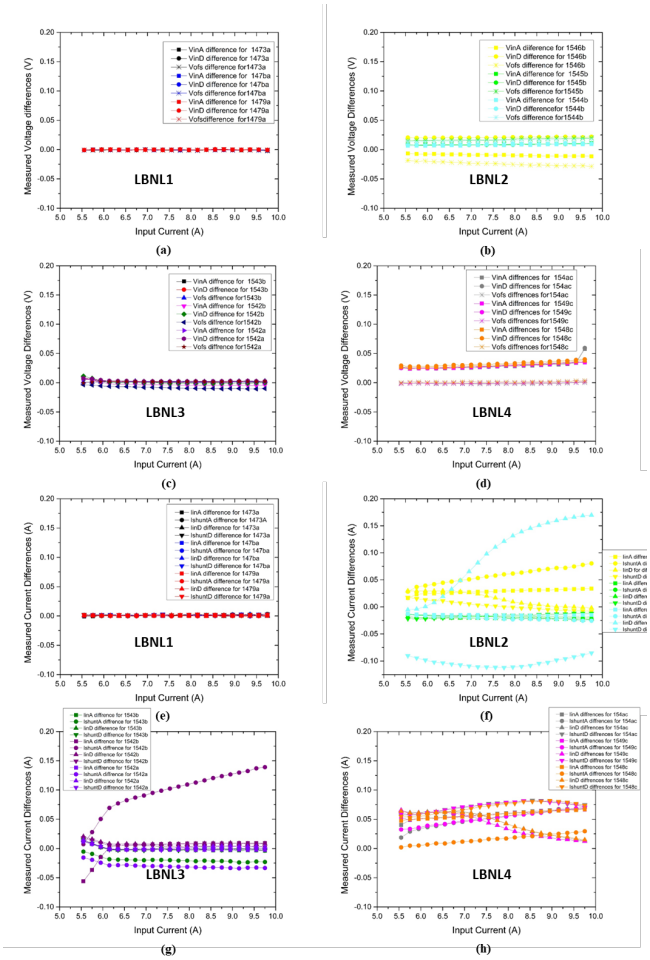

Figure 7: Differences of FE input voltage vs module input current (a, b, c, and d) and FE input currents vs module input current (e, f, g, and h)of the four triplet modules as a part of the serial power chain and as individual triplet.

serial power chains, as well as OVP characteristics. With these results, it can be concluded that the serial power chain can work as it was predicted. It is yet to be noted that this study was done before irradiation, a new study should be done after irradiation to predict the conditions after radiation defects.

Acknowledgments

References

[1] ATLAS collaboration, *Technical design report for the ATLAS inner tracker pixel detector CERN-LHCC-2017-021. ATLASTDR-030*

[2] Samy, Md AA, et al, *Characterization of FBK 3D pixel sensor modules based on RD53A readout chip for the ATLAS ITk Journal of Instrumentation 16.12 (2021): C12028*

[3] Chan, Jay. *Serial powering for ATLAS ITk pixel modules No. ATL-ITK-SLIDE-2022-674. ATL-COM-ITK-2022-131, 2023*

[4] Samy, M. A. A., et al. *Cold temperature characterization of ring triplets based on RD53A readout chip Journal of Instrumentation, 17.11 (2022): C11005*

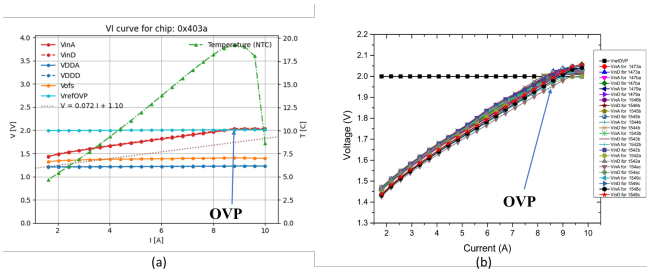

Figure 8: (a) FE input voltage vs module input current at Low Power (LP) mode for a single chip of an individual triplet and, (b) the same condition for all the chips as a part of the serial power chain. All of them get saturated around 9A current on 2 V, because of Over Voltage Protection (OVP) characteristics.