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An FPGA-based Front-end Module Emulator for the High Granularity Timing Detector*

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Abstract: This paper introduces an FPGA-based front-end module emulator developed for the High Granularity Timing Detector (HGTD) within the ATLAS experiment at LHC. The emulator serves as a stand-in for the HGTD readout module during the stage when the readout module is unavailable. Utilizing a Xilinx-Spartan 7 FPGA, the emulator simulates the digital functionalities of the ATLAS LGAD Timing Integrated Read-Out Chip used in the readout module. Notably, the emulator maintains identical overall dimensions and connectors as the readout module, ensuring seamless integration into the testing framework. The emulator's key advantage lies in its ability to act as a temporary replacement for the readout module during system tests, mitigating project delays caused by readout module unavailability. Furthermore, the emulator offers a cost-effective and adaptable means of verifying the digital logic design of ALTIROC before chip production. The successful application of the emulator within the HGTD project demonstrates its broader potential as a valuable tool in the realm of detector development and validation.

Keywords: Digital electronic circuits; Front-end electronics for detector readout; Timing detectors

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1 Introduction

The significant increase in pileup presents a major experimental challenge for the High Luminosity LHC [1] project's physics program. In response to this challenge, the High Granularity Timing Detector (HGTD) [2–4] is proposed as part of the ATLAS [5] Phase-II upgrade. The main aim of the HGTD is to effectively mitigate the detrimental impacts of pileup on object reconstruction by precisely measuring the time of tracks. Figure 1 shows the schematic of the HGTD electronics system. The HGTD is composed of 8032 front-end readout modules. Each readout module consists of two Low Gain Avalanche Detectors of approximately 2×2 cm^2 bump-bonded to two ATLAS LGAD Timing Integrated Read-Out Chips (ALTIROC) [6] and held together by a module flex (flexible PCB). Each module will be connected to the Peripheral Electronics Boards (PEB) through a flex tail (another flexible PCB). The connections between on-detector and off-detector electronics are performed via optical fibers, high/low voltage cables, interlock cables and monitoring signal cables. The time information of tracks is accurately measured, encoded, and structured within the readout module. The logical schematic depiction of ALTIROC is illustrated in Figure 2. ALTIROC integrates 225 channels to readout 15×15 sensor cells of 1.3×1.3 mm^2. The ASIC provides a timing measurement as well as a luminosity measurement (number of hits per Bunch Crossing). The data of each of the 15 columns are read out by a circuit located at the End Of Column (EOC). The periphery integrates the digital blocks for the readout, the data serializer and the analog common blocks. The resulting data traverses a flex tail and the PEB before being collected by the Data Acquisition system (DAQ). Simultaneously, the readout module handles the dual responsibilities of managing slow control information from the Detector Control System (DCS) and fast commands from the Time Trigger Control system (TTC).

The HGTD readout module is indispensable for testing both sub-systems and full system. However, due to the protracted nature of ASIC chip design and manufacturing, the readout modules remain elusive during the early stage of the project. In response, a front-end module emulator based on the Xilinx-Spartan 7 FPGA (XC7S15-2CPGA196C) is developed to alleviate the limitations imposed by the unavailability of readout modules in critical tests. In the subsequent sections, we delve into the emulator's design and its versatile applications.

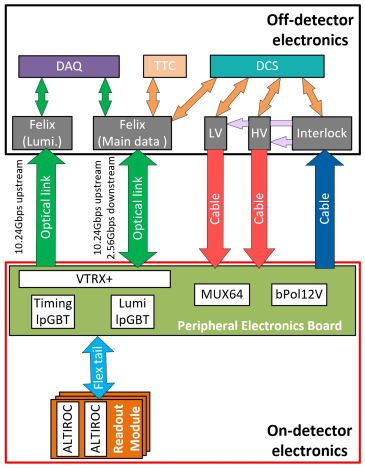

Figure 1. The schematic of the HGTD electronics system.

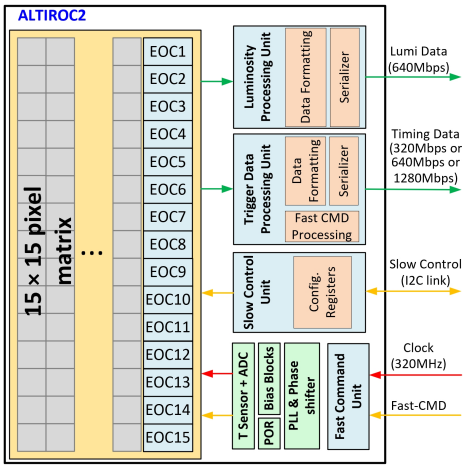

Figure 2. The schematic diagram of the HGTD readout module.

2 Hardware Design

The emulator meticulously adheres to the same physical dimensions, 2×4 cm^2, and connector type (FH26W) as the counterpart. This precision in design ensures that the emulator seamlessly conforms to the mechanical dimension prerequisites during installation. Detailed information regarding its dimension and electronic components arrangement can be found in Figure 3. Central to the emulator's functionality is the Xilinx-Spartan XC7S15-2CPGA196C FPGA. The FPGA is programmed to emulate the readout module through a JTAG interface with Xilinx JTAG-HS3 USB. A 16 MB NOR-FLASH memory is incorporated to securely store the configuration file and facilitate the emulator's operation. For debugging purpose, a crystal oscillator (XO) of 200 MHz is included. Additionally, a dial switch intended for hardware reset is included for effective control. Moreover, an NTC sensor is integrated into the design to enhance monitoring capabilities.

The amalgamation of these components forms the foundation of the emulator's hardware design, designed to effectively replicate the functions of the readout module.

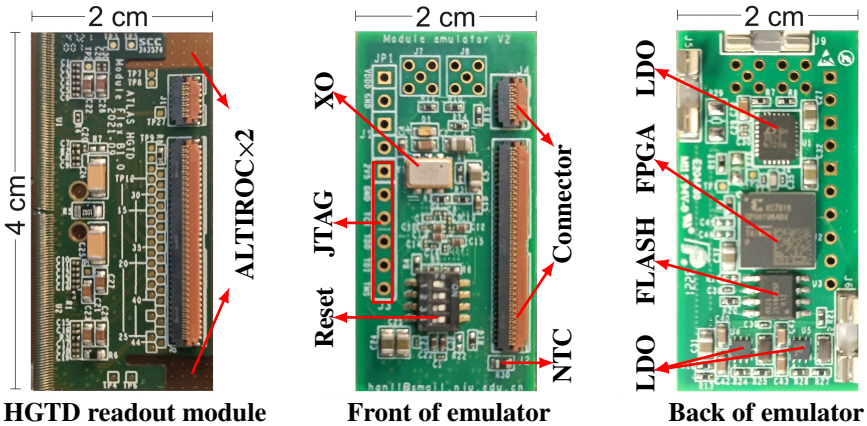

Figure 3. The dimensions of readout module and emulator as well as the electronic components layout of emulator.

3 Firmware Design

Based on the functionalities of the readout module, we devised a comprehensive firmware for the emulator. The logical architecture of this firmware is succinctly illustrated in Figure 4. The firmware translates the intricate digital functionalities of the readout module into four distinct logical functions:

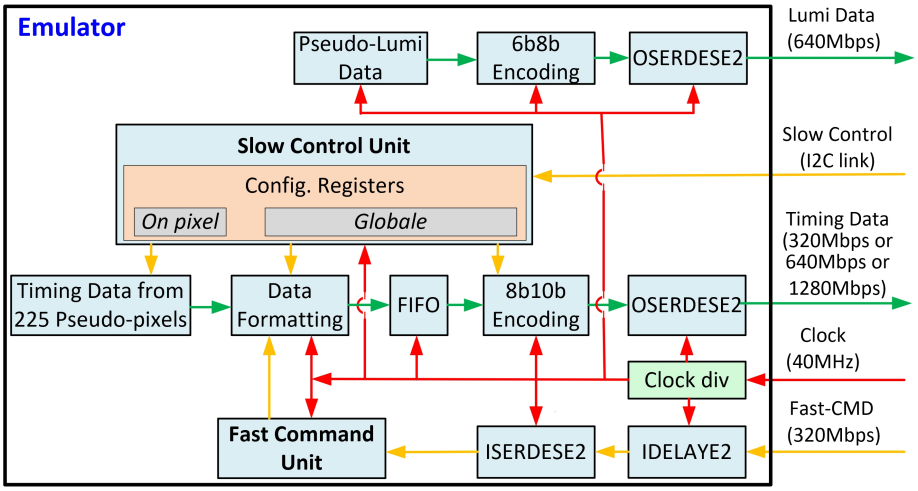

Figure 4. The logic schematic diagram of emulator.

a) **Clock generator:** The emulator harnesses the intellectual property resources of Xilinx to generate its requisite clocks. The primary clock source is a 40 MHz external signal from PEB, which mirrors the bunch crossing frequency of the LHC to ensure synchronization with the experimental environment.

b) **Slow control unit:** The logic code of this unit is directly transplanted from the ALTIROC design. The emulator's operational mode is determined by instantiating the corresponding registers both at the pixel level and global level. Reading from and writing to these registers are executed through I2C protocol.

c) **Fast command unit:** Responsible for receiving and deciphering fast commands dispatched by the TTC system, this unit is pivotal in acquiring trigger-related information for data acquisition. The majority of these commands consist of 8 bits transmitted sequentially at 320 Mbps, which results in one fast command reception per bunch crossing.

d) **Data formatting and encoding:** The FPGA is programmatically tailored to generate pseudo-data for 225 pixels, aligning with the readout module's data generation process. The data frame mirrors that of the readout module. The data frame's length dynamically adjusts according to slow control information. Upon receipt of a trigger, a data package is dispatched to a FIFO buffer. Subsequently, the readout frequency from the FIFO varies based on the configurations of the slow control registers. To maintain DC balance, the data undergoes encoding via an 8b10b encoder. Finally, the data is transmitted to the DAQ system in a serialized format at speeds of 320/640/1280 Mbps, adapting to diverse operational needs.

The firmware enables the emulator to emulate the essential features of the readout module, ensuring its effective integration into the HGTD project's testing and validation framework.

4 Application of Emulator

The minimum demonstrator system [7] for the HGTD is depicted in Figure 5. It is designed with full features of the HGTD to enable the systematic validation of individual sub-system functionalities, followed by comprehensive verification at the full system level. The emulators establish connectivity with modular PEB through flex tails. The modular PEB facilitate data exchange between the emulators and the DAQ/DCS/TTC systems. The DAQ/DCS/TTC functions are realized through a dedicated card, termed FELIX, which serves as a detector readout component designed by CERN. The emulator assumes a pivotal role in expediting system debugging processes and validating the digital logic design of the readout module.

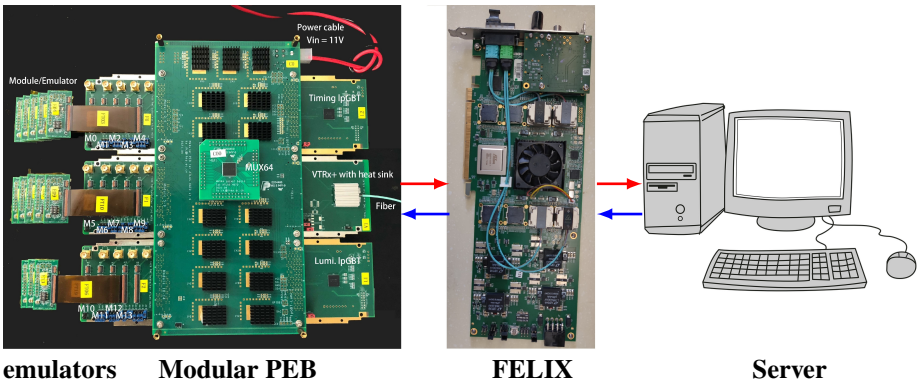

Figure 5. The minimum demonstrate system for the HGTD.

a) **Sub-system debugging facilitated by the emulator:** Debugging sub-systems without the readout module poses challenges, particularly for systems reliant on the readout module as a transceiver. This issue is addressed within the HGTD project. However, the emulator offers a salient solution by serving as a surrogate that aids in the comprehensive debugging of these sub-systems.

- Bit error rate test (BERT): The transmission of timing data from the readout module to the DAQ system transpires via a complex path comprising a flex tail, PEB, and optical fibers spanning tens of meters. The optical fiber can support data rates of up to 10.24 Gbps. To mitigate bit errors, configurable registers related to pre-emphasis are integrated into the design. To determine the optimal values of these registers, we perform optical eye diagram scans for various register configurations using the emulator output as a data source. Figure 6 shows an optical eye diagram with good opening widths, corresponding to a proper slow control configurations.
- DAQ test: The readout module packages and encodes timing data, with the DAQ system subsequently responsible for decoding and identifying the received data package. We assess this functionality using the emulator when the readout module is not accessible.

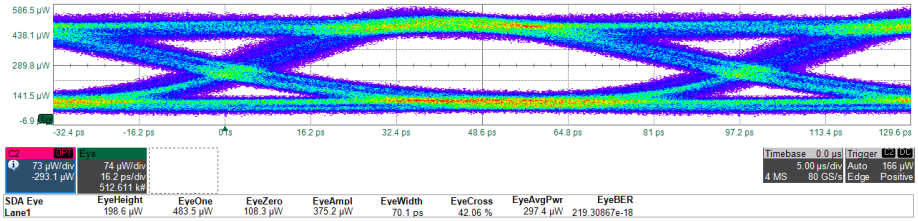

Figure 6. The optical eye diagram with good open width for timing data at 10.24 Gbps.

- Fast command test: The TTC system is responsible for sending fast commands to the readout module, providing trigger information for data acquisition. Within the emulator's framework, a dedicated fast command decoding unit is orchestrated to test and validate the functionality of the TTC system.
- ADC calibration: The calibration of Analog-to-Digital Converters (ADCs) assumes prominence in monitoring the temperature and voltage of the HGTD. This crucial task is entrusted to the Low Power Giga Bit Transceiver (lpGBT) ASIC, positioned on the PEB. Calibration of the ADC is effectively executed using the NTC sensor located on the emulator.

b) **Verification of readout module digital logic design:** A new logic design for the slow control unit is incorporated during an ALTIROC update. To validate this new design, we seamlessly transplant the corresponding code to the emulator, subsequently conducting testing within the demonstrator system. Through these tests, we verify that the new logic design works as expected.

c) **Full system debugging with emulator substitution:** The emulator instantiates key registers within the slow control unit, enabling the simulation of diverse responses to varying configurations of slow control. In full system tests, the emulator replicates the output characteristics of the readout module, encompassing data rate, encoding mode, and threshold discrimination across 225 pixels. Figure 7 shows threshold scans of these pixels sourced from emulator.

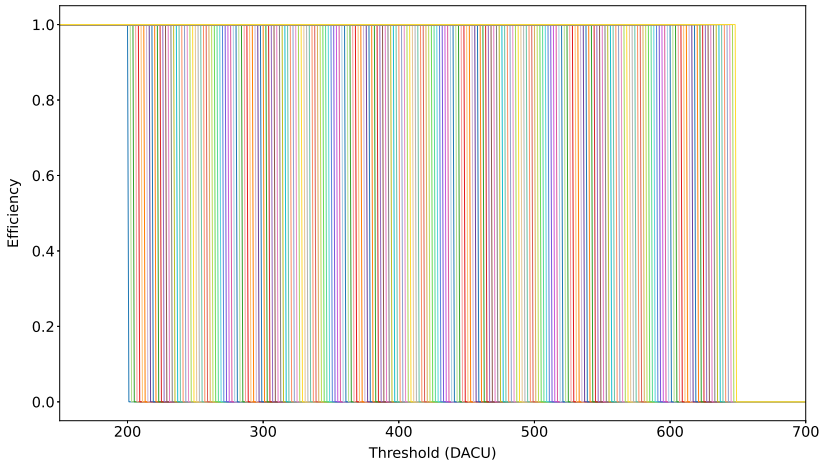

Figure 7. The S-curve scanning for 225 pseudo-pixels of emulator.

5 Summary

In this paper, we introduce an FPGA-based front-end module emulator tailored for the HGTD project in the ATLAS experiment at LHC. This emulator serves as a surrogate solution, effectively mimicking the functionality of the HGTD readout module during the project's initial design stage. Leveraging the capabilities of a Xilinx-Spartan 7 FPGA (XC7S15-2CPGA196C), the emulator adeptly replicates the intricate digital operations of the readout module. Its important role becomes evident in its capacity to temporarily replace the readout module during crucial system tests, thus preempting potential project delays attributed to readout module unavailability. Moreover, the emulator offers an economical and versatile avenue to validate the digital logic design of ALTIROC before venturing into chip production. The emulator's role extends beyond project-specific applications, highlighting its potential as a versatile tool for detector development and validation. This approach, as demonstrated by the HGTD project, could potentially find application in other experimental setups, fostering rapid progress and efficient validation in the realm of high-energy physics and beyond.

Acknowledgments

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