System-on-Chip Interest Group

Summary of the System-on-Module Survey

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Abstract

This report presents the outcome analysis from the System-on-Module survey taken during April and May 2022 among the members of the System-on-Chip interest group.

Replies to the System-on-Module Survey

No.	Respondent	Experiment/Project
1	L. Ardila	CMS/OT-DTC, CMS/L1T, CMS/HGC, CMS/MTD, CMS/BRIL
2	I. Bestintzanos	CMS/Barrel Muon Trigger Layer 1
3	A. Byszuk	CERN SY-EPC-CCE section, FGC4 project
4	A. Cicuttin	AMBER
5	G. Daniluk	CERN Distributed I/O Tier (HL-LHC WP18)
6	A. D. Tinoco Mendes	CMS/HGCAL test systems
7	R. Ferraro	CHARM
8	T. Gorski	CMS/APx
9	S. Haas	ATLAS/L1CT
10	H. Boukabache	CROME
11	H. Boukabache	CERN SGM (Site Gate Monitors)
12	M. Haranko	CMS/BRIL
13	E. Hazen	ATLAS/MDTTP and CMS/IT-DTC and CMS/OT-TF
14	J. D. Hobbs	ATLAS/LAr
15	M. Krupa	CERN HL-LHC IR1/IR5 Beam Position Monitors
16	M. Lipinski	CERN White Rabbit Switch v4
17	N. Loukas	CMS/BCP: CMS/EB, CMS/HB, CMS/HF, CMS/HO, possibly others like CMS ZDC and BHM
18	A. Madorsky	CMS/X2O
19	F. Meijers	CMS/Central DAQ for the DTH (DAQ and Timing Hub)
20	T. Mkrtchyan	ATLAS/L1Calo TREX
21	M. Gololo	ATLAS/TileCal Phase-II Upgrade
22	Y. Okumura	ATLAS/L0Muon Endcap
23	H. Sandberg	CERN SY-BI-XEI (Beam Instrumentation Group)
24	S. Schlenker	EMP, ATLAS/DCS
25	U. Schaefer	ATLAS/fFEX
26	S. Tang	ATLAS/Global Trigger

Contents

1 Introduction

The rise of System-on-Chip (SoC) usage at CERN throughout experiments, accelerators and equipment groups has clearly been outlined during two dedicated workshops held on June 2019, https://indico.cern.ch/event/799275, and June 2021, https://indico.cern.ch/event/996093. It was foreseen to reach 1500 SoCs for ATLAS and CMS for Run 4 and more than 675 SoCs for accelerators control and safety systems. The hardware integration of SoC into electronics boards is often complex and challenging. There is moreover limited added value to develop custom modules containing a SoC. Using off-the-shelf System on Modules (SoM), that package all the SoC functions, peripherals and management circuits into single boards, is an easy-to-use solution. Although, they significantly accelerate design speed and minimize development cost, one should consider several factors when selecting a SoM. Various fundamental factors shall be considered such as specifications, scalability, flexibility. In this frame, the SoC interest group committee launched a survey in April 2022 to evaluate the needs of CERN community. A study analysing the future usage of SoM at CERN was subsequently performed based on the responses of 26 teams throughout the organisation. The study was built above three pillars:

- Strategic criteria to select a SoM

- Technical requirements for SoM selection

- Limiting factors with SoM adoption

This study highlights common requirements and will pave the way for increased synergies between CERN groups and experiments.

2 General questions on the use of SoM

2.1 General questions concerning the type of SoM

2.1.1 Use or plan to use a SoM

Question 1.1.1: Are you using/planning to use a SoM?

Overall 26 projects at CERN participated in the SoM survey: 8 CMS projects, 9 ATLAS projects and 9 other projects from different departments at CERN. The majority (21) have indicated their plan to use a SoM, whereas the rest are planing to use SoCs without a mezzanine due to different reasons: some due to the number of I/Os their project requires that is higher than nowadays SoMs can support, or their specific design is not compatible with a SoM. Others have also indicated their desire to use the Xilinx Versal SoCs or even their own mezzanine design. There was also a mentioning of the extra costs by some of the projects.
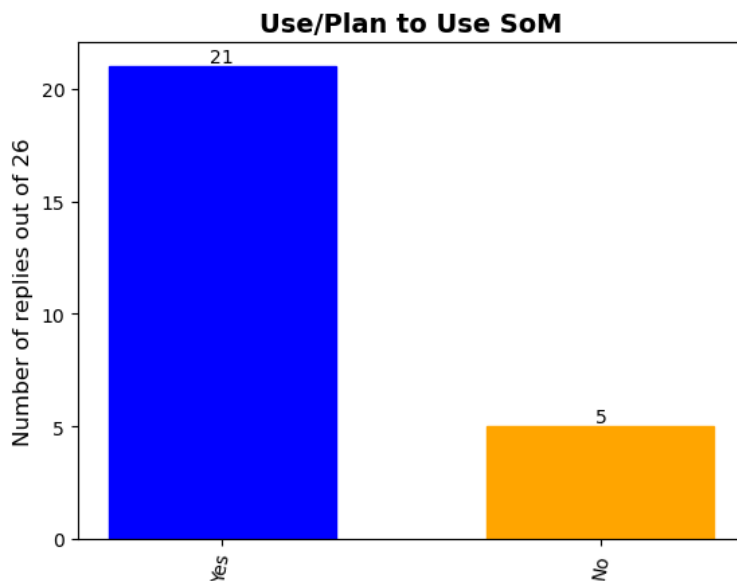

Figure 1: Replies to question 1.1.1 - Are you using/planning to use a SoM?
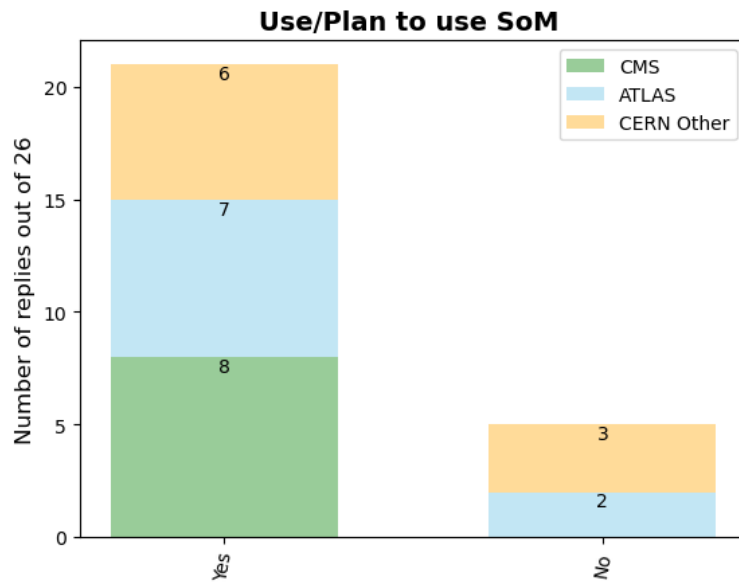
Figure 2: Replies to question 1.1.1 by project - Are you using/planning to use a SoM

2.1.2 Projected schedule for the use if the SoM

Question 1.1.2: What is your projected schedule for the use of the SoM?
(E.g. already using, Phase-I upgrade, or Phase-II upgrade)
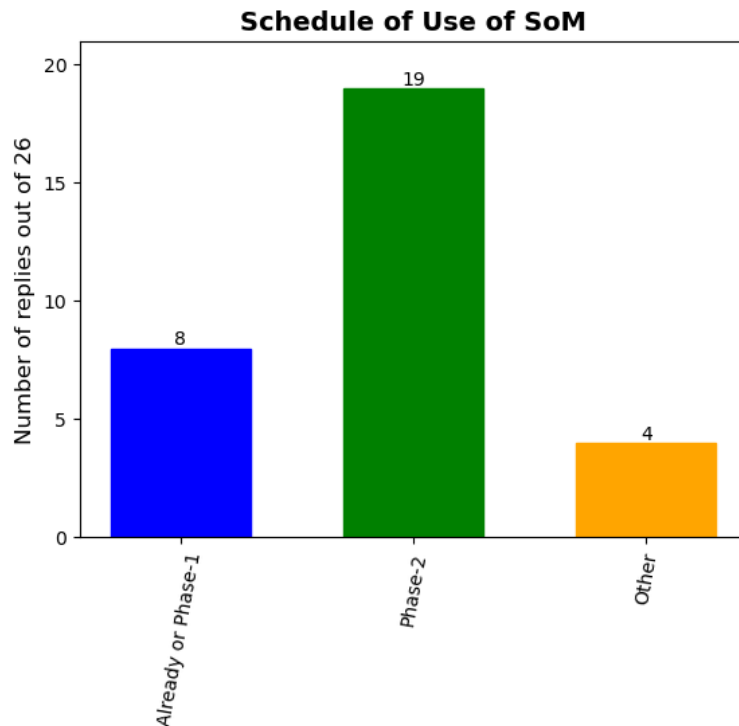
Figure 3: Replies to question 1.1.2 - What is your projected schedule for the use of the SoM?

Figure 4: Replies to question 1.1.2 by project - What is you projected schedule for the use of SoM?

The usage of SoMs had been indicated to already take place now (Phase-I) by 30% of the projects, whereas the majority are targeting its usage for Phase-II.

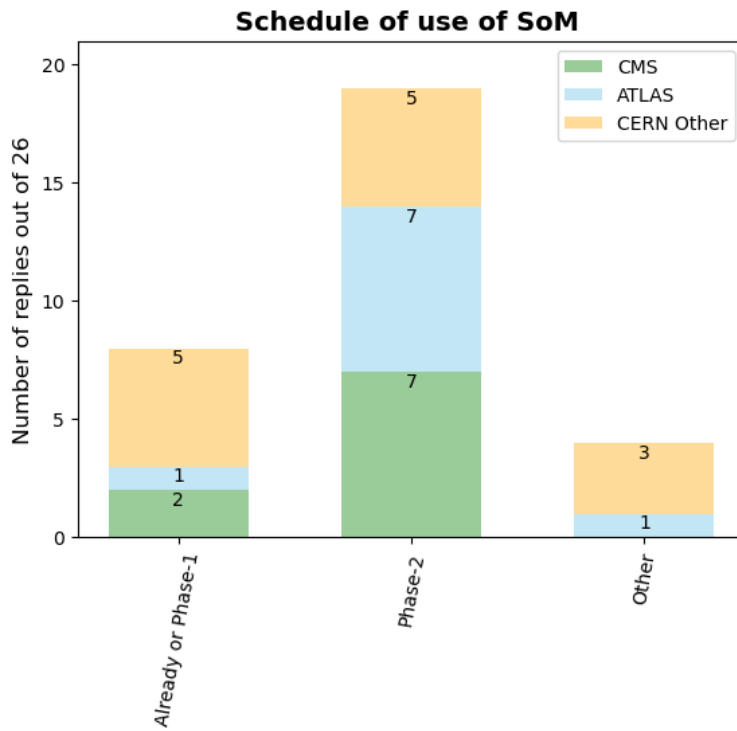### 2.1.3 Number of SoMs

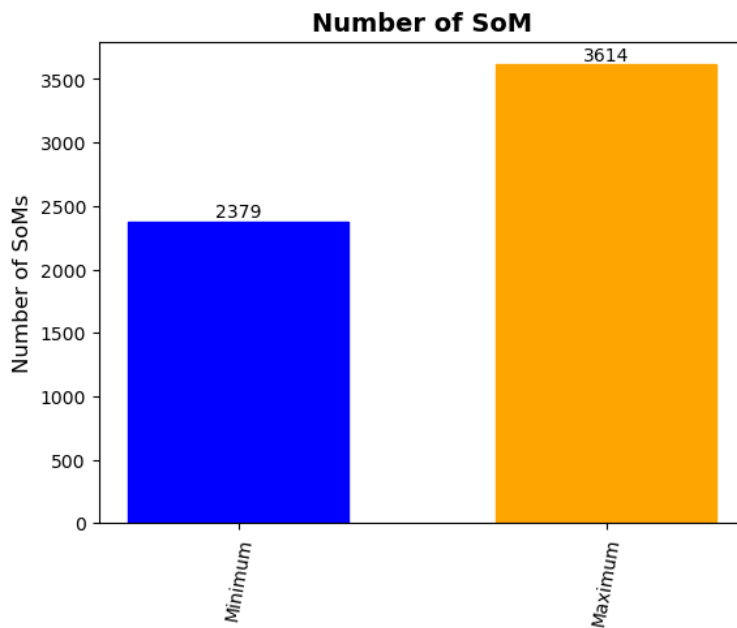Question 1.1.3: How many SoM are you using/will you use?

Figure 5: Replies to question 1.1.3 - How many SoM are you using/will you use?
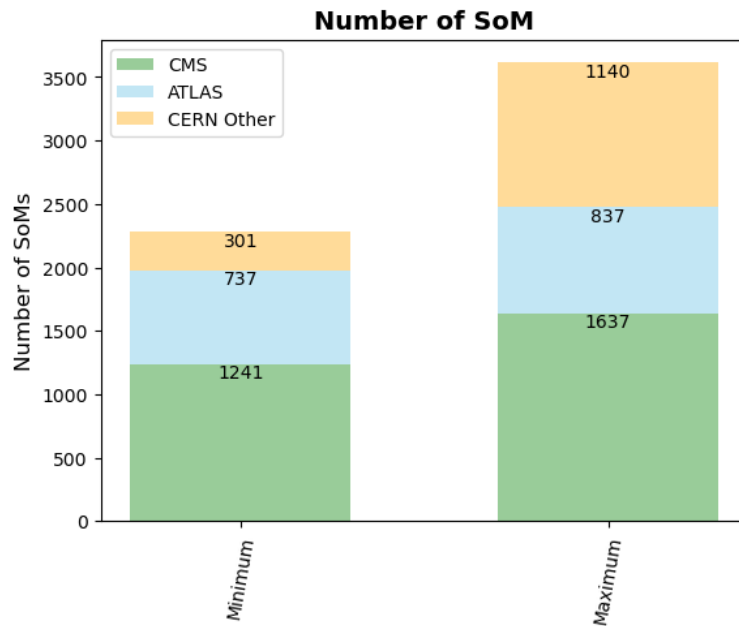
Figure 6: Replies to question 1.1.3 by project - How many SoM are you using/will you use?

All in all, based on the survey replies, we are looking at between 2.4k to 3.7k SoMs to be used at CERN by the different projects, with 50% of the overall SoMs are foreseen to be used by CMS, 25% by ATLAS and 25% by other projects.

Over the past few years the numbers of SoCs/SoMs had kept changing in general but also with respect to each of the CERN experiments or departments. It would be interesting to follow the evolution of the numbers and factors considered in the coming years.

2.1.4 Type of SoMs

> Question 1.1.4: Which SoM are you using/will you use?
> (Are you using Enclustra, Trenz, Xilinx Kria, or your own home built one?)

Out of the available SoMs in the market, there was no indication for a 'favorite' SoM vendor. From the projects, which had converged on their decision (as we know today), either Kria, Trenz or Enclustra were more or less evenly indicated. However close to 40% are either still exploring the available options or are planing for a custom made solution. We have the impression that the choice was largely determined by the availability of the products at the time of evaluation.
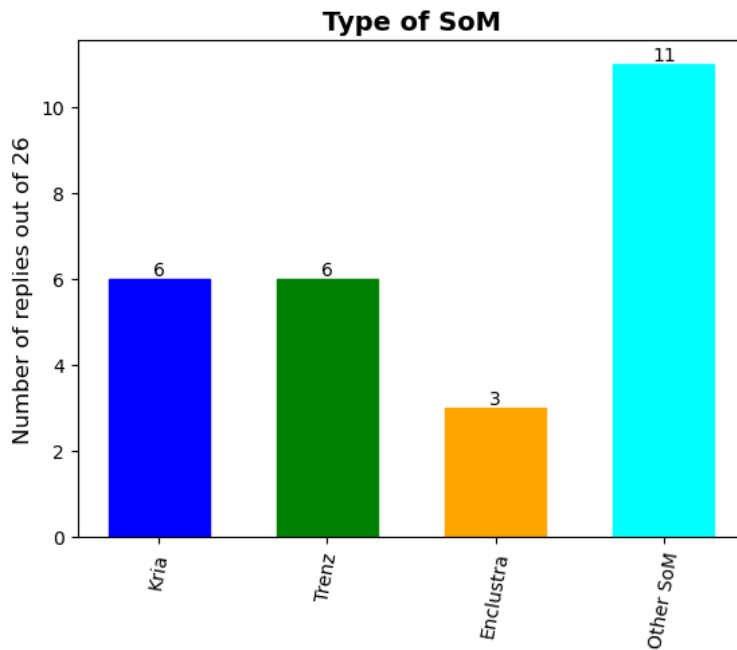
Figure 7: Replies to question 1.1.4 - Which SoM are you using/will you use?
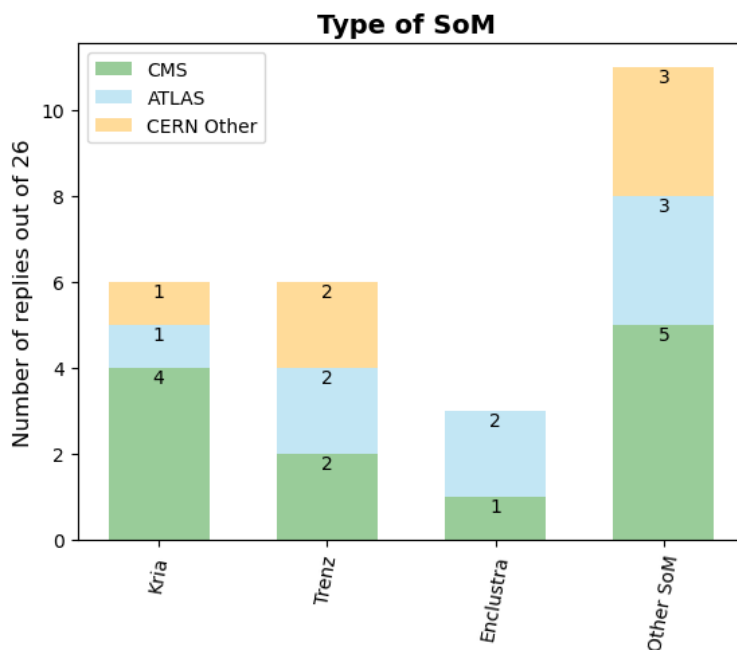
Figure 8: Replies to question 1.1.4 by project - Which SoM are you using/will you use?

2.1.5 Alternative SoM Manufacturers

Question 1.1.5: Are there other SoM manufacturers you have heard of?
('Exotic' designs are also interesting to learn about: please add a reference.)

Exotic flavors of SoM manufactures have also been looked at by our community, typically for small lab and test-beam setups. There was mentioning of the following:

- Embedded Linux Mezzanine from University of Wisconsin-Madison, https://indico.cern.ch/event/996093/contributions/4376629/attachments/2260579/3836837/20210609_SoC_Workshop_2021.pdf

- Miami Zynq from TOPIC Embbedded Systems, https://topic.nl/en/products/system-on-modules/miami-zynq

- Products from MyIR Tech Systems, http://www.myirtech.com/default.asp

- Products from iWave Systems, https://www.iwavesystems.com/product-category/soms-sbcs

- Products from ALDEC, https://www.aldec.com/en/products/emulation/hes_fpga_boards/virtex_ultrascale_plus/hes_xcvu9p_zu7ev

- Ultrazed-EV SoM from AVNET, https://www.avnet.com/wps/portal/us/products/avnet-boards/avnet-board-families/ultrazed/ultrazed-ev

2.1.6   SoM vs SoC

> Question 1.1.6: If you are not using a SoM, are you planning to use a SoC directly on your module? And if so, what are your reasons?

The main points of conclusion were the following:

- Either planning to use Xilinx Versal, or their own design board

- The number of I/Os on SoM is limited/too-small (MGTs, 25 Gbps)

- Specific design of the board clashes with SoM compatibility

- Extra costs of using a SoM

2.2   Selection of SoM

2.2.1   Reasons for selection of SoM

> Question 1.2.1: Why did you choose/are you planning to choose that particular type of SoM? Please answer the questions in section 2, "Criteria for the selection of SoM".

A single reply: Kria for price and availability. Other, more detailed replies are analysed in Section 3.

2.2.2   Criteria for choice of SoM

> Question 1.2.2: Which are for you the most important criteria to decide which type of SoM to choose?

There was a wide range of answers, which required some interpretation in order to group them. From the answers received it can be guessed that if there had been "multiple choice", most respondents would probably have selected most of the choices. It is nevertheless interesting to see what was the first thing that came to the mind of the respondents. According to the replies, the criteria were grouped into technical and other, i.e. non-technical, criteria.

Among the technical criteria the MGTs (shown in blue in Figure 9) were the most important ones, followed by CPU processing power, logic resources, and other low and high-speed IOs in equal importance. Those were followed by additional technical features on the SoM, like the presence of an SD card or a jitter cleaner on the SoM. The last criterion mentioned was the memory of the PL and the PS part of the SoC on the SoM.

Among the non-technical criteria for the choice of the SoM (shown in green in Figure 9) the most important one was the previous experience of the group with a similar system. This was followed by the cost of the SoM. The came the ease of the design, e.g. the availability of an example design, help with the resources, and the tools, the support, and the reliability. The size of the SoM was mentioned by two groups, and the availability of the SoM and the power consumption were mentioned once each.
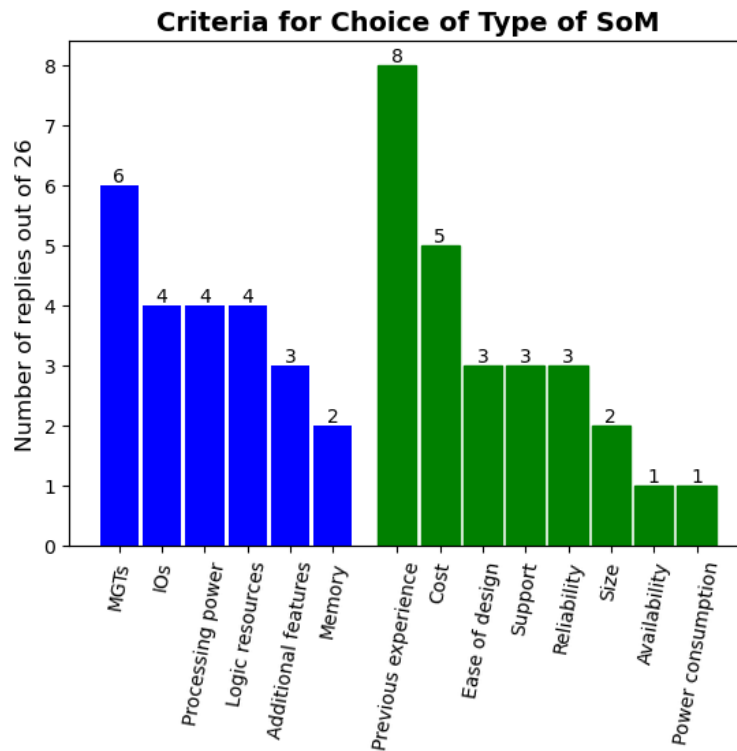
Figure 9: Replies to question 1.2.2 - Which are for you the most important criteria to decide which type of SoM to choose?

2.2.3 Reasons for change of SoM

> Question 1.2.3: Had you already used a SoM before, and have you moved to a different one? If so, why did you move?

It can be said that the question 1.2.3 was rather complex, being made up from two conditions (having had a SoM before, and having changed the type of SoM), as well as asking for the reasons of such a change. In any case, only nine out of the 26 returned surveys, had replies for this question. The replies can be grouped into technical reasons, and other, i.e. non-technical, reasons.

Among the technical reasons (shown in blue in Figure 10) the most important one was more and/or better IO, closely followed by better CPU performance; it has to be said that one of the replies referred to a project which previously had used soft-core processors. Other reasons for a change included more logic resources, performance (generally, without specifying specific aspects), and the availability of a clock chip.

Among the other, non-technical, reasons (shown in green in Figure 10) equally mentioned were upgradability, in terms of better standardisation of the connector definition, availability of the SoM, cost of the SoM, and availability of documentation. One reply was for a design that specifically required the SoM to be adapted to radiation testing.
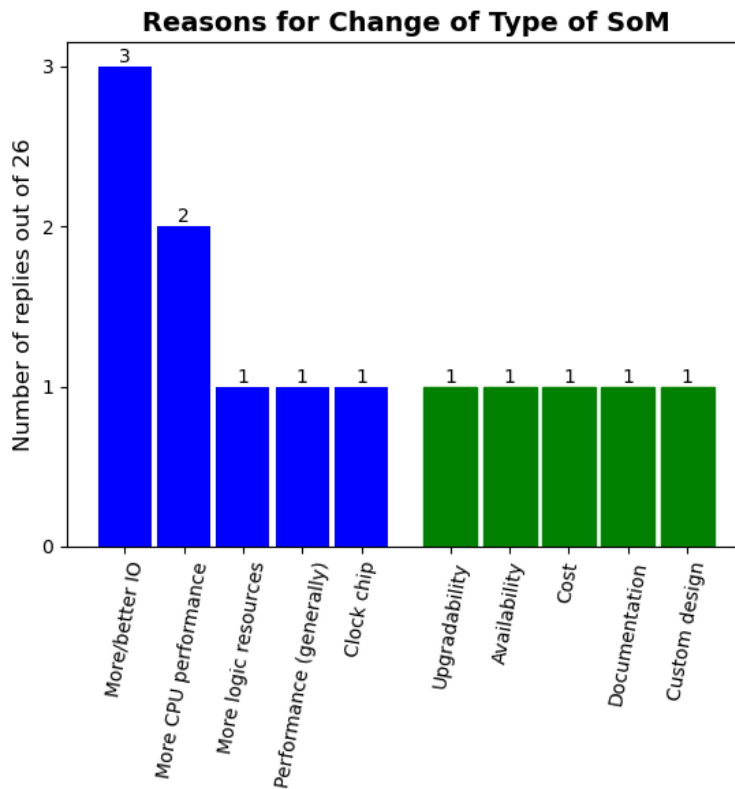
Figure 10: Replies to question 1.2.3 - Had you already used a SoM before, and have you moved to a different one? If so, why did you move?

2.2.4 Change of SoM after SoC workshop

Question 1.2.4: Have you changed your choice of SoM following the SoC workshop? If so, what were the choices old vs new? What was the main motivation for the change?

There was only one 'Yes' to this question, which came from project number 1: 'Currently using custom-built module, moving to Xilinx Kria for next revision of the board'.
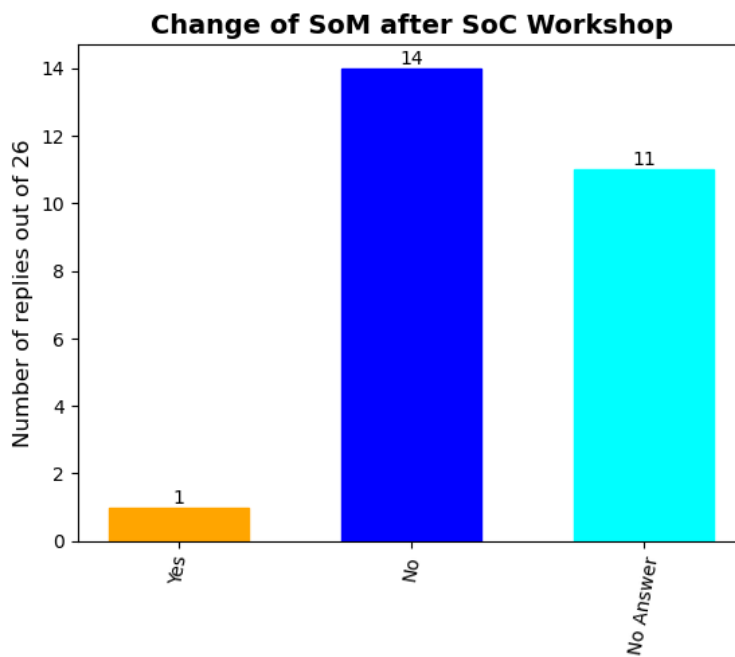

Figure 11: Replies to question 1.2.4 - Have you changed your choice of SoM following the SoC workshop?

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3 Technical criteria for selection of SoM

3.1 Use of SoM

3.1.1 Use of SoM

> Question 2.1.1: What is the expected usage of the SoM, e.g. hardware control/monitoring, run control application, event/trigger data processing/readout/monitoring?

The interpretation of the replies was not always straightforward, e.g. definitions of hardware, detector, and run control are overlapping. The replies were grouped into traditional "slow-control" and "run control" usage.

In the first group (shown in blue in Figure 12) the most frequent answer was hardware control/monitoring, followed by two replies explicitly mention supervisory control, where the SoM is used to control other equipment. One reply was for the use of the SoM as an Intelligent Platform Management Controller (IPMC) on Advanced Telecommunication Computing Architecture (ATCA) boards.

In the second group (shown in green in Figure 12) the most frequent answers were run control and data monitoring, closely followed by data readout. A smaller number was for data processing, and two replies indicated the use of the SoM for detector module calibration.

Apart from those two groups of answers, there was one very different answer for a project (shown in orange in Figure 12), which uses the SoM for analog signal acquisition.
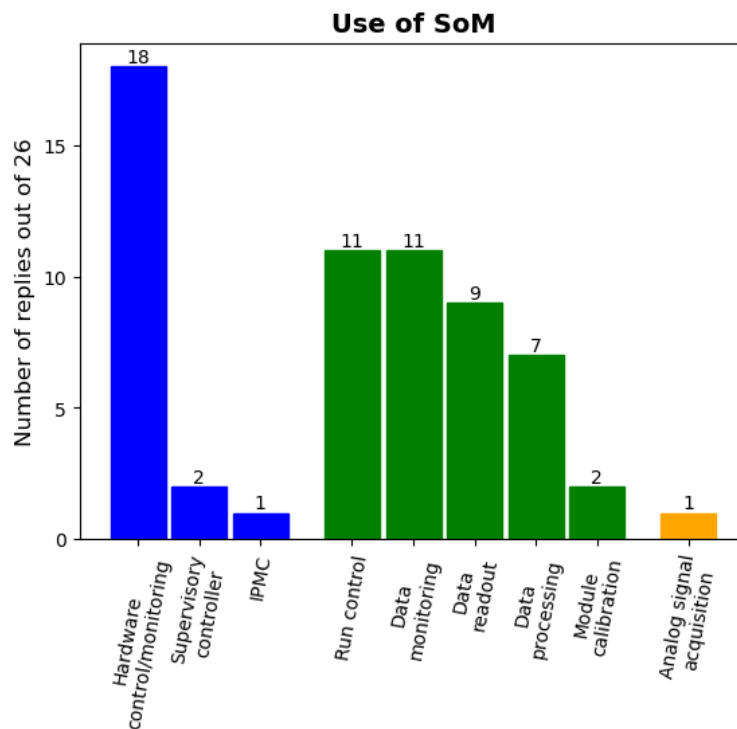

Figure 12: Replies to Question 2.1.1 - What is the expected usage of the SoM?

3.1.2 Use of PL

> Question 2.1.2: Are you using the programmable logic and/or the processor system in the data path, e.g. for trigger or readout?

The plans for the use of the PL were not always very clear: five replies were "Yes" without specifying what they want to use the PL for. Replying "No" or "at least for the time being" were ten out of 26. In total, 16 out of 26 use or plan to use the PL. The different uses were mostly for data collection/readout/monitoring (shown in blue in Figure 13). One reply was explicitly for trigger input and output (shown in green in Figure 13). And one for ADC and DAC/PWM (shown in orange in Figure 13). Other replies were for the 10 GbE, for safety critical applications, e.g. triplication of logic, and for providing an interface to the detector (shown in cyan in Figure 13).
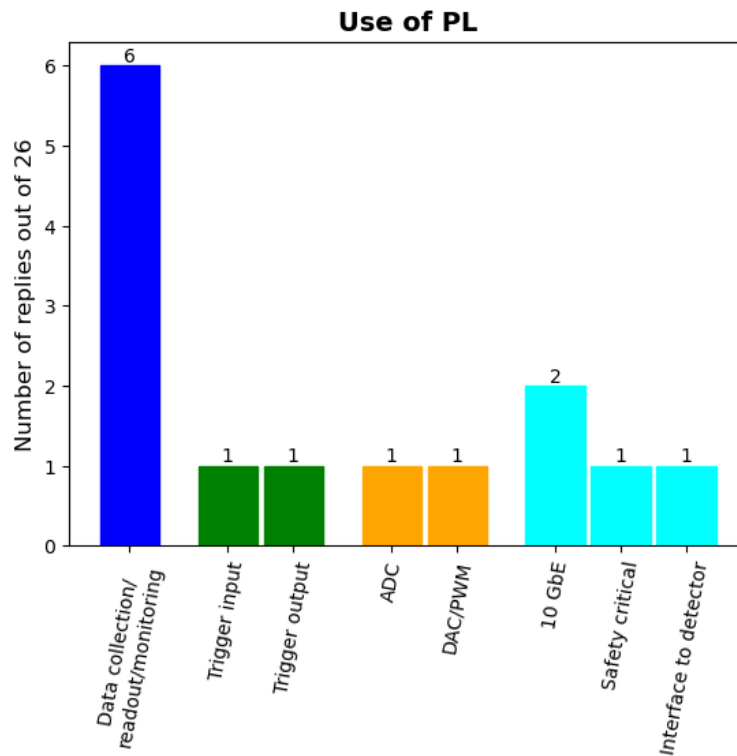
Figure 13: Replies to question 2.1.2 - Are you using the programmable logic and/or the processor system in the data path?

3.2 Challenges/issues expected

> Question 2.1.3: Are you expecting any particular challenges? Or do you foresee issues with the SoM for its intended usage?

The most frequent answer (shown in blue in Figure 14) was for the procurement, in particular, the long lead times.The concerns raised about software aspects of the use of the SoM (shown in green in Figure 14) were on the complexity of the SoC, the long-term support, the difficulties in migrating from one version to the next, as well as on missing user hooks in PetaLinux software, and one concern about excessive software growth. The more technical concerns (shown in orange in Figure 14) were on the PS processing power, the IO link speed, and the heat dissipation of the SoM.

It should also be mentioned that eleven replies did not see any issues or did not know about any issues at all.
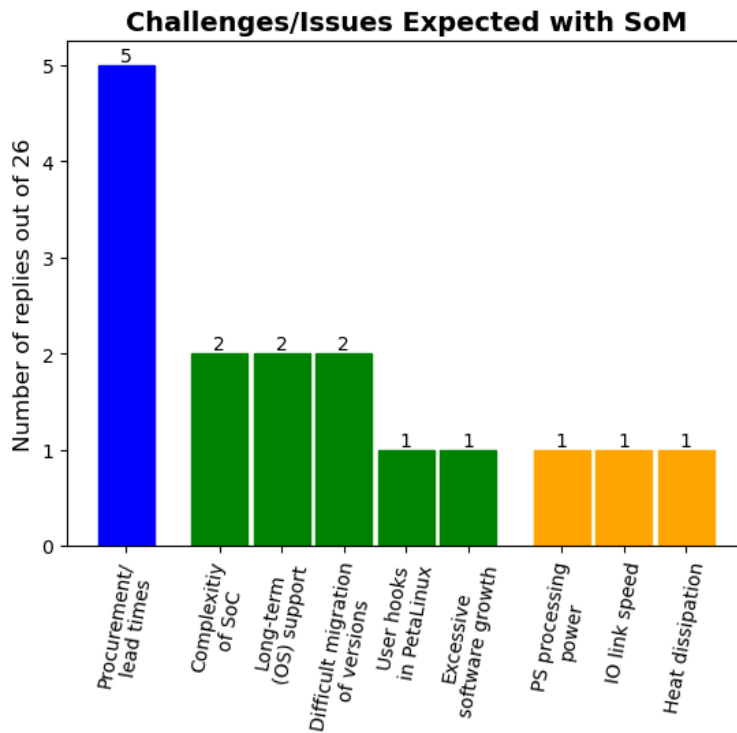
Figure 14: Replies to question 2.1.3 - Are you expecting any particular challenges?

3.3 Choice of SoC

3.3.1 Choice of SoC

Question 2.2.1: What SoC do you chose for your SoM? Xilinx Zynq, ZynqMP, Versal? Altera? Others?

Except from one custom design, all projects are using or planning to use SoMs with Xilinx SoCs. Most of those projects are using the Xilinx Zynq Ultrascale+ MPSoC. A smaller number of projects are using either the previous generation, Xilinx Zynq, or Xilinx RFSoC, or the next generation, Xilinx Versal.
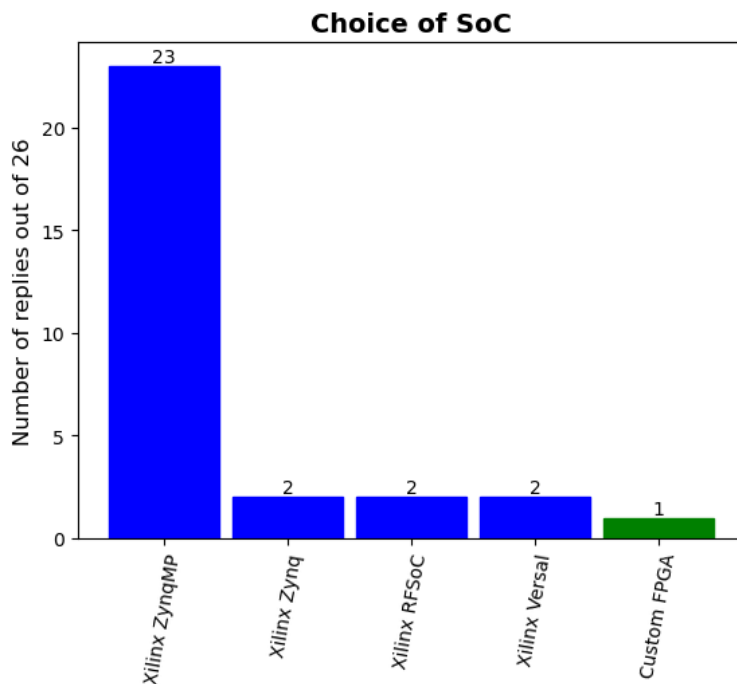

Figure 15: Replies to question 2.2.1 - What SoC do you chose for your SoM?

3.3.2 Reasons for choice of SoC

Question 2.2.2: Can you elaborate why specifically that type?

The most frequent answer for the choice of SoC was prior experience with hardware or knowledge of the tools. The architecture was the second most frequent answer, including one specific application for analog signal acquisition. This was followed by the performance, generally and with respect to cost. Then came the number and type of IO, i.e. transceivers, links, 10 GbE etc. After that came the support, i.e. technical support, widespread use implying a community, availability of tools, and the use of a common operating system. The less frequent reason for the choice of SoC was the availability of existing hardware.
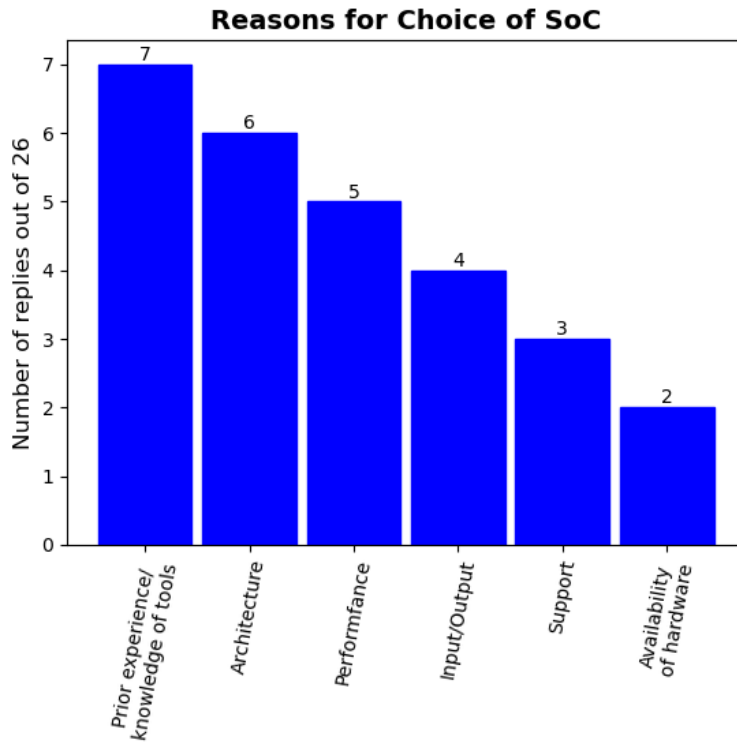
Figure 16: Replies to question 2.2.2 - Can you elaborate why specifically that type?

3.4 Multi-gigabit links

3.4.1 Number of multi-gigabit links

Question 2.3.1: How many MGTs for you foresee?
        (0 is a valid answer)

It is quite difficult to find a common need in term of MGTs numbers. Although, a quarter of the respondents are needing 4 MGT; most of the others are needing a specific number that can jump up to 72!
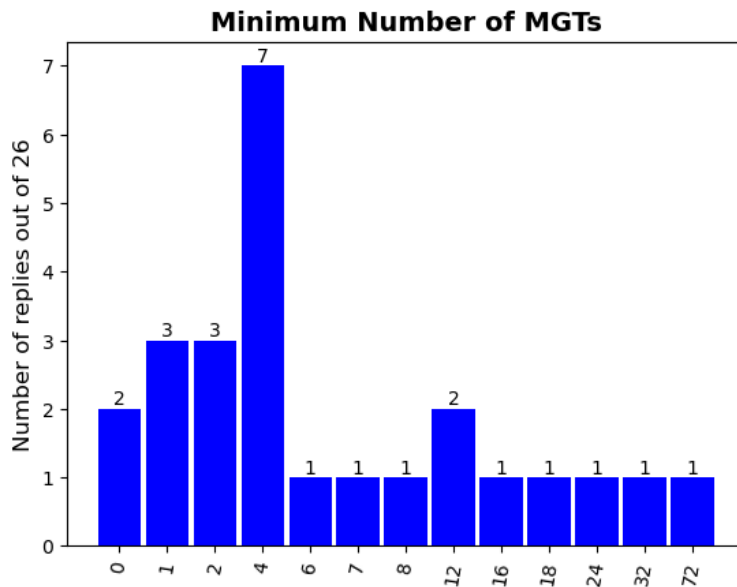
Minimum Number of MGTs

Figure 17: Replies to question 2.3.1 - How many MGTs for you foresee?

3.4.2 Types of multi-gigabit links

Question 2.3.2: Do you require specific types of MGTs? And if so, what are your reasons?

Almost half of the respondents need GTH MGT with a speed limit going from 13.1 Gb/s for the Xilinx Zynq 7000 series to 16.3 Gb/s for the UltraScale and UltraScale+ series. There are 3 outliers needing either GTX or GTP. The classification of the MGT links was done based on the table of Appendix A.
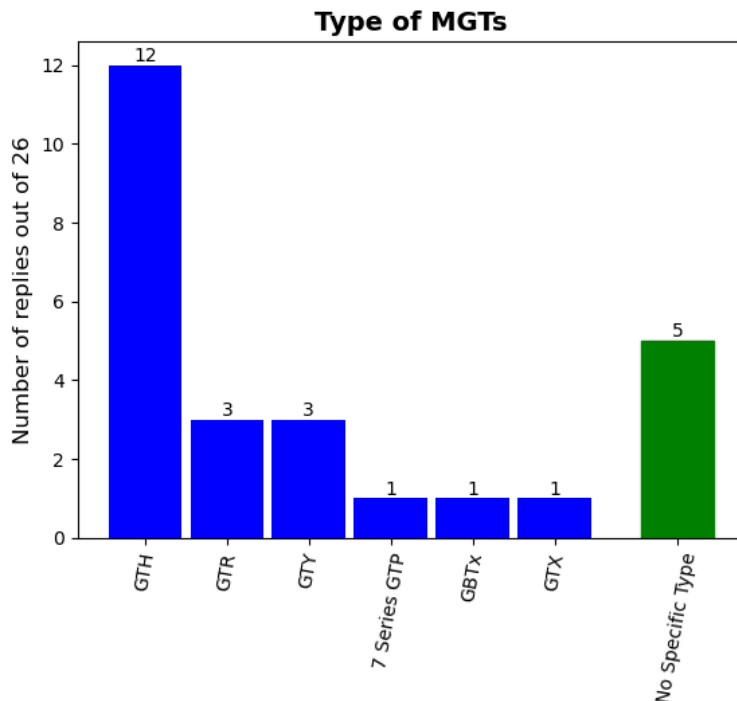

Type of MGTs

Figure 18: Replies to question 2.3.2 by type of MGT - Do you require specific types of MGTs?

The final applications are quite diverse:

- SSD Communication

- Ethernet

- Connect to lpGBT chips

- FPGA-SoC communication

- White Rabbit protocol

- Others, e.g. USB, DisplayPort, etc.

- Aurora protocol

- Test under radiation

- Video Processing
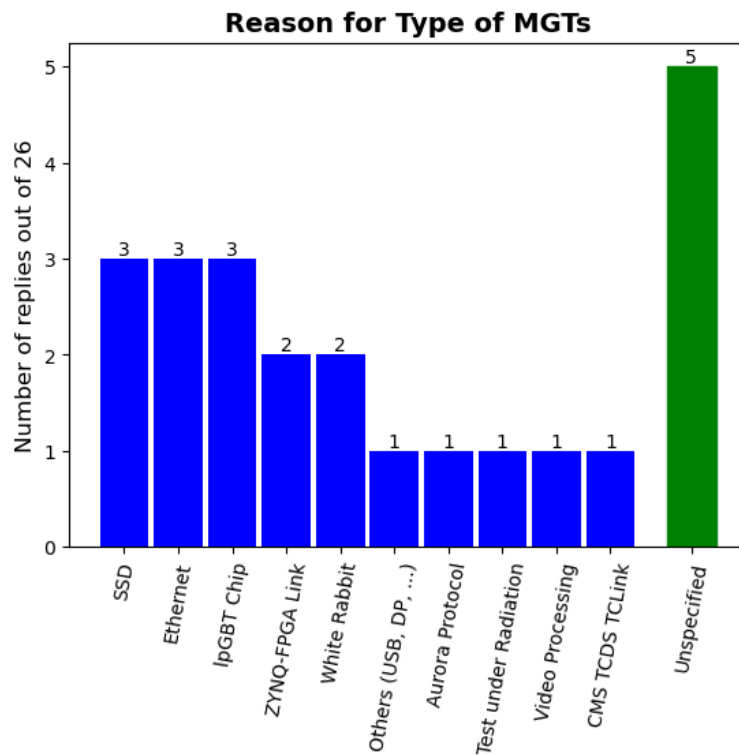
- CMS TCDS TCLink

Figure 19: Replies to question 2.3.2 by use of MGT - Do you require specific types of MGTs?

3.5 Other input/output

3.5.1 Number of GPIOs

Question 2.4.1: How many GPIOs do you foresee?

Pretty clear answers with high certainty. In a few cases it was not clear whether the respondent included the standard bus IO (UART, I2C etc.) in the total IO count or not.
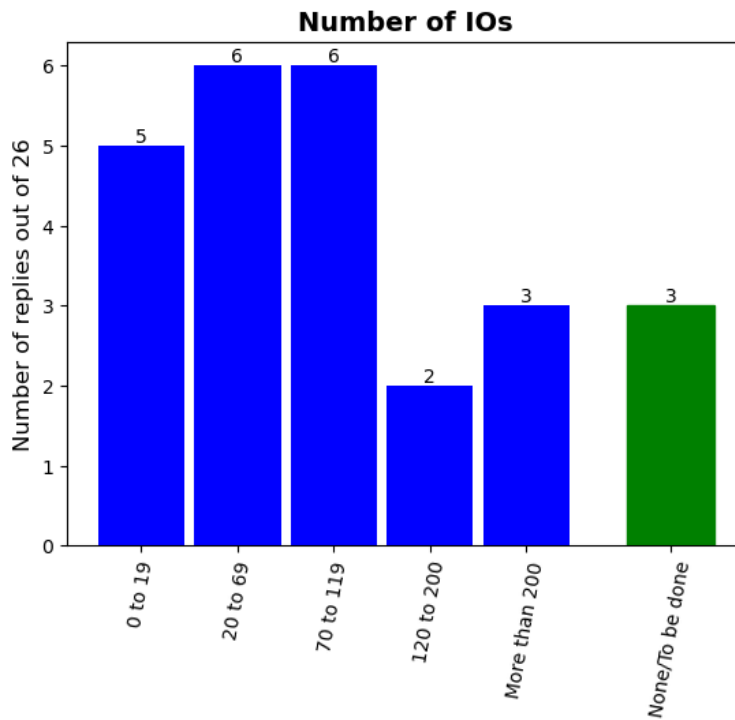
Figure 20: Replies to question 2.4.1 - How many GPIOs do you foresee?

3.5.2 Number and type of communication buses

Question 2.4.2: How many communication buses do you need, e.g. for UART, I2C, SPI, JTAG, etc.?

In order to analyse the replies to this question a larger analysis, including answers from other questions, was conducted. As a result, it can be concluded that most of the projects use Ethernet, both 1G and 10G. Three responses mentioned SATA, one mentioned DisplayPort. It was not clear if the answer "AXI" meant the use of Aurora/C2C or PCIe.
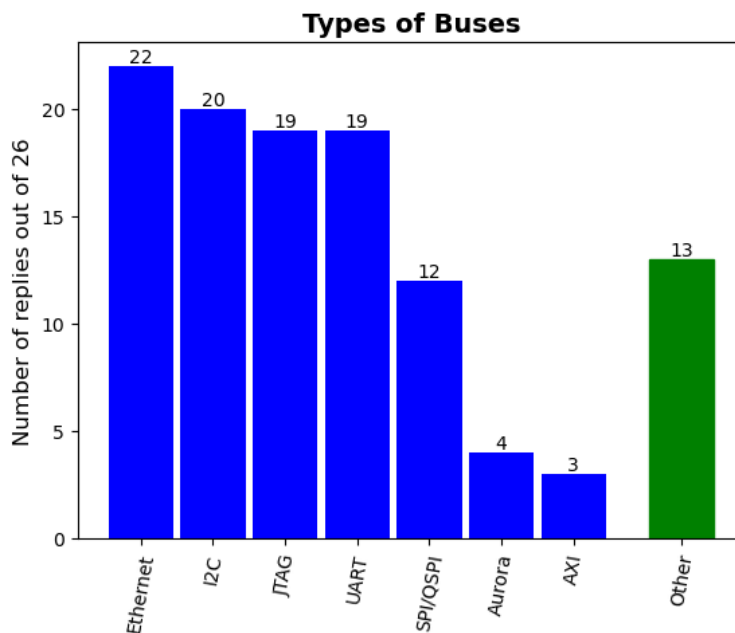

Figure 21: Replies to question 2.4.2 - How many communication buses do you need?

A few projects made the "other" category shoot through the roof – due to unspecified protocol of gigabit links. The assumption taken is that some of the projects had used it for GBT/lpGBT, with a known exception of

ATLAS Global Trigger which will use mostly the Interlaken Core1990 over 25.78125 Gb/s GTM/GTY links.
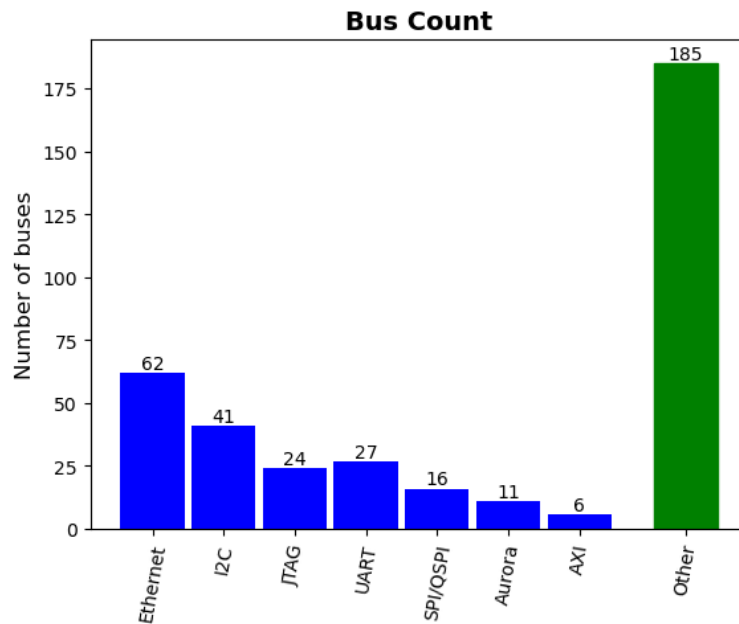
Figure 22: Replies to question 2.4.2 weighted by bus count - How many communication buses do you need?

3.6 Programmable logic

3.6.1 Requirements on programmable logic

Question 2.5.1: What are your requirements on the use of the programmable logic?

The interpretation of the question by the survey respondents turned out to be ambiguous. Some had addressed it considering the functional purpose of the PL, while others were considering more the resource requirements.

Most inputs concerning the logic utilization were vague and not quantitative. Therefore, for the functional purpose, the answers can be grouped into a few categories. In some cases an extrapolation of available information on the different projects was used in order to categorize the reply.
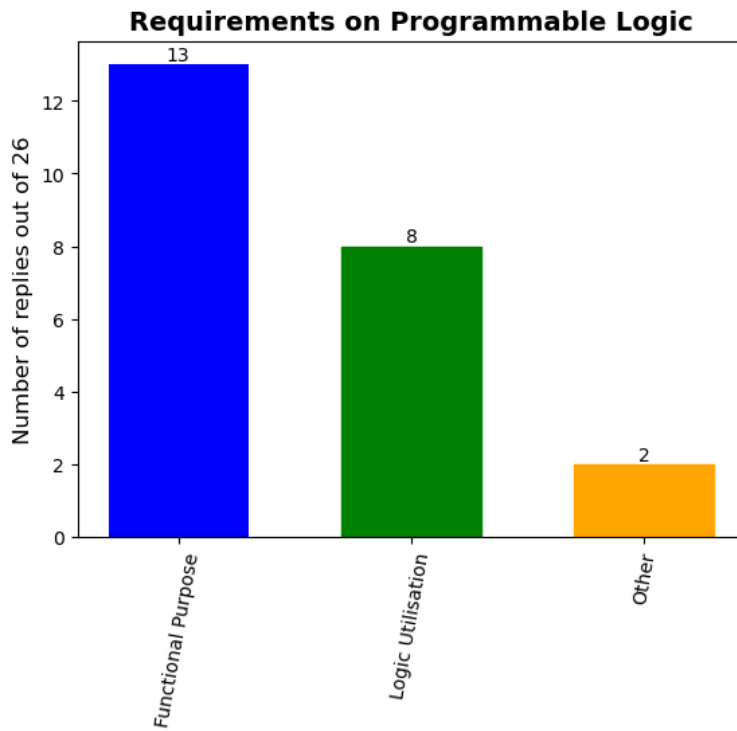
Figure 23: Replies to question 2.5.1 by requirements - What are your requirements on the use of the programmable logic?

For the functional purpose, the answers can be grouped into a few categories. However, even then the answer was not always very clear. In few cases google was used to learn more about project and the possible use cases.

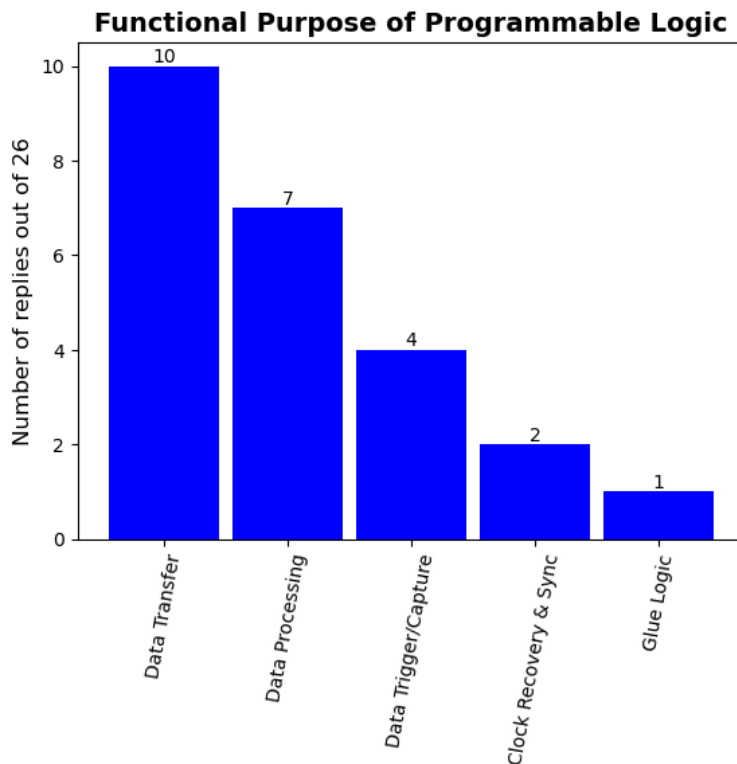

Figure 24: Replies to question 2.5.1 by functional purpose - What are your requirements on the use of the programmable logic?

3.7 Operating system

3.7.1 Choice of operating system

> Question 2.6.1: Which operating system are you using or planning to use?

From previous questions, all projects are using ZynqMP.

All projects use or are planning to use Linux for the regular ARM processing (ARM Cortex-A) cores. Some projects use/intend to use the real-time (ARM Cortex-R5) cores: for real-time applications in the accelerator/technical sector and for the IPMC in the experiment ATCA environment. For these real-time cores FreeRTOS is the choice.

Concerning which Linux distribution: the experiments use PetaLinux and CentOS7/CentOS8 as root file system; the other projects use PetaLinux and are using/considering CentOS, Debian, or Ubuntu.

3.7.2 Reasons for not using Linux

> Question 2.6.2: If Linux is not your choice, please elaborate why? Do you foresee a reason why a common Linux solution will not work?

There was no feedback on the question for a reason why a common Linux solution will not work.

3.7.3 Real-time requirements

> Question 2.6.3: Do you have real-time requirements?

The inputs provided imply that there were different interpretations to the meaning of 'real-time'.

The experiments mostly do not require any real-time, while for the IPMC FreeRTOS is run on the SoC's R5 cores. Some replies mention logic in PL for real-time.

For the other projects there is a mix of 'No' and 'Yes'. In case of 'Yes', the real-time functionality is implemented in the PL, or using FreeRTOS or bare-metal code on the SoC's R5 cores.

3.7.4 Particular devices or features

> Question 2.6.4: If known already, for which particular device or feature will you need support for within the operating system kernel?

Most replies mention the Xilinx IP cores and associated drivers. Particular attention was given to DMA controllers. Some projects mention, in addition, PMBus, IRPS5401, and Si5341. One project in an experiment mentions DHCP ClientID support.

3.8 Memory

3.8.1 Memory requirements

> Question 2.7.1: What are you requirements on memory?
> (E.g. size and bandwidth?

Most projects indicated that 4GB DDR4 seems reasonable for Linux. Few pointed out that they use less now, one project needs more than 8 GB.

3.9 Network

3.9.1 Network requirements

> Question 2.8.1: What are your requirements on network? How many links and what bandwidth do you require?
> (Details are welcome)

Experiments have typically ATCA-based systems and need 2x 1 GbE, sometimes 1x is sufficient.
Few have, in addition, expressed a need for 10 GbE.

3.9.2 Network connectivity

> Question 2.8.2: Do you prefer a direct connection to a technical control network or do you prefer to have the SoM protected behind a gateway PC or an LAN DB set?
> (Please elaborate)

All answers were equally spread between direct connection, gateway or control set, no preference, and still to be determined. Four projects did replied 'No' or gave an unclear answer.
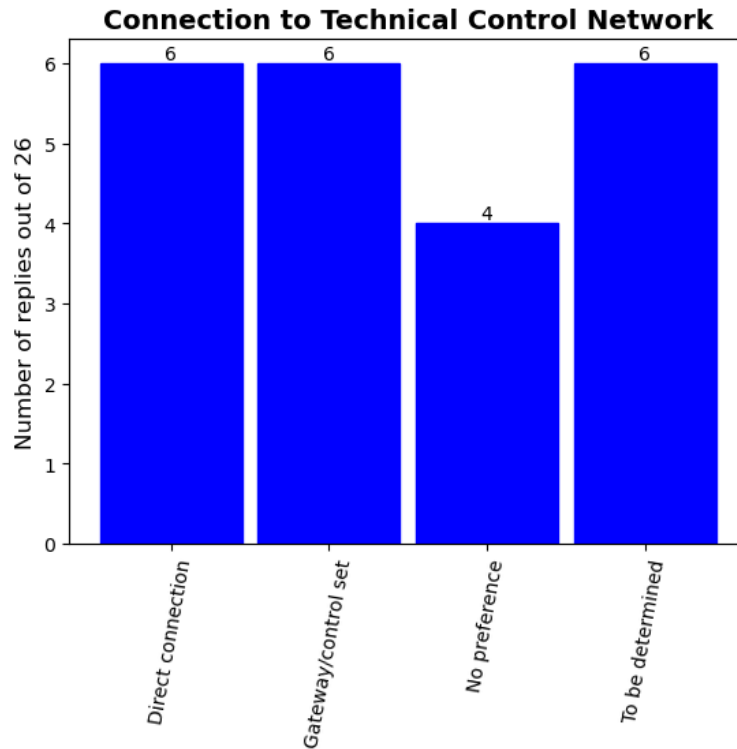

Figure 25: Replies to question 2.8.2 - Do you prefer a direct connection to a technical control network or do you prefer to have the SoM protected behind a gateway PC or an LAN DB set?

4   Other criteria for selection of SoM

4.1   Limitations

> Question 2.9.1: Limitations to consider: form factor, connectors, power?

The most frequent answer to the limitations to consider was the form factor, including size, height with heat sink, etc. This was followed by the cooling, in particular, for the space it takes in air flow. Then came the power required, followed by connectors and IO, in general, for the GBTx IO standard, and the RF performance. Four projects did not foresee any limitations as the design was already finished. Seven projects did not provide any answer to this question.
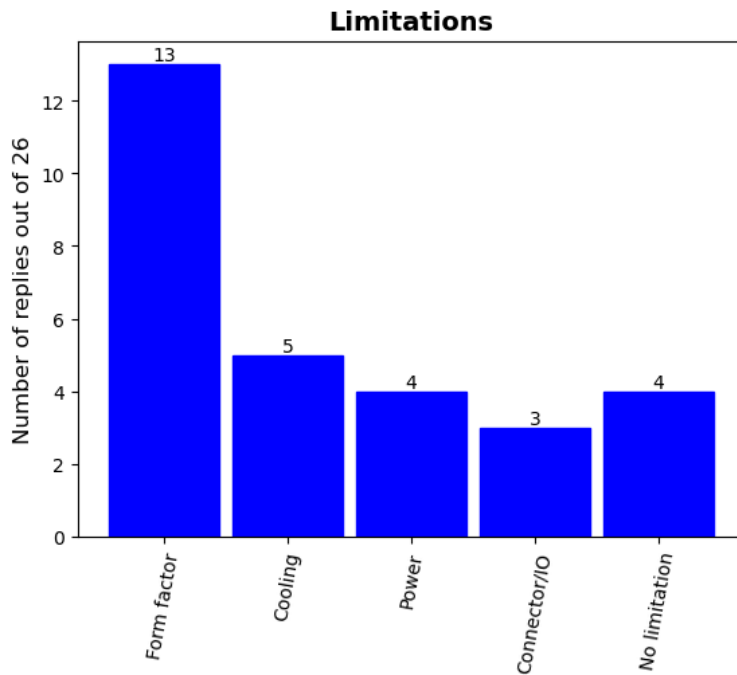
Figure 26: Replies to question 2.9.1 - Limitations to consider?

4.2 Customer support

Question 2.10.1: Do you have comments on the customer support provided by the SoM manufacturer?

More than 50% of the respondents did not answer this question. Out of the 50% who did, half indicated that they were either 'Happy' or 'OK' with the customer support (1x Enclustra, 3x Trenz, 1x Aldec, 1x Xilinx). The others indicated an issue of missing schematics (3x), and long-term support and obsolescence management, in particular, for more than ten years (2x).
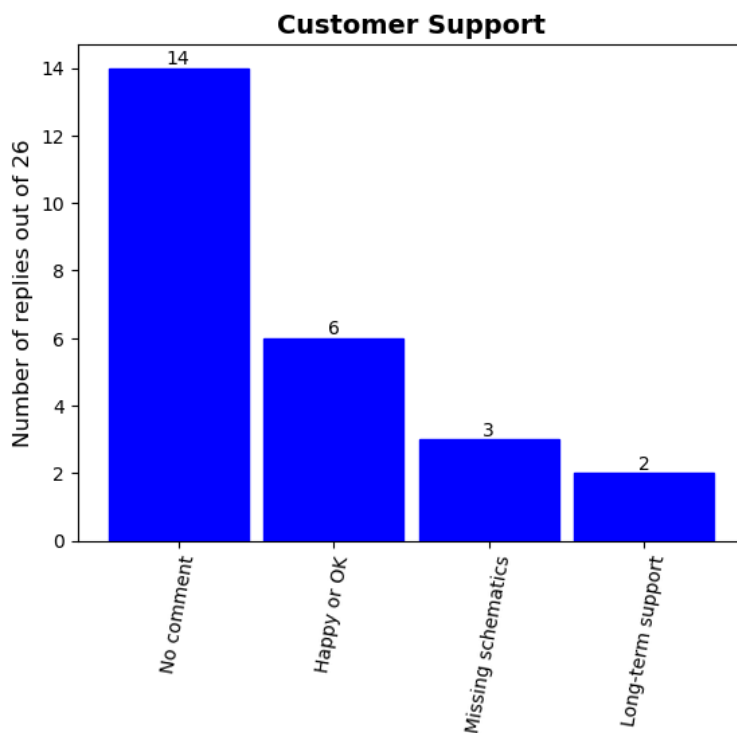

Figure 27: Replies to question 2.10.1 - Do you have comments on the customer support provided by the SoM manufacturer?

4.3 Wish list

Question 2.11.1: Do you have particular wishes or features of the SoM that would be good to have?

The following list summarizes the overall inputs provided by the respondents:

- Tighter PL-PS coupling (e.g. latency)

- More powerful processor (e.g. x86)

- Complete design examples

- Larger eMMC (mentioned twice!)

- Connector standardisation

- CERN support for a common SoC operating system

- Common SoC framework

- Minimal requirement on what software to run on SoC

- RF clocking circuitry, better clocking SoM PLLs, clock chip, mentioned three times!

- PL DDR memories

- Integrate IPMC functionality

- SoM with cooling (heatsink and fan mount)

- Many PS boot options supported

5   Other remarks

Following are extra comments included in the provided feedback:

- Some concerted effort to have PetaLinux CI wrappers would be really great. We are also facing some issues in moving away from 2019.2 (Vivado) to 2021.2 that is fully Vitis.

- We might use the PL of the Zynq to do online calibration of the Front-End raw data and save FPGA resources.

- Many thanks to the CERN SoC group!

6   Conclusion

This study has outlined a clearly growing interest in System-on-Modules (SoM) and more generally in System-on-Chips (SoC). 26 teams responded to the survey across ATLAS and CMS experiments, the Accelerator and Technology Sector and the radiation protection group. The study has shown many common technical choices but has also raised some concerns.

All responding teams are using AMD Xilinx SoCs such as the Zynq 7000, the UltraScale+ Zynq MPSoC or Versal. The majority of SoMs are from Enclustra, Trenz or Xilinx, and most of them are using an Ethernet connection. The choice of a SoM is majorly driven by previous experience, availability of design examples, and widely available documentation. The concerns, on the other hand, focus on hardware portability due to lack of standardisation of inter-board connectors and procurement issues. The most frequent answer to the question of limitations to consider was the form factor, including size, and height with the heat sink mounted. Vendor lock-in due to the non-standard connector tightens the developer to one SoM manufacturer and rises the concern of long-time support. This worry is exacerbated by the current chip shortage that lengthens delivery time. From the software and firmware aspect, although, very few teams are requiring real-time operating system, most of them are using the SoMs for hardware control and monitoring applications. The survey shows that the majority of the teams are using or planning to use Linux-based operating systems such as PetaLinux, CentOS or Ubuntu for ARM processing cores. The programmable logic of the SoC is used mainly for data collection and electronics interfacing.

Overall, the survey provides a clear and comprehensible snapshot of the trajectory that SoM, and more widely SoC, is taking at CERN and throughout the experiments. The findings of this survey will serve as a valuable resource for the SoC Interest Group Organising Committee in determining the direction of future developments, in order to make informed recommendations to our community.

Appendix A   Classification of Multi-Gigabit Links

Link type	Link usage
Versal™ ACAP GTY (32.75Gb/s)	Optimized for latency and power reduction
Versal ACAP GTM (58Gb/s)	Tuned for the latest copper cable, backplane, and optical interfaces with PAM4 and NRZ support
Versal ACAP GTM (112Gb/s)	Scaling for 800G Networks on Existing Infrastructure
UltraScale+™ GTR (6.0Gb/s)	Easiest integration of common protocols to the Zynq Processor Subsystem
UltraScale+ GTH (16.3Gb/s)	Low power & high performance for the toughest backplanes
UltraScale+ GTY (32.75Gb/s)	Maximum NRZ performance for the fastest optical and backplane applications; 33G transceivers for chip-to-chip, chip-to-optics, and 28G backplanes
UltraScale™ GTH (16.3Gb/s)	Low power & high performance for the toughest backplanes
UltraScale GTY (30.5Gb/s)	High performance for optical and backplane applications; 30G transceivers for chip-to-chip, chip-to-optics, and 28G backplanes
UltraScale+ GTM (58Gb/s)	Maximum performance using PAM4 for 58G chip-to-chip, chip-to-optics, and backplane applications
7 Series GTP (6.6Gb/s)	Power optimized transceiver for consumer and legacy serial standards
7 Series GTX (12.5Gb/s)	Lowest jitter and strongest equalization in a mid-range transceiver
7 Series GTH (13.1Gb/s)	Backplane and optical performance through world class jitter and equalization
7 Series GTZ (28.05Gb/s)	Highest rate, lowest jitter 28G transceiver in a 28nm FPGA
Spartan-6® GTP (3.2Gb/s)	Power and cost optimized transceiver for cost-sensitive applications