RESEARCH INSTITUTE FOR HIGH ENERGY PHYSICS

REPORT SERIES

HU - SEFT RD 1995 - 04

First Testbench Measurements of the DELPHI Vertex Detector Outer Layer Modules for the 1996 Upgrade

R. Brenner and C. Eklund

Research Institute for High Energy Physics and
Physics Department, University of Helsinki, Finland

SEFT

ISSN 0788-3587

UNIVERSITY OF HELSINKI
RESEARCH INSTITUTE FOR HIGH ENERGY PHYSICS
P.O.Box 9 • FIN-00014 UNIVERSITY OF HELSINKI • FINLAND

First Testbench Measurements of the DELPHI Vertex Detector Outer Layer Modules for the 1996 Upgrade

R. Brenner, C. Eklund

Abstract

SEFT is assembling silicon detector modules which will be used in the DELPHI Vertex Detector upgrade 1996. The first modules have been assembled and we are presenting the results from the first testbench measurements.

1. Introduction

In the preparation for LEP200 the DELPHI Vertex Detector (VD) is upgraded to cover a bigger part of the solid angle. The VD geometry is completely reshuffled. The present barrel is extended by 24 cm and a forward tracker with tilted modules is being added to both ends of the barrel. The proposal for the upgrade can be found [1].

New outer layer ladders are now being produced for the barrel. The ladders consist of two electrically independent double sided modules which will give two-dimensional hit information. Since both new readout electronics and new sensors are developed for this project the performance is hard to estimate. We will here present the measurements of the noise performance of the first module which was built at SEFT .

2. Module layout

A double sided hybrid with five readout chips connected to four daisy-chained silicon microstrip sensors on each side form a module. The five readout chips, first in the readout chain, are connected to rphi-sensors with strips parallel to the beam axis. The last five readout chips are connected to rz-sensors with strips orthogonal to the beam axis. The rphi- and rz-sensors are glued back-to-back with a ceramic spacer with the same thickness as the hybrid in between. A sideview of a half module is shown in figure 1, where the around 600 μm gap between the rphi- and rz-sensors is clearly visible.

The rphi-sensors, produced by Hamamatsu, are AC-coupled, FOXFET biased and have an area of 30 x 60 mm^2. The strip pitch is 25 μm with 50 μm readout pitch leaving every second strip floating for capacitive charge division. The rz-sensors, produced by SINTEF, have the same size as the rphi-sensors however trusting on more classic polysilicon biasing. The strip pitch is 50 μm but the readout pitch is split into three groups.

The sensor closest to the interaction point, in the center of the ladder, has two compartments with 640 readout strips and 50 μm pitch. Next sensor towards the hybrid has 640 readout strips with 100 μm pitch and the two sensors closest to the hybrid have 320 readout strips each with 200 μm pitch. To avoid having readout electronics in the sensitive volume the readout lines, the metal 1 layer, are connected to routing lines orthogonal to the readout lines, the metal 2 layer, which will bring the signal to the readout chips on the hybrid.

Hence the double metal technique which was developed for the double sided sensors presently in the DELPHI VD was used for the rz-sensors. The readout lines are in this technique separated with an about 5 μm thick polyimid layer. The rz-side of a module is shown in figure 2.

The MX6 readout chip used in the present VD has been redesigned to stand the high capacitance required by long modules. The new TRIPLEX chip is basically the MX6 chip made in the more dense 1.2 μm AMS process. Figure 3 shows a close view of the hybrid with TRIPLEX chips bonded to a sensor. New features such as band-width limit and triggering capabilities give some additional advantages to the chip compared to the precessor. The trigger capability is activated on the five first chips which are connected to the rphi-sensors. We have not tested the trigger and will not discuss the trigger in this paper.

3. Mounting

Big care has been put into the mounting of the detector modules. Several jigs are needed for the mounting. The goal is that the alignment should reach a precision better than 50 μm.

The hybrid and the rz-sensors are aligned under a microscope on a mounting jig with four xy-translation and rotation stages for the sensors and one x-translation stage for the hybrid. Figure 4 shows the microscope setup and figure 5 a close view of the mounting jigs. The sensors and the hybrid are kept on the jig with vacuum. The first sensor is glued on top of the hybrid. After the glue has cured the four sensors and the hybrid are lifted from the mounting jig with a pick-up jig. The sensors are held by vacuum onto the pick-up jig and the hybrid is hanging from the sensors. The four rphi-sensors are aligned on the same mounting jig and lifted by a second pick-up jig. The ceramic pieces joining the sensors are applied when the sensors are on the pick-up jig just before the module is made by sandwiching the two sensor layers together.

Figure 6 shows the two pick-up jigs in position for sandwiching. The clock on the top jig is need to sense when the sensors are touching each other.

The sensors on the rphi-side and those on the rz-side have independent biasing. The electrical contact to the back-planes is done by E-solder epoxy, but some additional Araldite is needed to improve the mechanical strength.

Electrical tests are done between each sensor being wire bonded to the readout electronics.

4. Measurements

Several electrical measurements have been done to find out the settings for getting the optimal performance of the module.

Scan of integration time:

The TRIPLEX chip uses the method of double correlated sampling for signal filtering [2]. By scanning the width of the integration window the risetime of the signal and noise can be studied. If the integration time is short there will not be enough time to collect the full charge but on the other hand the noise will also be reduced. If the integration time is long the full signal will be collected but the noise will increase because of the parallel noise mainly from the biasing resistors. The optimal adjustment is when the integration time is about the same as the shaping time of the TRIPLEX.

The signal and noise plots for the rphi- and rz-side with fast shaping is shown in figure 7. The corresponding plot for a slow shaping time is shown in figure 8. The rphi-sensors show a lower noise than the rz-sensors because of lower capacitance. At long integration times the noise hardly increases reflecting the minimal contribution of parallel noise. The typical integration time in the experiment will be around 3 μs.

Band-Width Limit scan:

The Band-With Limit adjustment is done by setting a resistor in front of the storage capacitors by an external voltage. Figure 9 shows the effect of the noise and signal for a BWL-voltage scan from 0V to 1.8V for the rphi-side. The corresponding plot for the rz-side is shown in figure 10. High settings of BWL voltage reduce the gain in the TRIPLEX but also the noise. The Signal/Noise clearly peaks towards the end for the rphi-side but for the rz-side the curve flattens out. The optimal operation point for the BWL is above 1 V.

Noise performance:

The performance of the module was retested each time an additional sensor was bonded to the module. Figure 11 shows the noise, including the system noise, for 2,3 and 4 sensors on rphi-a nd rz-side connected to the triplex . The capacitance for the rphi-side is expected to be around 1.4 pF/cm. For the rz-side the capacitance is more complicated to estimate because of the capacitance contribution both from the first metal layer with implants and the second metal layer coupling through the insulation to the first metal layer. Given the first metal layer contribution of 1.4 pF/cm a second metal layer contribution of 1.2 pF/cm gives good agreement with the measurements. The real situation is, however, much more complicated than only noise contribution from capacitive load. The long modules have a large contribution from the series resistance arising from the sheet resistance in the metal lines. The series resistance scales the contribution from the capacitance making the noise slope steeper. The fit in figure 11 is done using only the points from the rphi-side. The rz-points, however, follow well the fit. The fitted value of the noise slope does not reflect the design performance of the TRIPLEX because the slope is affected by the series resistance.

Calibration with ^{90}Sr beta source:

The calibration of the setup was done with a ^{90}Sr source. High momentum betas were selected using two semiconductor triggers in coincidence placed on both sides of the module. Only betas transversing the module inside the integration time window were selected. The distribution obtained differs from a clean Landau distribution because of contamination from low momentum betas which broadens the high energy tail of the distribution. The low energy tail is broadened by betas entering in the beginning or at the end of the integration window and not reaching full pulse-height. Figure 12 shows a beta spectrum fitted with a landau distribution.

5. Conclusions

We have studied a module produced for the DELPHI Vertex Detector upgrade in 1996. The 24 cm long modules with standard rphi- and double metal rz-sensors show a good performance with TRIPLEX chips despite the high capacitance. The noise for the rphi-side of the module is around 1000 ENC and for the rz-side 1200 ENC resulting in a signal to noise ratio better than 20 for a MIP for the module. The good performance is achieved when Band-Width Limiting the TRIPLEX.

6. Acknowledgements

We want to thank Antti Numminen and Mirja Luoma for the skillful work they did in assembling and bonding and repairing the module. We want also thank Olle Byström and Lasse Lindqvist from Uppsala University with the design and construction work on the jigs.

7. References

1. The DELPHI Collaboration, An Upgrade of DELPHI in the Forward Region, Letter of Intent, CERN/LEPC/92-5, May 1992

2. J. C. Stanton, A low Power Low Noise Amplifier for A 128 Channel Detector Read-Out Integrated Circuit, RAL-89-009, February 1989

8. Figures

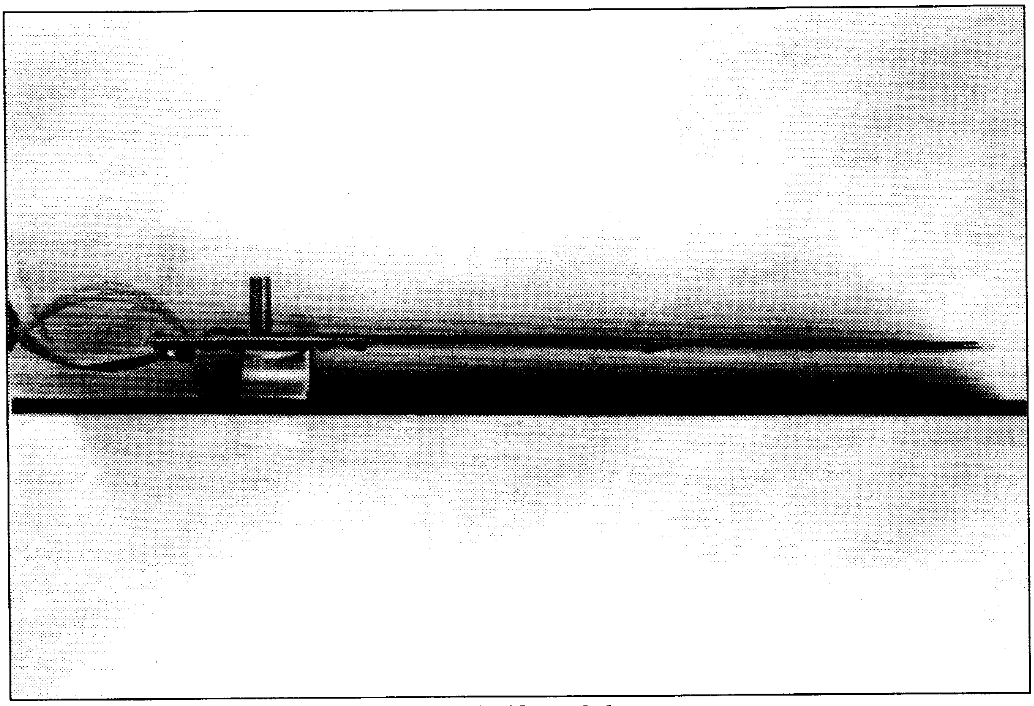

Figure 1: A side view of a detector half-module.

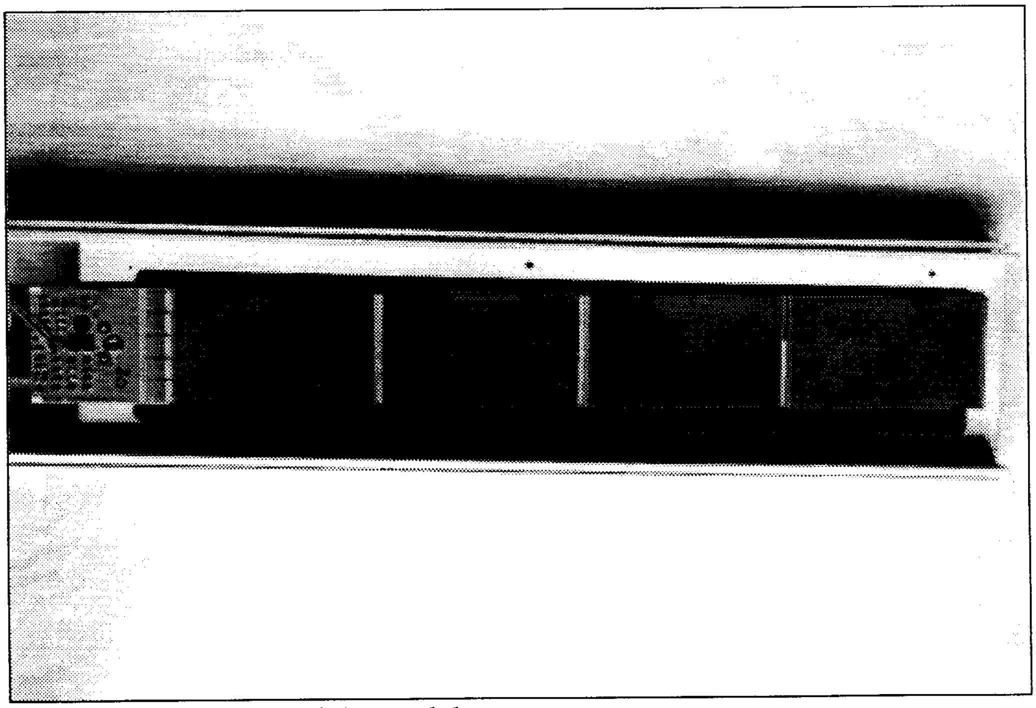

Figure 2: The rz-side of the module.

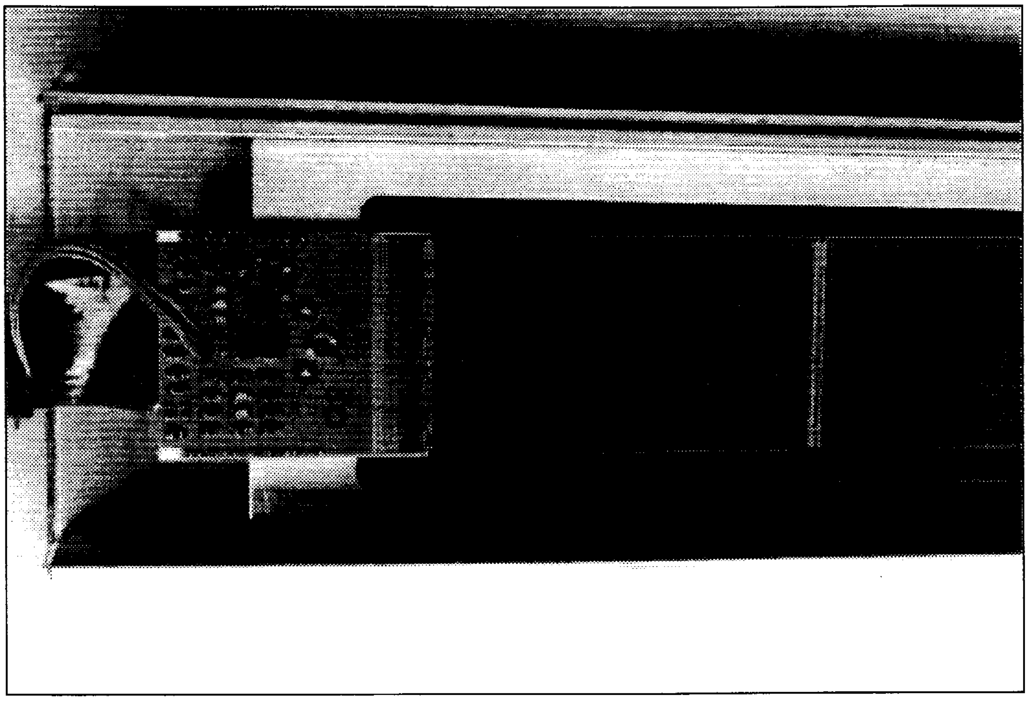

Figure 3: A close view of the hybrid with five TRIPLEX chips bonded to a sensor.

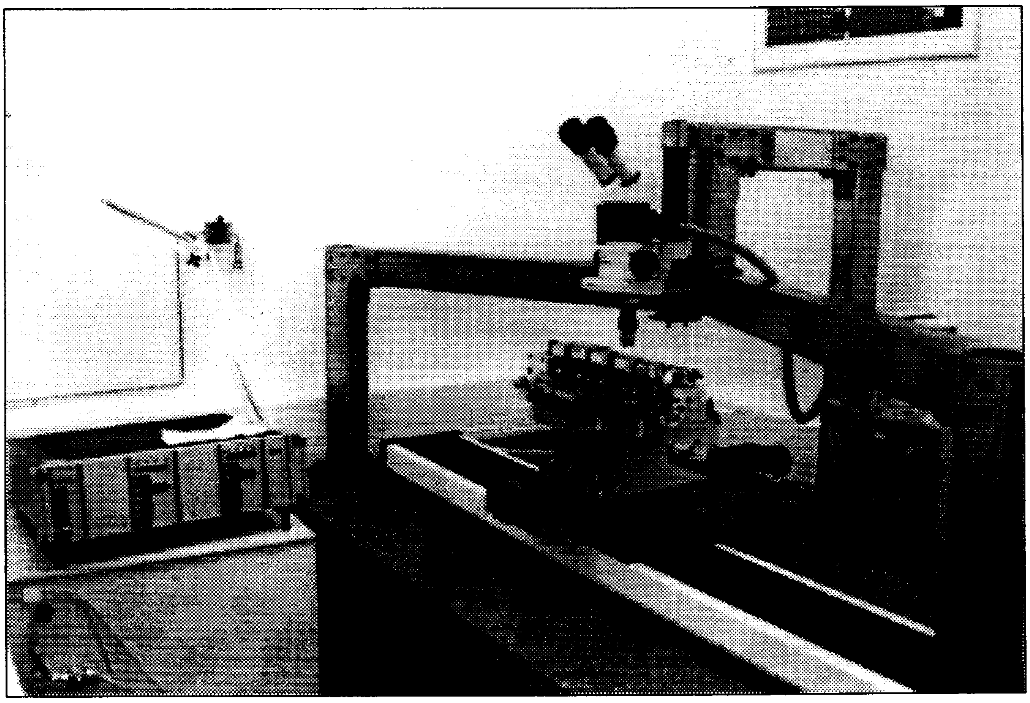

Figure 4: The mounting jig under the microscope.

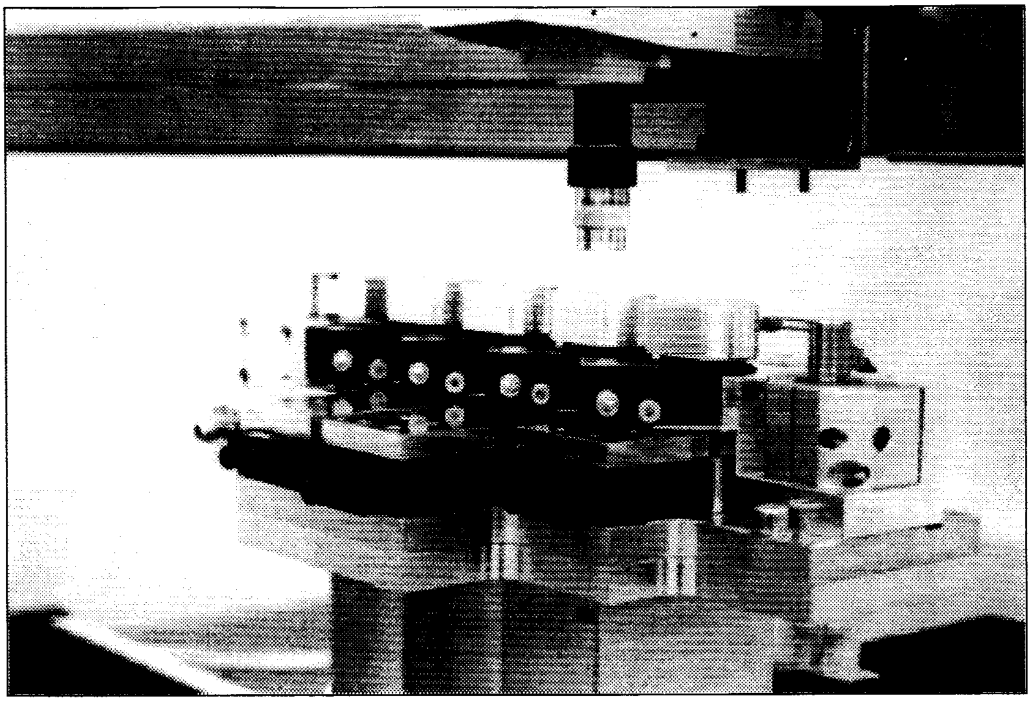

Figure 5: A close view of the mounting jig.

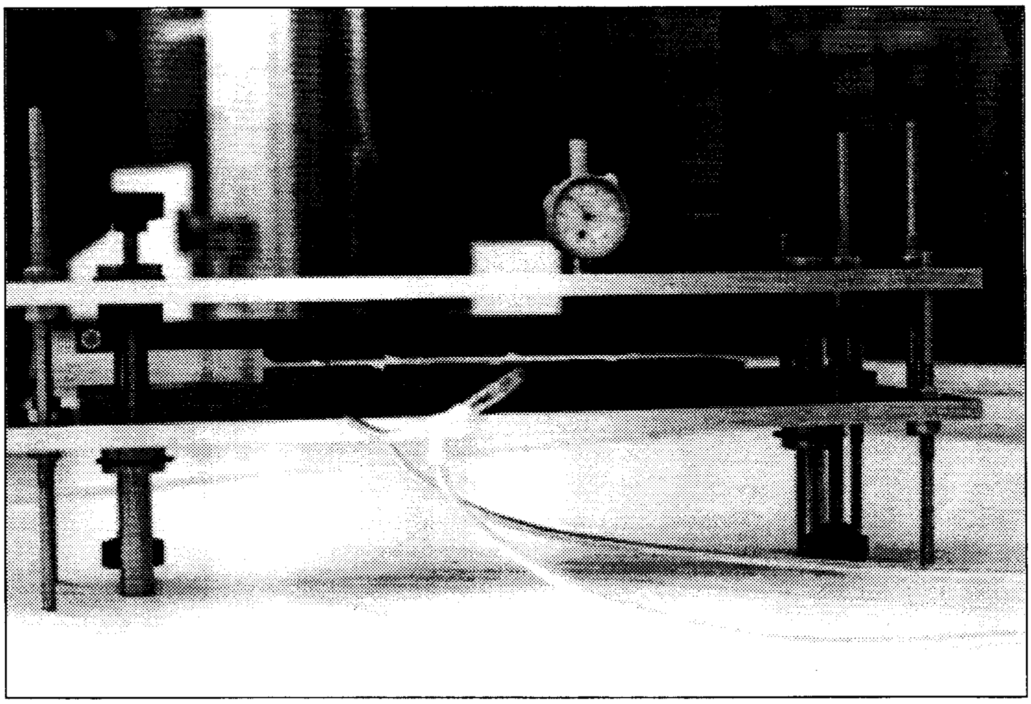

Figure 6: The pick-up jigs in position for sandwiching a module.

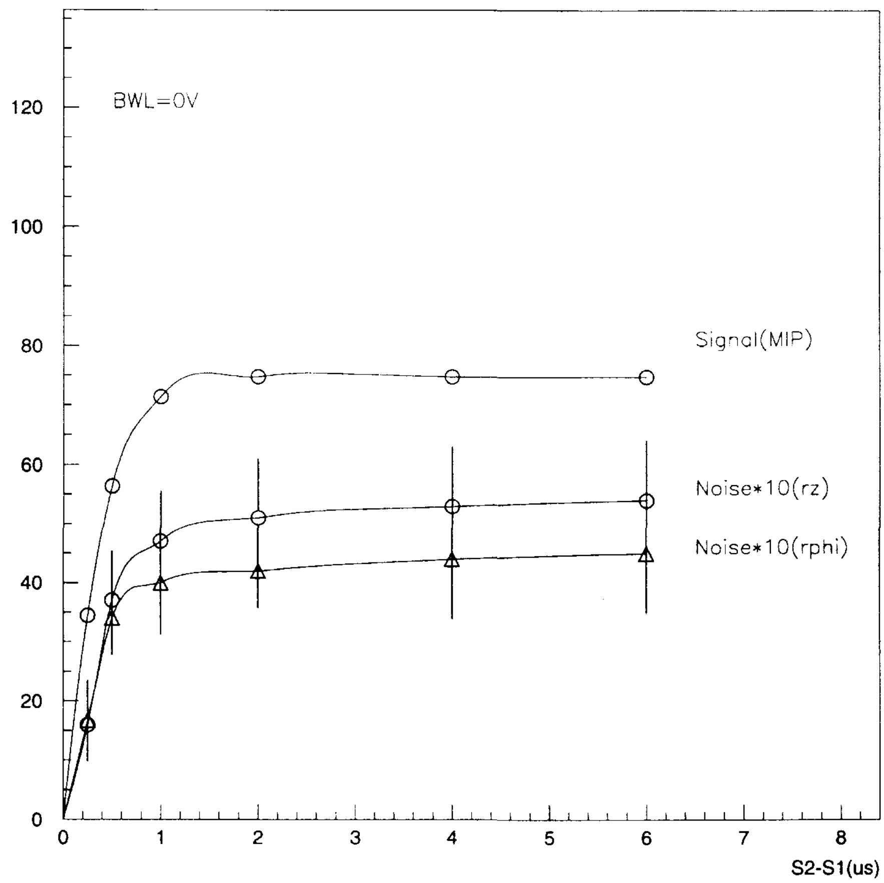

Figure 7: Scan of integration time with fast shaping.

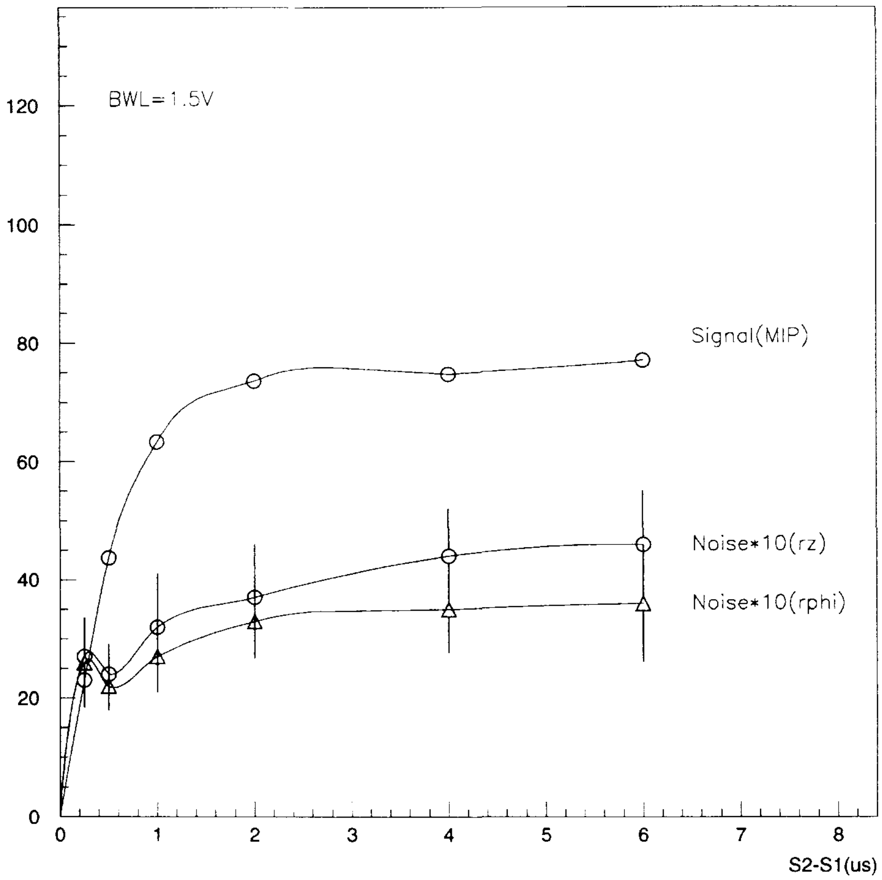

Figure 8: Scan of integration time with slow shaping.

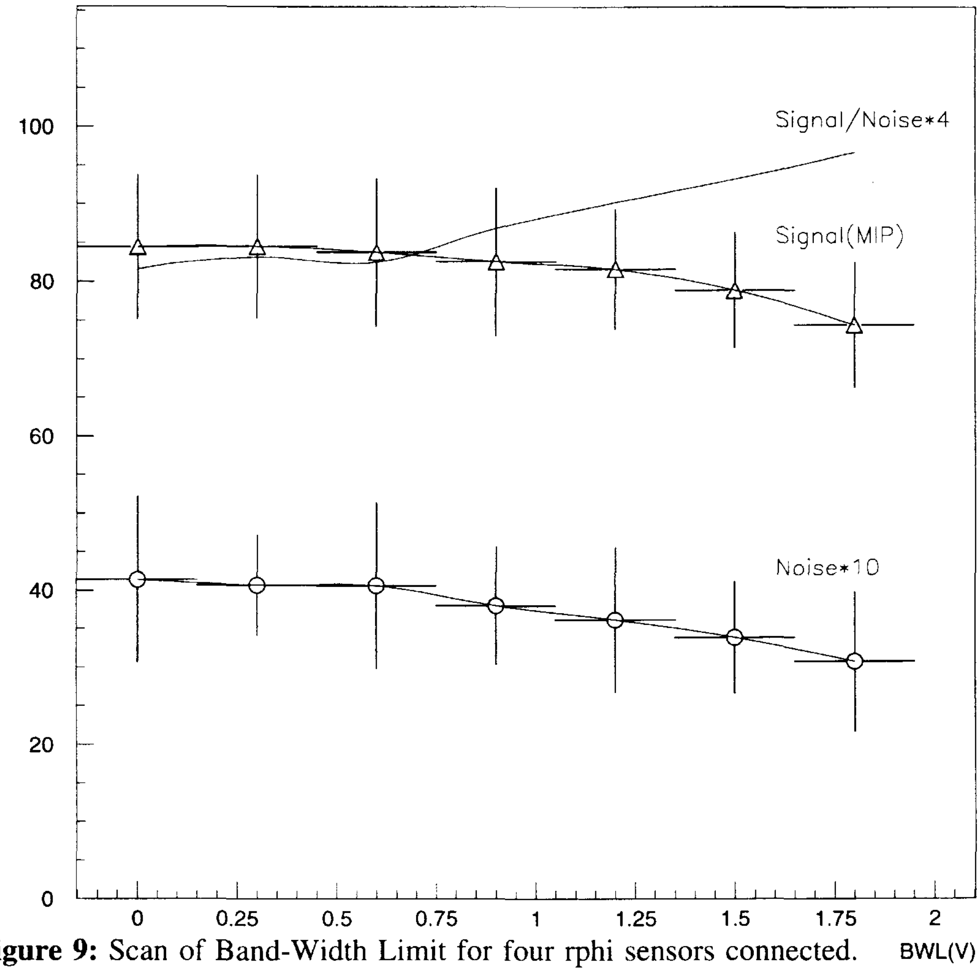

Figure 9: Scan of Band-Width Limit for four rphi sensors connected.

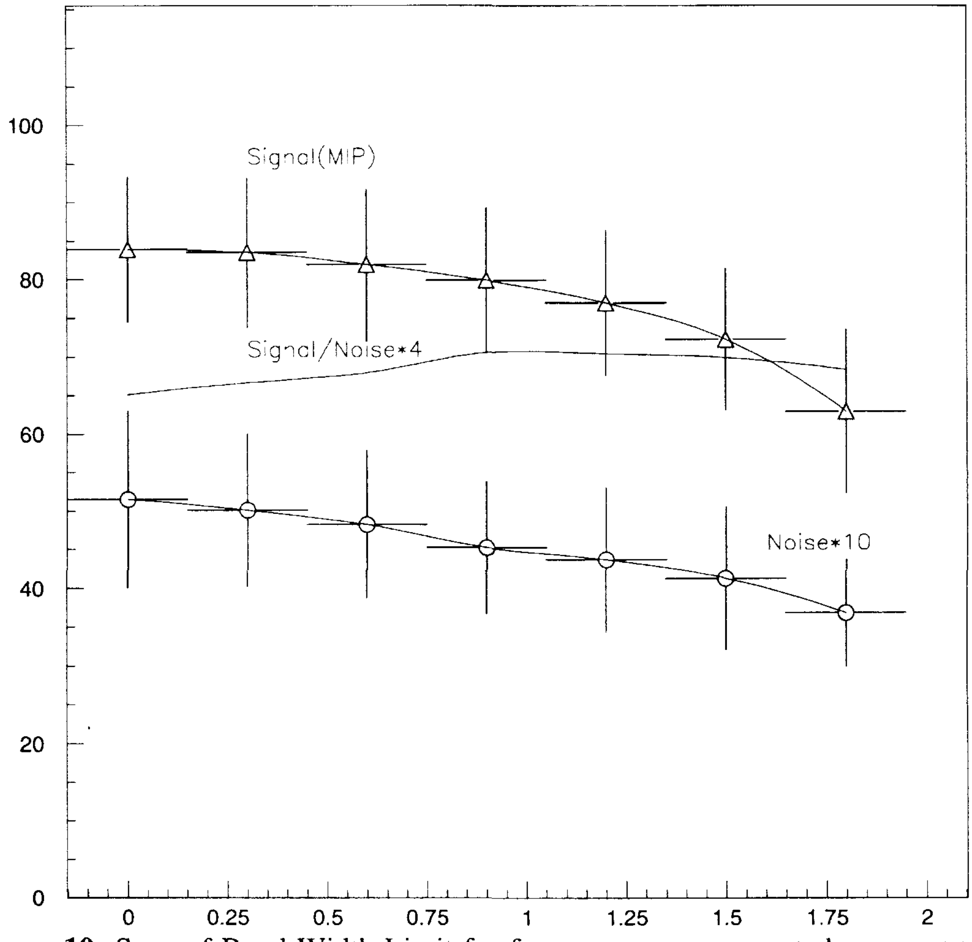

Figure 10: Scan of Band-Width Limit for four rz-sensors connected.

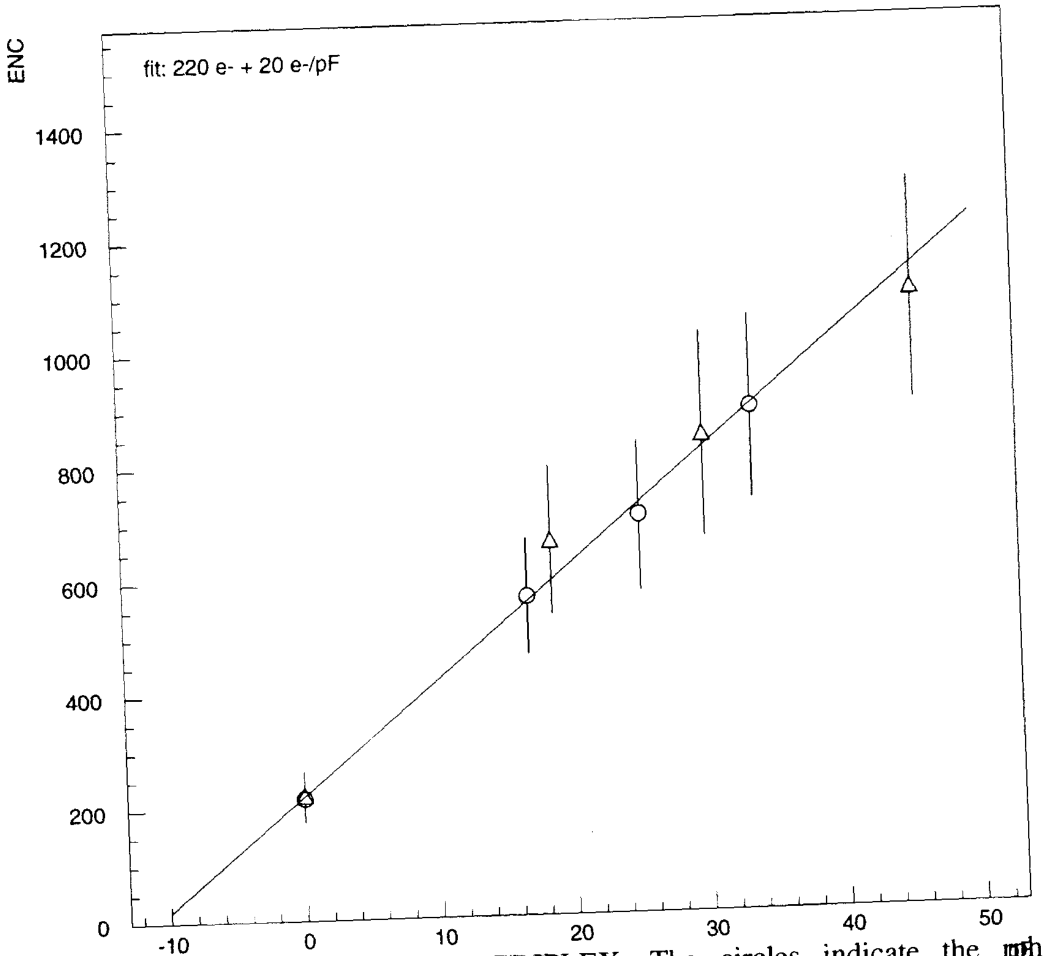

Figure 11: Noise slope of the TRIPLEX. The circles indicate the rphi measurements and the triangles the rz-measurements.

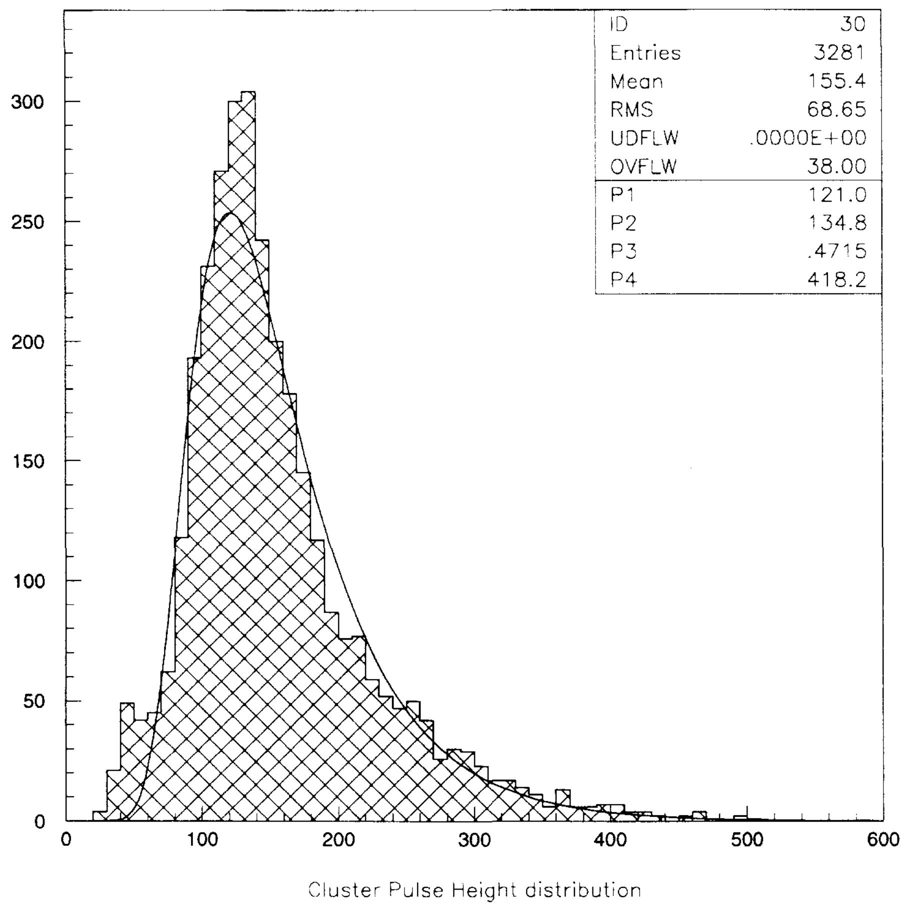

Figure 12: The pulse-height distribution from the rphi-side fitted with a Landau distribution.